Effect of ultrathin GeO_x interfacial layer formed by thermal oxidation on Al_2O_3 capped Ge*

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We propose a modified thermal oxidation method in which an Al_2O_3 capping layer is used as an oxygen blocking layer (OBL) to form an ultrathin GeO_x interfacial layer, and obtain a superior Al_2O_3/GeO_x/Ge gate stack. The GeO_x interfacial layer is formed in oxidation reaction by oxygen passing through the Al_2O_3 OBL, in which the Al_2O_3 layer could restrain the oxygen diffusion and suppress the GeO desorption during thermal treatment. The thickness of the GeO_x interfacial layer would dramatically decrease as the thickness of Al_2O_3 OBL increases, which is beneficial to achieving an ultrathin GeO_x interfacial layer to satisfy the demand for small equivalent oxide thickness (EOT). In addition, the thickness of the GeO_x interfacial layer has little influence on the passivation effect of the Al_2O_3/Ge interface. Ge (100) p-channel metal–oxide–semiconductor field-effect transistors (pMOSFETs) using the Al_2O_3/GeO_x/Ge gate stacks exhibit excellent electrical characteristics; that is, a drain current on-off (I_{on}/I_{off}) ratio of above 1×10^4, a subthreshold slope of $\sim$ 120 mV/dec, and a peak hole mobility of 265 $cm^2/V\cdot s$ are achieved.

Keywords: GeO_x interfacial layer, thermal oxidation, GeO desorption, Al_2O_3

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1. Introduction

Si metal–oxide–semiconductor field-effect transistors (MOSFETs) have reached physical and technique limitations with device scaling. Ge has received great attention as a promising candidate for channel material because of its high electron and hole mobility.[1–3] Utilizing high-*k* gate stacks can further improve the performance of Ge MOSFETs. However, the direct deposition of high-*k* dielectric on Ge has been proved to show poor electrical characteristics because of reactions and diffusion between high-*k* metal oxides and Ge surface during thermal treatment. Many efforts, such as sulfur passivation,[4] fluorine passivation,[5] and Si passivation,[6] have been made to protect the interface and reduce interfacial trap density (D_{it}). Forming a thin GeO_2 interfacial layer between high-*k* and Ge is one of the best solutions to improve the interface quality, such as in the SiO_2/Si system.[7–9] However, GeO_2/Ge interface is generally considered to be defective due to GeO desorption under high temperature. Lee *et al.*[10] have used high-pressure oxidation to suppress GeO desorption, while Zhang *et al.*[11] have taken advantage of plasma post oxidation and maintained an ultrathin GeO_2 interfacial layer. Meanwhile, it is significant to scale down the thickness of GeO_2 layer for small equivalent oxide thickness (EOT) due to its low *k* value. Other investigations, such as ozone oxidation[12] and neutral beam oxidation,[13] have also been carried out to form a GeO_x interfacial layer. Nevertheless, to obtain a well controlled thin GeO_2 layer, the most fundamental thermal oxidation method has been seldom reported. Murad *et al.*[14] have utilized a dilute oxidizing ambient to scale down the thickness of GeO_2 to approximately 3 nm by using thermal growth at 550 °C. However, it is still not enough to obtain small EOT gate stacks to satisfy the scaling trend of Ge MOS devices.

In this paper, we employ a thin Al_2O_3 film as an oxygen blocking layer (OBL) to form a thin GeO_x interfacial layer between Al_2O_3 and Ge through using the modified thermal oxidation. The thin Al_2O_3 layer is beneficial to suppressing the oxidation reaction and preventing the GeO desorption from taking place at the GeO_x/Ge interface.[15] Different thermal growth conditions are investigated to optimize the control of GeO_x interfacial layer growth, especially the thickness of Al_2O_3 OBL. MOS capacitors (MOSCAPs) and p-channel MOSFETs are fabricated to investigate the electrical characteristics of the Al_2O_3/GeO_x/Ge gate stacks. Experimental results demonstrate that the modified method is effective in terms of ensuring a scaled EOT, small capacitance–voltage (*C*–*V*) hysteresis, and has excellent interface properties.

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2. Experiment

N-type Ge (100) substrates each with a resistance of $\sim 0.01\ \Omega\cdot$cm were used in this work. After organic substances are cleaned by acetone and alcohol, the Ge substrates were dipped into HCl (12%) solution by cyclic cleaning (three times) to remove native oxides and obtain better surface morphologies.[16] Then the Ge substrates were immediately transferred to the process chamber of atomic layer deposition (ALD) system. Afterwards, the first Al_2O_3 deposition layer, which is the OBL shown in Fig. 1(a), was grown on the Ge substrate by ALD at 300 °C.[17] Thermal oxidation was carried out inside a rapid thermal furnace at atmospheric pressure in pure oxygen ambient at 550 °C to obtain an Al_2O_3/GeO_x/Ge gate stack. The influence of different conditions on growth of GeO_x interfacial layer, such as thickness values of Al_2O_3 OBLs and oxidation time, were investigated by X-ray photoelectron spectroscopy (XPS) measurements and spectroscopy ellipsometry.

For the MOSCAPs, the second Al_2O_3 deposition layer, which is the high-k dielectric shown in Fig. 1(a), was grown on the top of Al_2O_3 OBL/GeO_x/Ge sample by ALD system. Post-deposition oxygen annealing at 550 °C for 10 min in O_2 ambient and low-temperature oxygen annealing for 30 min in O_2 ambient were utilized to improve the gate stack performance.[18,19] Then, Ti/Au top electrodes were deposited by electron beam evaporation, followed by post-metallization annealing at 350 °C in N_2 ambient. The C–V characteristics were measured by an Agilent 4284A precision impedance analyzer. A low-temperature conductance method was used to extract the D_{it} of the Al_2O_3/GeO_x/Ge interface.

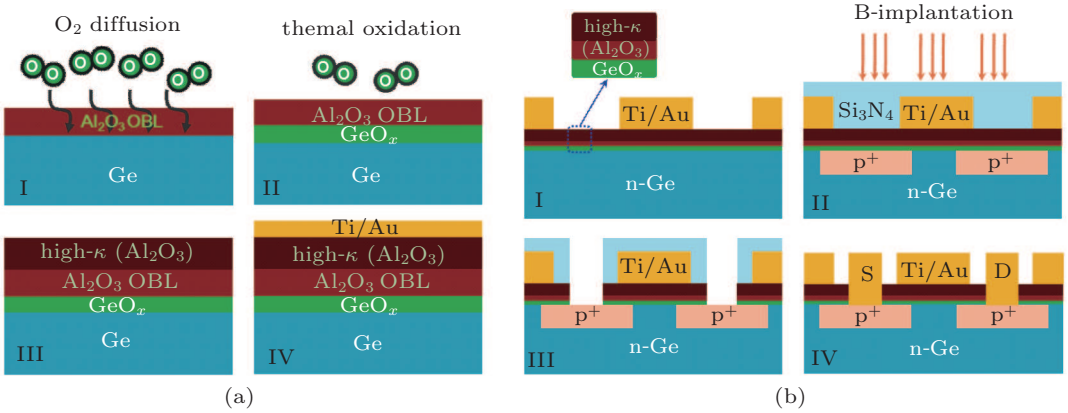


Fig. 1. (color online) Process flow charts for (a) MOSCAPs and (b) pMOSFETs using the Al_2O_3/GeO_x/Ge gate stacks.

The Ge pMOSFETs were fabricated on heavily doped n-type Ge (100) substrates ($\sim 2\times10^{17}$ cm^{-3}) using the Al_2O_3/GeO_x/Ge gate stack. The main fabrication flow of Ge pMOSFETs with gate-first process is shown in Fig. 1(b). A Ti/Au gate electrode was deposited and patterned after the formation of gate stack. Then, the source/drain regions were formed by B^+ ion implantation at a dose of 1×10^{15} cm^{-2} with an energy of 30 keV, followed by activation annealing. The Ni/Pt/Au source/drain contacts were deposited by electron beam evaporation. Current–voltage (I–V) measurements and conventional split C–V method were used to investigate the electric properties of Ge pMOSFETs.

3. Results and discussion

Although GeO_2 could repair the high-k/Ge interface and reduce interface states, GeO_2/Ge is thermodynamically unstable due to GeO desorption from GeO_2/Ge interface. Figure 2(a) shows the redox reaction constant for candidate dielectric oxides on Ge substrates, indicating the poor thermal stability of the GeO_2/Ge interface. The redox reaction constant is directly calculated by thermodynamic database software (HSC Chemistry 7 (version 7.11, ©Outotec)). Thermal desorption spectroscopy (TDS) measurements are performed to reveal the thermal stabilities for GeO_2/Ge and Al_2O_3/Ge. Figure 2(b) shows the TDS results corresponding to GeO deposition, where the mass number of 90 is taken into account and the heating rate is 20 °C/min, which implies that GeO desorption from GeO_2/Ge interface occurs above 400 °C. GeO desorption can generate a huge number of interface states and cause a serious deterioration of electrical properties.[20] Therefore, measures must be taken to protect the GeO_2/Ge interface and suppress the GeO desorption during thermal treatment. However, it is clarified that GeO does not come out from Al_2O_3/Ge stack from 200 °C to 650 °C, as shown in Fig. 2(b). In addition, Al_2O_3 has a small redox reaction constant, which also indicates its better thermal stability on the Ge surface. Furthermore, Tabata *et al.*[21] have proved that Al_2O_3 films can suppress GeO desorption from the Al_2O_3/GeO_x/Ge

stack even at 600 °C. Consequently, Al_2O_3 would work as well as OBL because of its better thermal stability and suppressing effect on GeO desorption from both Al_2O_3/Ge and Al_2O_3/GeO_x/Ge stacks.

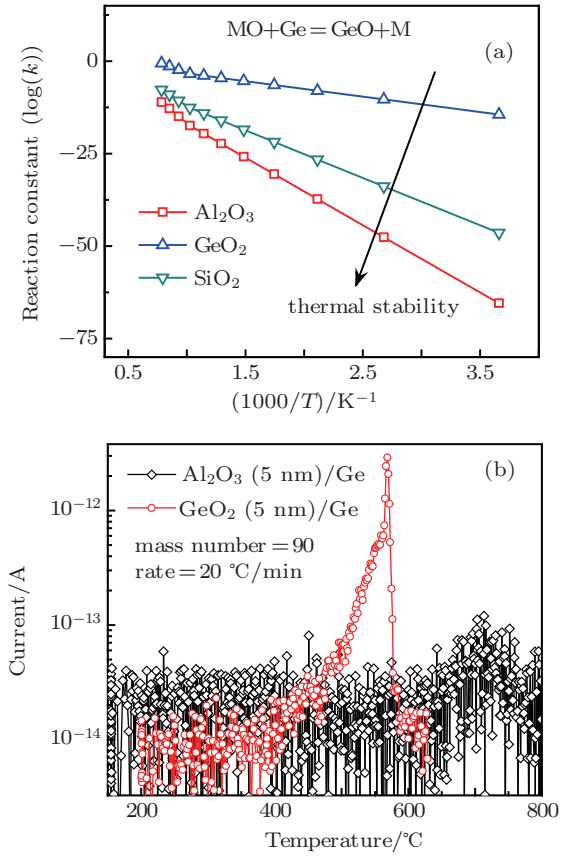


Fig. 2. (color online) (a) Redox reaction constant for candidate dielectric oxides on Ge surface. (b) TDS spectra of GeO desorption from Al_2O_3/Ge and GeO_2/Ge stacks.

In order to acquire a superior Al_2O_3/GeO_x/Ge gate stack by using thermal oxidation method, the oxidation conditions should be analyzed and investigated in detail. Although the low oxidation temperature, like 400 °C or lower, could also reduce the velocity of oxidation, the quality of GeO_x would degrade.[22] Therefore, the thermal growth of high quality GeO_x interfacial layer needs a high temperature condition.[23] Although the D_{it} of GeO_x/Ge interface is found to be reduced as the oxidation temperature increases, the roughness of GeO_x/Ge surface would also increase when the oxidation temperature increases to 600 °C.[24] On the basis of the reported work and our previous experiments, 550 °C would be a proper temperature for the thermal growth of GeO_x.

The effects of GeO_x interfacial layers with different thickness values on interface passivation are examined by the typical *C*–*V* measurement. Figure 3 shows *C*–*V* characteristics of MOSCAPs with different thickness values of GeO_x interfacial layers. The samples, Al_2O_3 (9 nm)/GeO_x (1.7 nm)/Ge and Al_2O_3 (9 nm)/GeO_x (3.9 nm)/Ge MOSCAPs, are obtained by thermal oxidation with 1-nm-thick Al_2O_3 OBL at 550 °C for 10 s and 3 min, respectively, followed by the deposition of 8-nm-thick Al_2O_3 serving as top high-*k* dielectric. It is found that the *C*–*V* curves of MOSCAPs with GeO_x interfacial layers show less frequency dispersion in a flat band than those of MOSCAP with an Al_2O_3 (10 nm)/Ge stack, demonstrating that the Al_2O_3/Ge interface is well passivated by GeO_x interfacial layer. However, frequency dipersion in the flat band of the MOSCAP with 1.7-nm-thick GeO_x interfacial layer is as small as that of MOSCAPs with a 3.9-nm-thick GeO_x interfacial layer. These results indicate the excellent passivation effect of GeO_x interfacial layer on the high-*k*/Ge interface, which is little influenced by the thickness of GeO_x interfacial layer. Consequently, scaling down the thickness value of GeO_x interfacial layer could reduce the EOT of gate stack, without cutting down its effect on interface passivation.

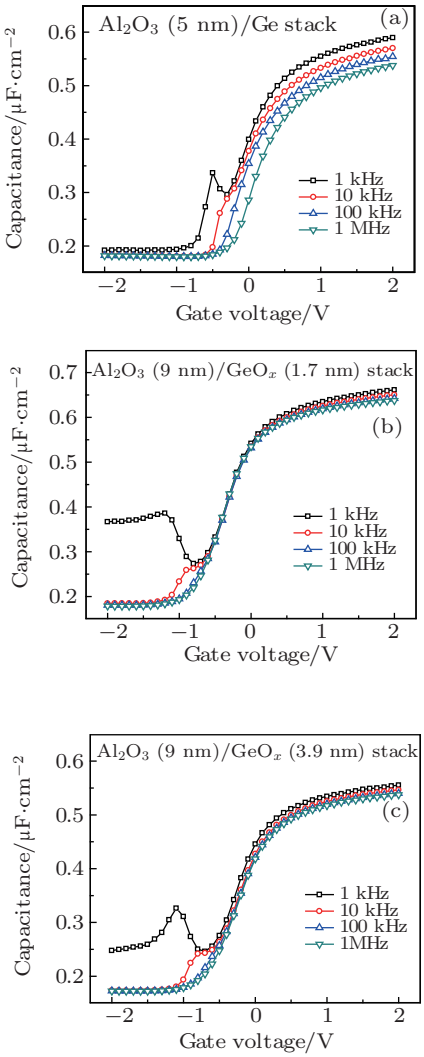


Fig. 3. (color online) *C*–*V* characteristics of MOSCAPs with (a) Al_2O_3 (10 nm)/Ge stack, (b) Al_2O_3 (9 nm)/GeO_x (1.7 nm)/Ge stack, and (c) Al_2O_3 (9 nm)/GeO_x (3.9 nm)/Ge stack.

Furthermore, the thickness of Al_2O_3 OBL is optimized to well achieve control of the thickness value of GeO_x interfacial layer and obtain an ultrathin GeO_x interfacial layer. The effect of Al_2O_3 OBL thickness value on GeO_x growth is inves-

tigated using the XPS method. Figure 4 shows the XPS spectra of Ge 3d core level from $Al_2O_3/GeO_x/Ge$ samples. The Ge substrates with four different thick Al_2O_3 OBLs (0 nm, 0.5 nm, 1.0 nm, and 1.5 nm) are thermally oxidized at 550 °C for 3 min under atmospheric pressure of O_2. The peak observed at a binding energy of 32.5 eV would be attributed to the formation of GeO_x. There is almost no GeO_x growth detected at the interface of the as-deposited 1.5-nm-thick Al_2O_3 on Ge, while it grows into oxide at 550 °C even though it is thin Al_2O_3 OBL. The peak intensity at a binding energy of 32.5 eV dramatically decreases with the increase of Al_2O_3 thickness, especially when the thickness value of Al_2O_3 increases to 1.5 nm. This demonstrates that Al_2O_3 OBL could scale down the thickness of GeO_x interfacial layer effectively.

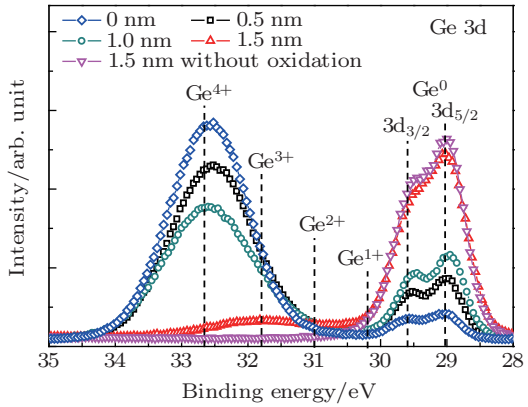


Fig. 4. (color online) XPS spectra of Ge 3d core level from $Al_2O_3/GeO_x/Ge$ samples, with the Ge substrates with four different thick Al_2O_3 OBLs (0 nm, 0.5 nm, 1.0 nm, and 1.5 nm) thermally oxidized at 550 °C for 3 min under atmospheric pressure of O_2.

Spectroscopy ellipsometry is utilized to quantitatively determine the thickness values of GeO_x interfacial layers when employing Al_2O_3 OBLs with different thickness values. Figure 5 shows the thickness values of GeO_x interfacial layer each as a function of oxidation time for thermal growth at 550 °C. For GeO_x thermal growth without Al_2O_3 OBL, it is demonstrated that the thickness of GeO_x interfacial layer is difficult to scale down to less than 2 nm due to its high growth velocity. By increasing the thickness value of the Al_2O_3 OBL, the growth rate of GeO_x significantly decreases. When using 1.5-nm-thick Al_2O_3 OBL, the GeO_x thickness value reaches approximately 0.5 nm for a thermal oxidation time of 10 s. The thickness value of the GeO_x interfacial layer seems to be saturated at about 1 nm, even the oxidation time is extended up to 300 s. The dramatic reduction of GeO_x thickness is significant for high-k dielectric stacks, which improves the interface quality and does not increase EOT simultaneously. It is worth pointing out that more than 2∼3 nm Al_2O_3 OBL is thick enough to prevent the oxygen from diffusing into the Ge surface, thereby entirely suppressing oxidation on Ge surface. Thus, 1.5-nm-thick Al_2O_3 OBL would be a better option for suppressing oxygen diffusion and oxidation reaction at Ge surface.

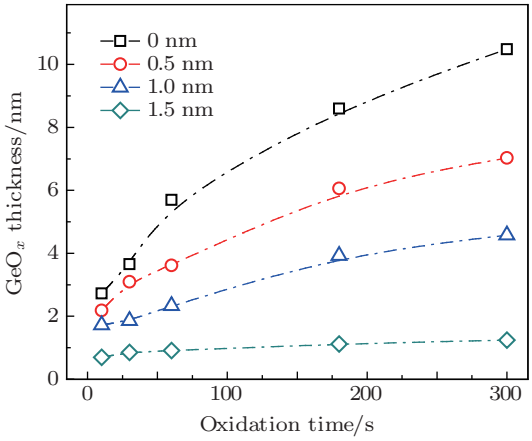


Fig. 5. (color online) Thickness values of GeO_x interfacial layer each as a function of oxidation time for thermal growth at 550 °C, when employing Al_2O_3 OBLs with four different thicknesses (0 nm, 0.5 nm, 1.0 nm, and 1.5 nm).

To further confirm the interface structure of the $Al_2O_3/GeO_x/Ge$ stack, transmission electron microscope (TEM) measurement is carried out on the MOSCAPs to determine the GeO_x thickness value in the final gate stack structure, as illustrated in Figure 6. For the 1.5-nm-thick Al_2O_3 OBL and thermal oxidation at 550 °C for 60 s, the GeO_x thickness is approximately 0.5 nm, which is consistent with our result obtained by spectroscopy ellipsometry, demonstrating the effectiveness of Al_2O_3 OBL in scaling down the thickness of GeO_x interfacial layer.

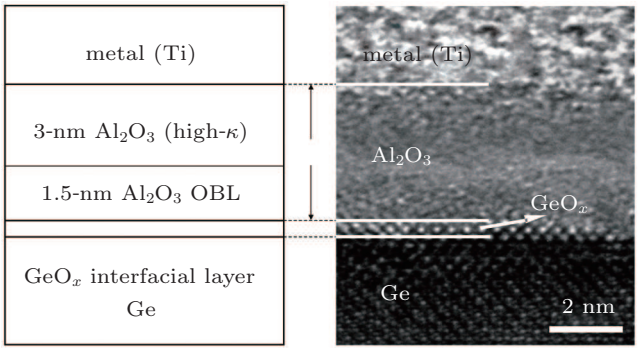


Fig. 6. TEM image of MOSCAP with the $Al_2O_3/GeO_x/Ge$ gate stack. The left panel is in one-to-one correspondence to the TEM image.

The electrical characteristics of MOSCAPs are measured to investigate the electrical quality of the scaled GeO_x interfacial layer. Figure 7(a) shows the C–V characteristics of MOSCAPs with Al_2O_3(4.5 nm)/GeO_x (0.5 nm)/Ge gate stack fabricated by thermal oxidation with 1.5-nm-thick Al_2O_3 OBL at 550 °C for 60 s and deposition of 3-nm-thick Al_2O_3 as top high-k dielectric. Well-behaved C–V curves of the MOSCAPs demonstrate less frequency dispersion at flat band voltage, which means that the remained dangling bonds at GeO_x/Ge interface are passivated by the ultrathin GeO_x interfacial layer and low-temperature oxygen annealing technique, which could further stabilize the GeO_x/Ge interface.[19] The hysteresis happens at less than 50 mV, which is determined by the bidirectional C–V measurement at 1 MHz.

The capacitance density in the accumulation region is ∼ 1.2 μF/cm^2, indicating that its EOT is 2.4 nm. The EOT value is slightly smaller than the estimation using the permittivities and thicknesses of Al_2O_3 and GeO_x layers (8.5 nm and 5.2 nm, 4.5 nm and 0.5 nm). This is attributed to the compaction of dielectrics and quality improvement during the post-deposition oxygen annealing,[18] possibly by reducing the oxygen vacancy as well as the residual organic substance in the ALD deposition process. Moreover, a low-temperature conductance method[25] is used to quantitatively extract the D_{it} at the Al_2O_3(4.5 nm)/GeO_x(0.5 nm)/Ge interface. Figure 7(b) shows the D_{it} spectrum extracted by the conductance method ($D_{it} = \sim 1 \times 10^{12}$ eV^{-1}·cm^{-2} at $E_i + 0.25$ eV) versus energy, and its comparison with the data previously reported by other groups.[26] The leakage current density of the Al_2O_3(4.5 nm)/GeO_x(0.5 nm)/Ge gate stack is suppressed to $\sim 5\times10^{-6}$ A·cm^{-2} at $V_G = V_{FB} + 1$ V. These results confirm the truth of the good effect of scaled GeO_x interfacial layer formed by our modified thermal oxidation method and post treatments.

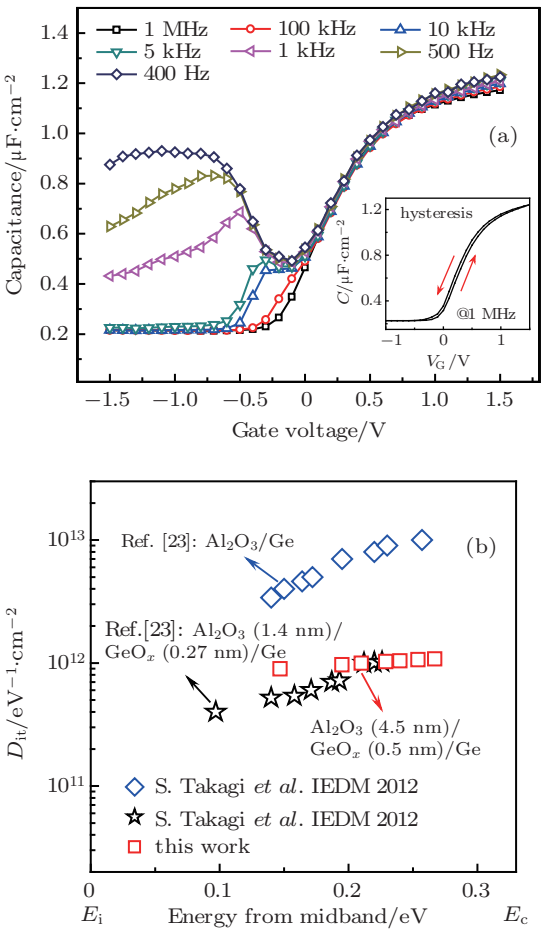


Fig. 7. (color online) (a) *C*–*V* curves of MOSCAP with Al_2O_3(4.5 nm)/GeO_x(0.5 nm)/Ge gate stack. The inset of panel (a) shows the hysteresis of the MOSCAP at 1 MHz. (b) D_{it} distribution of MOSCAP with Al_2O_3(4.5 nm)/GeO_x(0.5 nm)/Ge gate stack in this work, in comparison with the data previously reported by other group.

The Ge (100) pMOSFETs with a channel length of 6 μm are fabricated using the Al_2O_3/GeO_x/Ge gate stacks in order to further verify the influence of the MOS interface quality on the electrical properties of Ge pMOSFETs. Figure 8(a) shows the typical output characteristics of a Ge (100) p-MOSFET with a threshold voltage (V_T) of 0.15 V, using the Al_2O_3(4.5 nm)/GeO_x(0.5 nm)/Ge gate stack. The transfer characteristics of the MOSFET are shown in Fig. 8(b). The drain current on-off (I_{on}/I_{off}) ratio at room temperature is above 1×10^4. A subthreshold slope of ∼ 120 mV/dec at $V_D = -50$ mV is achieved, indicating the small D_{it} of pMOSFET. The conventional split *C*–*V* method is used to extract the hole mobility of the fabricated pMOSFET. The peak hole mobility for the Ge (100) pMOSFET with the Al_2O_3(4.5 nm)/GeO_x(0.5 nm)/Ge gate stack is above 265 cm^2/V·s.

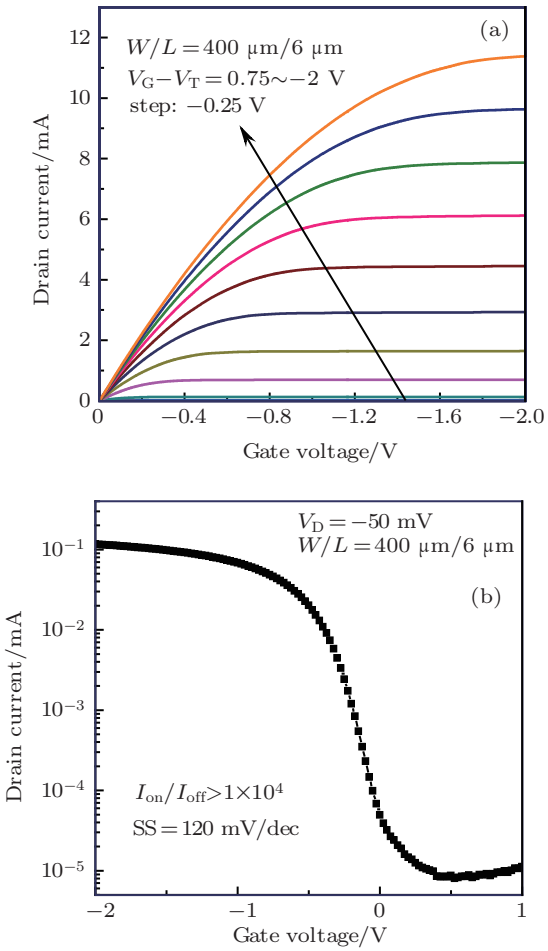


Fig. 8. (color online) (a) The output and (b) transfer characteristics of the Ge (100) pMOSFET with the Al_2O_3(4.5 nm)/GeO_x(0.5 nm)/Ge gate stack.

4. Conclusion

The modified thermal oxidation method and post treatments have been confirmed to be effective in improving qualities of the interface and gate dielectric. The thin Al_2O_3 film serves well as OBL to scale down the thickness of GeO_x interfacial layer and suppress the GeO desorption. As the thickness value of Al_2O_3 OBL increases, the thickness value of GeO_x interfacial layer would dramatically decrease. However

the thickness value of GeO_x interfacial layer has little influence on passivation effect for the Al_2O_3/Ge interface. The Ge (100) pMOSFET with the Al_2O_3/GeO_x/Ge gate stack is demonstrated with a small EOT of 2.4 nm, which exhibits excellent electrical characteristics. Also, other high-k dielectrics, such as HfO_2 and La_2O_3, can replace the second Al_2O_3 deposition layer to obtain better properties of gate stacks. The modified thermal oxidation method needs to be further improved and will provide a potential application to Ge MOS devices.

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