Single event effect in a ferroelectric-gate field-effect transistor under heavy-ion irradiation*

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The single event effect in ferroelectric-gate field-effect transistor (FeFET) under heavy ion irradiation is investigated in this paper. The simulation results show that the transient responses are much lower in a FeFET than in a conventional metal–oxide–semiconductor field-effect transistor (MOSFET) when the ion strikes the channel. The main reason is that the polarization-induced charges (the polarization direction here is away from the silicon surface) bring a negative surface potential which will affect the distribution of carriers and charge collection in different electrodes significantly. The simulation results are expected to explain that the FeFET has a relatively good immunity to single event effect.

Keywords: single event effect, heavy ion irradiation, charge collection, ferroelectric memory, FeFET

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1. Introduction

Nonvolatile memories are extensively used in modern integrated circuits. Ferroelectric memories have good application prospects in computing, aerospace, and military industry because of many advantages such as low power consumption, high reading and writing speed, high endurance, high density, anti-radiation, and non-volatility. Thus ferroelectric memories have attracted a great deal of attention and become one of the most promising and advanced nonvolatile memory technologies today.[1,2]

Ferroelectric memory can be classified into two categories, i.e., capacitor-type (1T1C or 2T2C) ferroelectric random access memory (FeRAM) and FeFET ferroelectric NOT-AND (FeNAND) flash memory. Recently, a FeFET with a metal ferroelectric insulator silicon (MFIS) structure has attracted considerable attention as promising high density and high speed nonvolatile memory due to its superior characteristics such as a single device structure, a simple process flow, and low power consumption.[3–6] Therefore, the MFIS structure FeFET from Ref. [7] is selected and simulated in this paper. As is well known, the FeRAM based on a 1T1C or 2T2C cell has a high radiation endurance,[8,9] consequently, the FeRAM could be widely used in a space environment. However, for the MFIS FeFET, the study of its irradiation effect is still not enough, so it is important and necessary to simulate and estimate the single event effect of an MFIS FeFET.

In this paper, first, the transfer characteristic and output characteristic of an MFIS FeFET are simulated, then, its single event transient response are simulated and investigated. For comparison, we also carry out the same simulation for a conventional MOSFET with the same feature size.

2. Simulation details

The two-dimensional (2D) architecture considered in the simulation and the definitions of its main geometrical parameters are presented in Fig. 1. The device structure is based on the fabricated device reported in Ref. [7]. The following parameters are considered: the channel length is 10 μm, the silicon film thickness is 10 μm, the ferroelectric film is 300 nm, and the buffer layer is 10 nm. The remanent polarization P_r is 7 μC/cm^2, coercive field is 200 kV/cm, and the dielectric constant is 100. The channel is lightly doped and the source and drain are doped at 1×10^{19} cm^{-3}. The FeFET is biased in the off-state (the gate voltage V_g is 0 V, and the polarization direction is away from the silicon surface), and the drain electrode is constantly biased at a low voltage of 1 V when we simulate

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the single event effect.

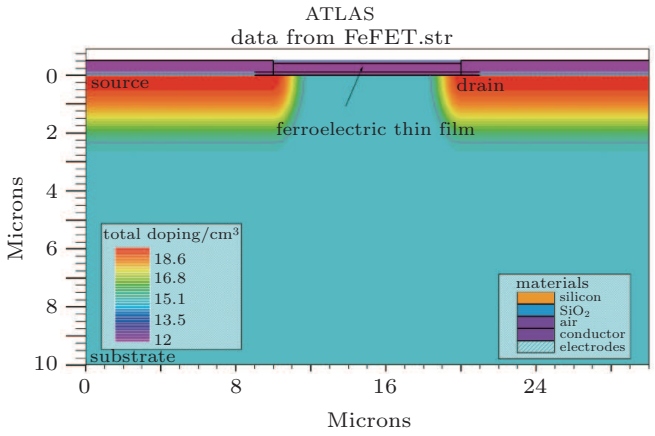


Fig. 1. (color online) 2D description of the simulated MFIS FeFET structure considered in this work.

In order to clearly show the transient response in the channel and the worst case in terms of single event transient, a strike in the middle of the gate is considered in the simulation.[10] The collected charge is given by the integration of the drain current over the transient duration.

All the simulations are performed with an ATLAS device simulator from Silvaco International Inc. The set of physical models used in the simulation includes Shockley–Read–Hall and Auger recombination as well as the Lombardi's mobility model accounting for doping, parallel and transverse electric field mobility dependencies. The ion strike is simulated using the ATLAS single event upset module.[11] Moreover, the Selberherr model is used for the impact ionization whose parameters have been experimentally verified. The electron–hole pair columns created by the ion are modeled using a carrier-generation function which has a Gaussian radial distribution with a radius of 200 nm. The physical model of a FeFET is cited from Ref. [12] and four parameters are considered: saturated polarization P_s, remanent polarization P_r, coercive field E_c, and dielectric constant.

3. Static characteristics

Figure 2 shows the typical transfer characteristic (drain current I_d versus gate voltage V_{gs}) of the simulated MFIS FeFET. Here, an applied drain voltage V_{ds} is fixed at 1 V, while the gate voltage V_{gs} here is swept from +4 V to −4 V and then returned to +4 V. The I_d–V_{gs} characteristic shows a counter-clockwise hysteresis loop due to the polarization reversal in the ferroelectric film. Figure 2 clearly shows a memory window width of around 0.9 V and a drain current on/off ratio of as high as 10^6. The derived subthreshold slope is about 133 mV/dec, indicating a good device performance on the leakage current and switching characteristics.[13]

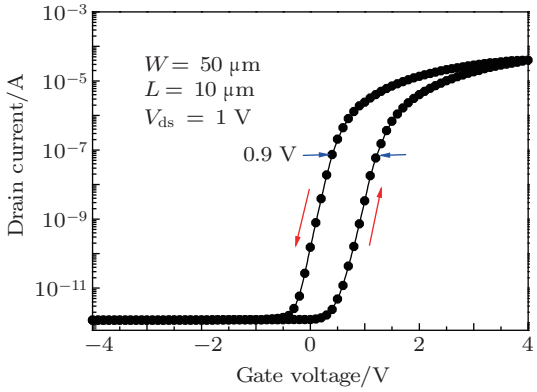


Fig. 2. (color online) Drain current characteristic as a function of gate voltage of the MFIS FeFET.

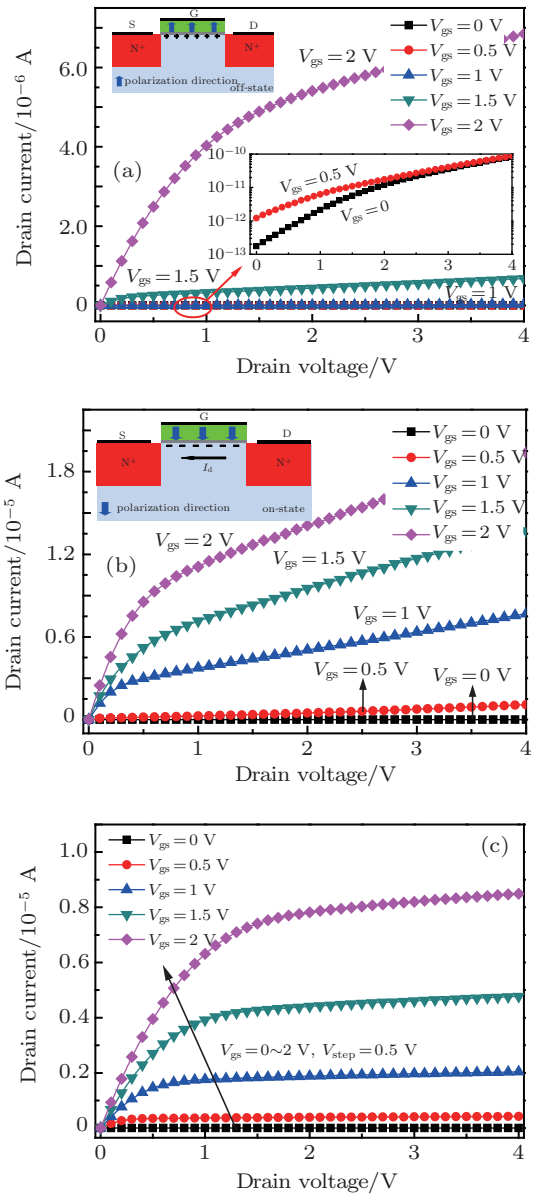


Fig. 3. (color online) Drain current characteristics each as a function of drain voltage for the MFIS FeFET [(a), (b)] and the MOSFET (c). Panel (a) shows the output characteristics when the polarization direction is away from the silicon surface, and panel (b) shows the output characteristics when the polarization direction points to the silicon surface.

Figure 3 shows the output characteristic (drain current I_d versus drain voltage V_{ds}) of the MFIS FET. V_{ds} is swept from 0 to 4 V, and V_{gs} is changed from 0 to 2 V in steps of 0.5 V. Specifically, Fig. 3(a) shows the output characteristics when the polarization direction is away from the silicon surface, and Fig. 3(b) shows the output characteristics when the polarization direction points to the silicon surface. For comparison, the output characteristic of the MOSFET is simulated and shown in Fig. 3(c).

4. Transient simulation results

4.1. Drain current and collected charge

The drain current transients and charge collection produced by the ion strike are illustrated in Fig. 4 with different ion linear energy transfers (LETs). We can clearly see that the drain current transients center in about 1 ns, the possible reason is that diffusion current is the main component of the drain current transient, the drift current is small because the long channel brings a small drift electric field. Figure 4 also shows that the drain current transient peaks and the collected charge increase with the increase of LET, and the peak value of drain current transient in the FeFET is much lower than that in the conventional MOSFET. From this we can infer that the bipolar amplification in the MOSFET is higher than that in the FeFET.

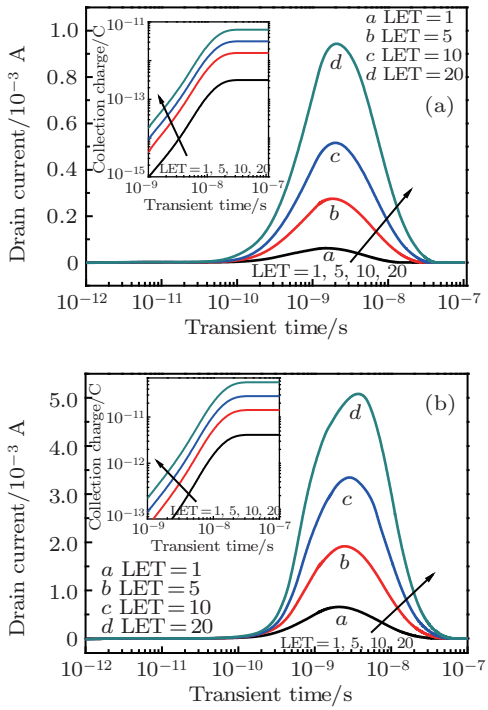


Fig. 4. (color online) Time variations of the drain current transients and charge collection for the MFIS FeFET (a) and the MOSFET (b).

In order to investigate the bipolar amplification effect clearly, the devices (MOSFET and MFIS FeFET) without source junction are simulated in the same conditions. As shown in Fig. 5, we can see that the drain current transient and drain charge collection decrease significantly when the source junction is removed, which indicates the existence of bipolar amplification effect in the simulated devices. The negative current in source electrode after 1 ns indicates that the source injects electrons into the channel due to the fact that the residual holes left in the substrate raise the substrate potential and lower the source junction potential barrier, these injected electrons can be amplified and collected by the drain electrode.[14,15] For a better view of the current in different electrodes, the substrate current is defined as having a negative value here. When the source junction is removed, the substrate current shows a considerable increase. The main reason is that part of the electrons which should be collected by source electrode are collected by the substrate electrode. Comparing Fig. 5(a) with Fig. 5(b), we can find that the peak value of drain current transient in the FeFET is much lower than that in the conventional MOSFET, no matter whether the source junction is removed, this is mainly due to the fact that the polarization-induced charges bring a negative surface potential which makes more electrons transfer to the substrate and collected by the substrate electrode.

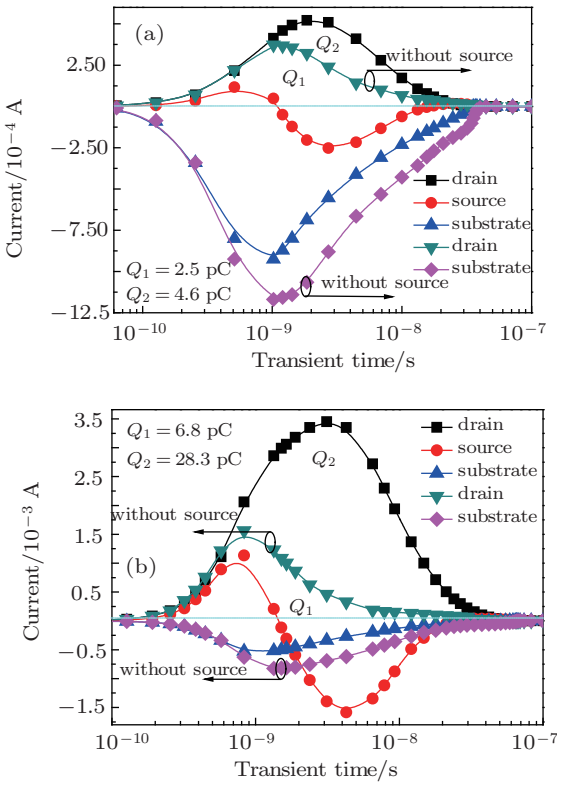


Fig. 5. (color online) Different current transients in FeFET (a) and in MOSFET (b). The LET is 10 MeV·cm^2/mg.

4.2. Potential and carrier density

The time evolutions of the electrostatic potential in the silicon film before and after the ion has struck the middle of the channel are shown in Fig. 6. The electrostatic potential here is along a horizontal cutline through the silicon surface (10 nm deep). The LET here is 10 MeV·cm^2/mg. We can see that

the polarization-induced charges bring a negative surface potential (the polarization direction here is away from the silicon surface) before the ion has struck the channel. The negative surface potential causes an accumulation of majority carriers (holes) near the semiconductor surface, which will contribute to preventing the electrons generated by the ion strike from diffusing. Figure 6 also indicates that the channel potential is raised to a highest value at 10 ns, and the potential in FeFET is lower than that in the conventional MOSFET.

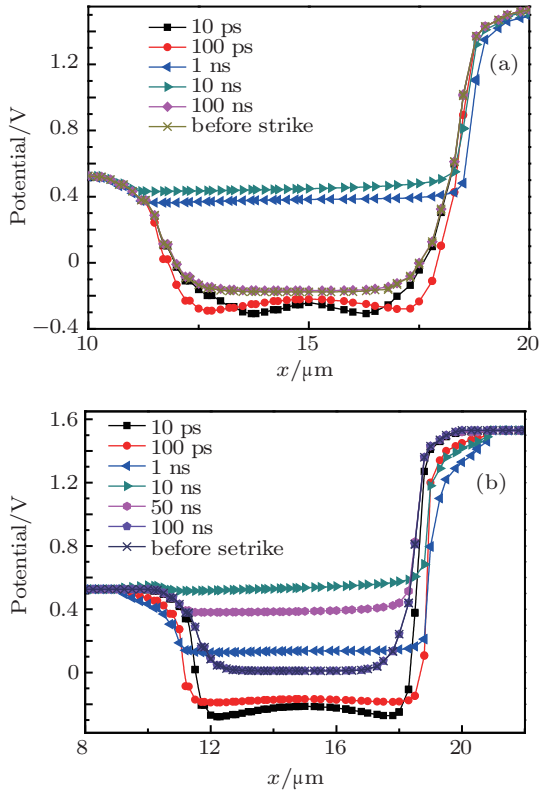


Fig. 6. (color online) Time evolutions of electrostatic potential in the channel before and after the ion strikes, (a) FeFET and (b) MOSFET.

For a lightly doped p-type silicon, the diffusion coefficient of electrons is about three times as large as the diffusion coefficient of holes. As shown in Fig. 6, within the first few tens of picoseconds after the ion impact, the number of electrons along a horizontal cutline through the silicon surface is greater than the number of holes due to their different diffusion coefficients. The extra electrons could lower the surface potential at 10 ps and 100 ps. Then, the electrons are collected by the electrodes, and the residual holes left in the substrate raise the surface potential to a positive value in the following few nanoseconds (at 1 ns and 10 ns). The similar results can be found in Ref. [16].

Figure 7(a) shows the electron densities in the channel of FeFET before and after the ion has struck the channel. Here the LET is 10 MeV·cm^2/mg. We can see that the electron–hole pairs generated by the ion impact ionization make the channel electron concentration significantly increase. The high electron density may provide a conductive channel for the FeFET just like the inversion layer, which will make the device turn on transiently. For a comparison, the electron density in MOSFET is shown in Fig. 7(b). Also, the channel electron concentration in FeFET is lower than that in the conventional MOSFET when the ion strikes the channel.

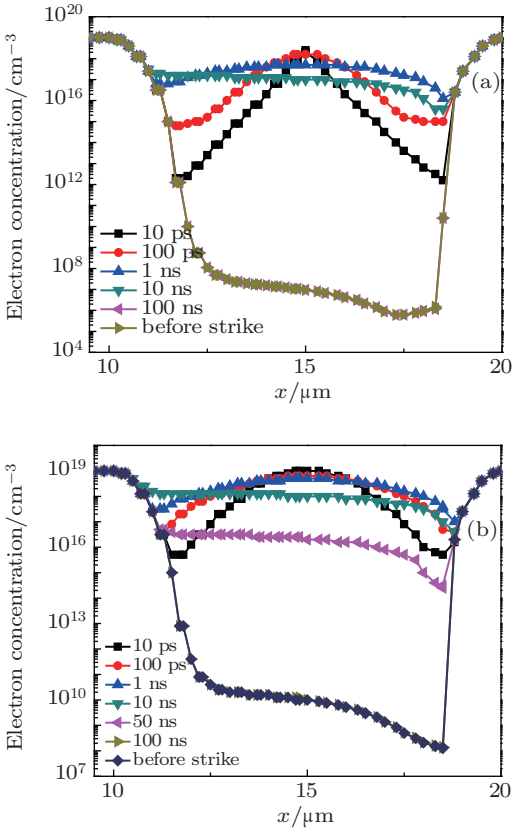


Fig. 7. (color online) Time evolutions of electron density in the channel before and after the ion strikes, (a) FeFET and (b) MOSFET.

4.3. Influence of strike location

The impact of the ion track location on the single event transient is studied in this part. From Fig. 8 we can see that different strike locations bring different transient responses. When the strike location (from position 1 to position 3) is close to the drain, the drain current peak is higher and more charges are collected. The reason is that the closer to the drain, the shorter electron drift-diffusion distance is, which contributes to collecting more charges. When the ion strikes the drain junction (position 4), the drain current transients reach a maximum value, and the peak value of drain current transient in the FeFET is almost equal to that in the conventional MOSFET. The reason is that the funnel-aided drift current is the main component of drain current transients. From the simulation results we can say that when the ion strikes the channel, the FeFET shows a relatively good immunity to the single event effect compared with the conventional MOSFET, this is mainly due to the fact that the channel potential is under the control of ferroelectric thin film, which will affect the distribution of carriers and charge collection in different electrodes significantly.

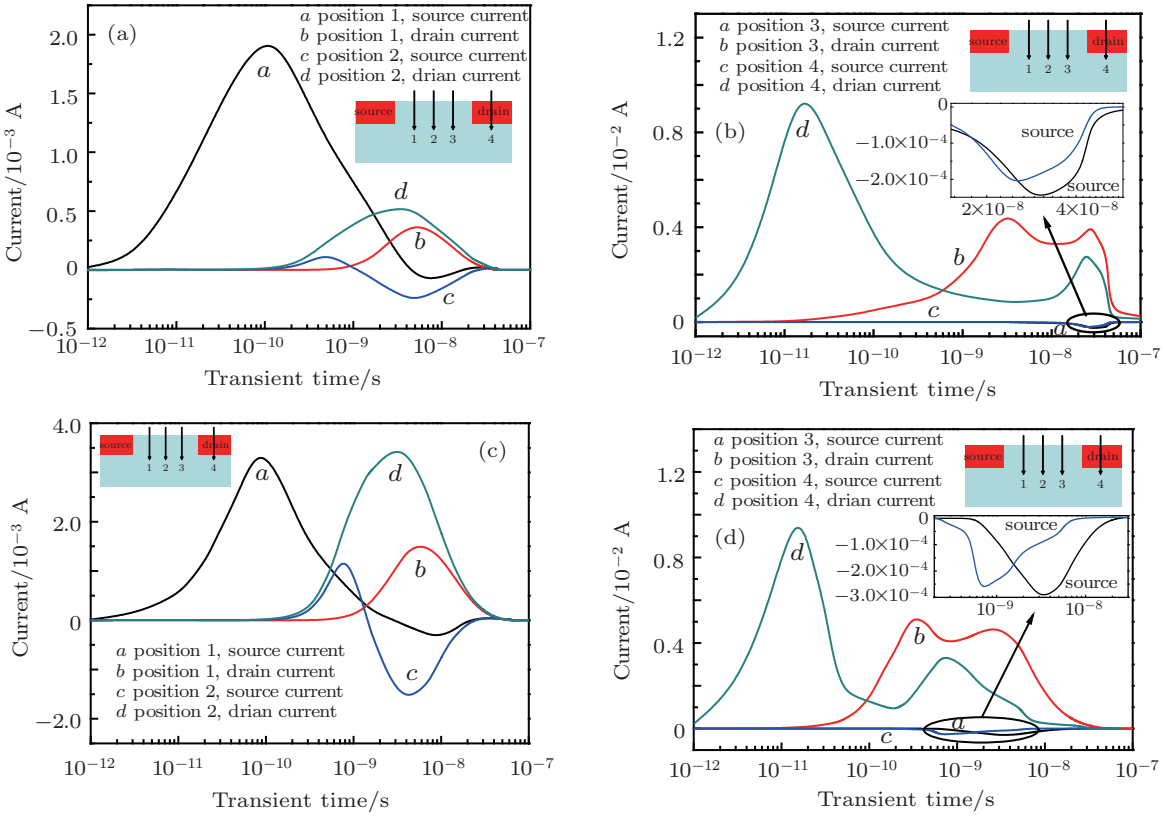


Fig. 8. (color online) Time variations of current transients at different strike positions in FeFET ((a), (b)) and in MOSFET ((c), (d)). The LET is 10 MeV·cm^2/mg.

5. Conclusion

In this paper we present the single event transient responses of the MFIS FeFET. The simulation results show that the charge collection and drain current transient in a conventional MOSFET are much larger than those in an MFIS FeFET when the ion strikes the channel. The main reason is that the polarization-induced charges bring a negative surface potential which will affect the distribution of carriers and charge collection in different electrodes significantly. The simulation results also show that the transient responses of channel electrical characteristics (channel potential and channel electron concentration) in the MFIS FeFET are lower than those in a conventional MOSFET. This illustrates that the MFIS FeFET has a good off-state characteristic, which is very important for a storage device.

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