Low on-resistance high-voltage lateral double-diffused metal oxide semiconductor with a buried improved super-junction layer*

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A novel low specific on-resistance ($R_{on,sp}$) lateral double-diffused metal oxide semiconductor (LDMOS) with a buried improved super-junction (BISJ) layer is proposed. A super-junction layer is buried in the drift region and the P pillar is split into two parts with different doping concentrations. Firstly, the buried super-junction layer causes the multiple-direction assisted depletion effect. The drift region doping concentration of the BISJ LDMOS is therefore much higher than that of the conventional LDMOS. Secondly, the buried super-junction layer provides a bulk low on-resistance path. Both of them reduce $R_{on,sp}$ greatly. Thirdly, the electric field modulation effect of the new electric field peak introduced by the step doped P pillar improves the breakdown voltage (BV). The BISJ LDMOS exhibits a BV of 300 V and $R_{on,sp}$ of 8.08 mΩ·cm^2 which increases BV by 35% and reduces $R_{on,sp}$ by 60% compared with those of a conventional LDMOS with a drift length of 15 μm, respectively.

Keywords: multiple-direction assisted depletion effect, breakdown voltage (BV), electric field modulation, lateral double-diffusion MOSFET (LDMOS)

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1. Introduction

The lateral double-diffusion MOSFET (LDMOS) acts as an important component in power electronics applications for its facility integration. One of the main issues is the trade-off between breakdown voltage (BV) capability and specific on-resistance ($R_{on,sp}$). Some new structures have been reported.[1–4] The superjunction (SJ) concept[5] used in an LDMOS[6] further improves the trade-off between the BV and $R_{on,sp}$. Based on an SJ concept, several new structures have been developed.[7–12]

In this paper, we propose a novel LDMOS with a buried improved superjunction (BISJ) layer. The BISJ layer not only enhances the reduced surface field (RESURF) effect,[13] but also provides a bulk low on-resistance path. Moreover, the new electric field peak caused by the BISJ layer modulates the surface electric field. As a result, the BISJ layer reduces the $R_{on,sp}$ and increases the BV in the proposed device.

2. Device structure and mechanism

The proposed BISJ LDMOS and its physical mechanism are illustrated in Fig. 1. An SJ layer is imbedded in a drift region and the P pillar is split into two parts with doping concentrations N_p and N_m, respectively. The buried SJ layer which is surrounded by the N$^-$ drift region causes multiple-directional depletion not only along the z direction but also along the y direction. The depleting directions and the charges balance between the ionized donors and acceptors are shown by arrows in Figs. 1(b) and 1(c). Consequently, the drift

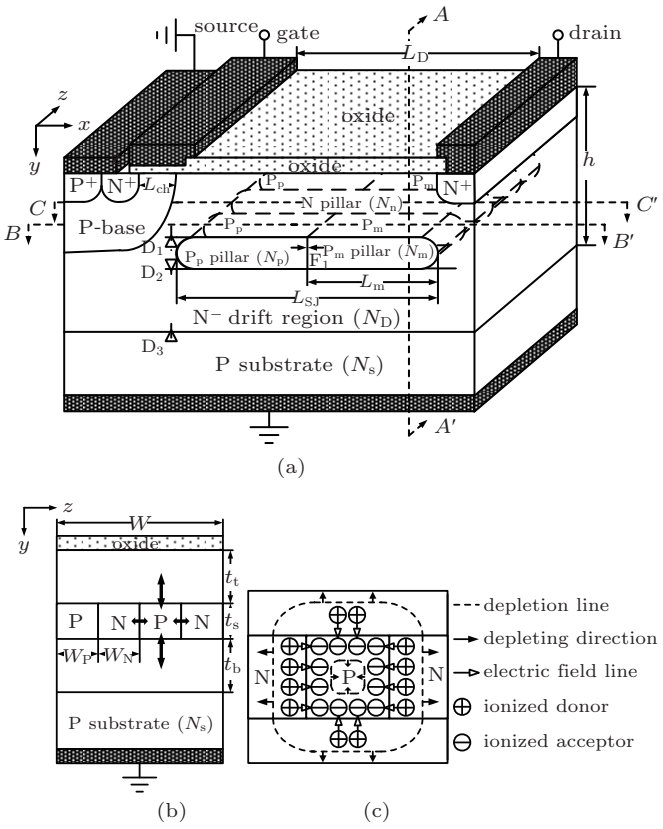


Fig. 1. (a) Structure of the BISJ LDMOS; (b) cross sections along the AA' plane; (c) schematic of charge balance.

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region implantation dose in the BISJ LDMOS is much higher than that in the conventional LDMOS and the implantation dose of the P pillar is also much higher than that of the N pillar in the SJ layer. The highly doped SJ layer also provides a bulk low on-resistance path. Therefore, the buried SJ layer reduces $R_{on,sp}$ significantly. Furthermore, the new electric field peak appearing at P_p-pillar/P_m-pillar interface (i.e., interface F_1 in Fig. 1(a)) modulates the surface electric field, which causes a more uniform distribution of the surface electric field. It results in a high BV. t_s and h are the thickness of the BISJ layer and the N^- drift region. t_t is the buried SJ layer depth. W_N and W_P are the widths of the N pillar and the P pillar, respectively. L_{ch}, L_D, and L_{SJ} are the length of the channel, the drift region, and the buried SJ layer, respectively. In this paper, $W_N = W_P$ = 2 μm, h = 5 μm, $N_s = 2 \times 10^{14}$ cm^{-3}, $N_n = 1 \times 10^{16}$ cm^{-3}, $L_{ch} = 3$ μm, and $t_s = 1$ μm are used, and $L_D = 15$ μm is used in Figs. 2–7.

3. Results and discussion

The three-dimensional (3D) device simulations are performed by Sentaurus.[14] Figure 2 shows the comparison of the equipotential contour between the BISJ LDMOS and the conventional LDMOS at the drain voltage $V_{DS} = 20$ V. Arrow heads show depleting directions. It is clear that the multiple-directional depletion is caused in the BISJ LDMOS.

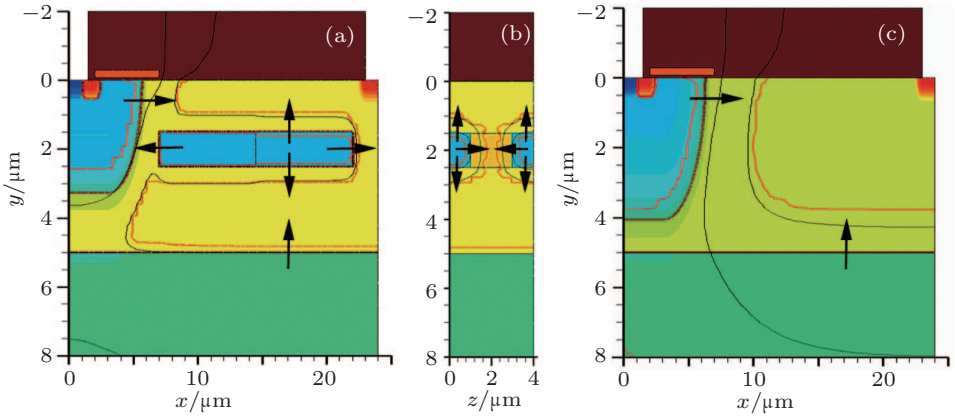


Fig. 2. (color online) Equipotential contours for (a) BISJ LDMOS along the BB' plane, (b) BISJ LDMOS along the AA' plane, and (c) the conventional LDMOS at $V_{DS} = 20$ V (10 V/contour. BISJ LDMOS: $t_t = 1.5$ μm, L_m = 7.5 μm, $N_m = 3.5 \times 10^{16}$ cm^{-3}, $N_p = 6.5 \times 10^{16}$ cm^{-3}, $N_D = 6.8 \times 10^{15}$ cm^{-3}, $L_{SJ} = L_D$; conventional LDMOS: $N_D = 1.6 \times 10^{15}$ cm^{-3}).

Figure 3 shows the 3D equipotential contours at breakdown for the kind of devices above. It is clear that the equipotential contours of the BISJ LDMOS are evenly spaced and the depletion area is further extended into the substrate in comparison with those of the conventional LDMOS. The BV of the BISJ LDMOS reaches 300 V, which increases 35% compared with the BV of 220 V for the conventional LDMOS.

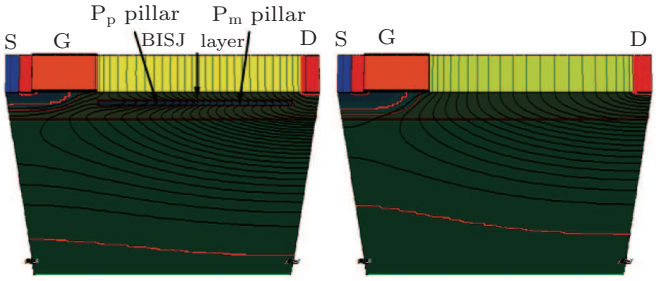


Fig. 3. (color online) The 3D equipotential contours for (a) BISJ LDMOS (300 V) and (b) the conventional LDMOS (220 V) (10 V/contour). The device structure parameters are the same as those in Fig. 2.

In Fig. 4(a), the lateral electric field profiles are compared. There is another electric field peak P_K at F_1 interface in the P pillar due to the variation in doping concentration. This new electric field P_K makes the lateral electric field of the BISJ LDMOS in the middle of the drift region much higher than that of the conventional LDMOS. Figure 4(b) shows vertical electric field distributions and the charge densities. For the BISJ LDMOS, firstly, the high electric field strength E_P is introduced by the high doping concentration of the P pillar in the BISJ layer; secondly, the electric field peak at D_3 junction increases greatly ($E_1 > E_2$). Thus the drift-region/substrate junction sustains a higher blocking voltage. It is also evident that the concentrations of the drift region in the BISJ LDMOS and the P pillar are much higher than those of the drift region in the conventional LDMOS and the N pillar respectively.

Figure 5 shows the current flow lines for the BISJ LDMOS and the conventional LDMOS in the on-state. It shows that the high doping N pillars in the BISJ offer bulk low on-resistance paths. These paths coupled with the increased doping concentration of drift region reduce $R_{on,sp}$ significantly. The BISJ LDMOS exhibits an $R_{on,sp}$ of 8.08 mΩ·cm^2 in comparison with 20.5 mΩ·cm^2 for the conventional LDMOS at the same drift length, which decreases by 60%.

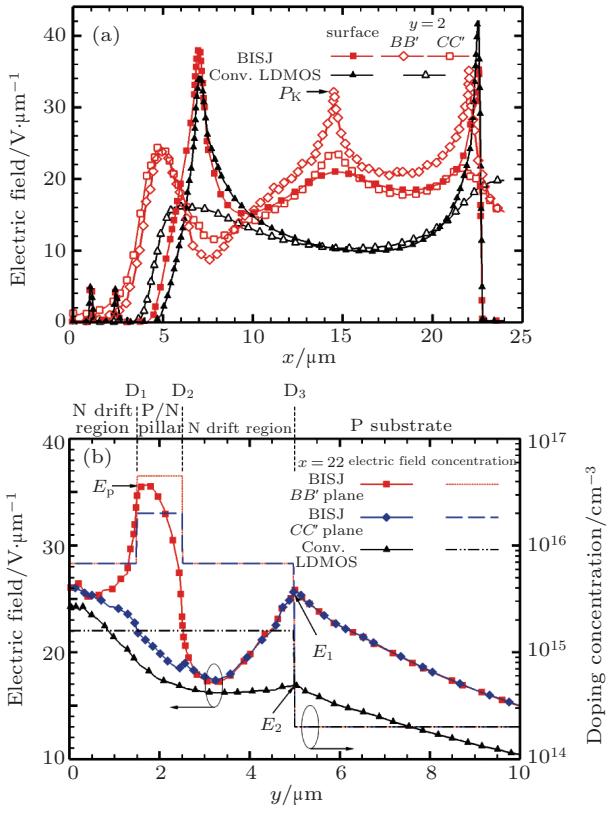


Fig. 4. (color online) (a) Lateral electronic field distributions, (b) vertical electronic field distributions and the charge density around the drain ($x = 22$ μm) for the BISJ LDMOS and the conventional LDMOS at breakdown (with the same structure parameters as those in Fig. 2.

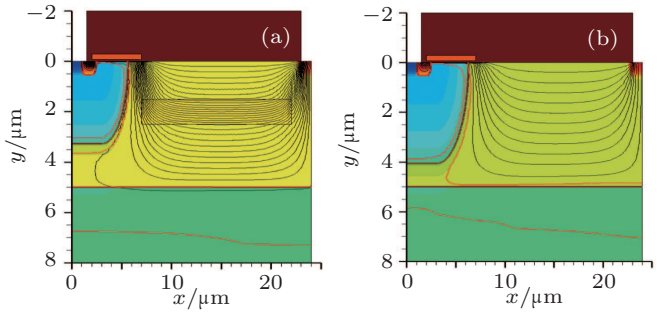


Fig. 5. (color online) Current flow line contours for (a) the BISJ LDMOS along the CC' plane and (b) the conventional LDMOS (the gate oxide thickness t_{ox} is 800 Å, $V_{GS} = 12$ V, and the device structure parameters are the same as those in Fig. 2. Under the unit thickness (i.e., $z = 1$ μm), each current line represents a current value of 6×10^{-7} A·μm^{-1}/contour.

Figure 6 shows the dependences of $R_{on,sp}$ and doping concentration of the drift region on L_{SJ} for the BISJ LDMOS respectively. With the decrease of L_{SJ}, the multiple-directional depletion effect is weakened and the doping concentration of the drift region is reduced. Meanwhile, the bulk low on-resistance paths become shorter. The $R_{on,sp}$ is therefore increased. However, the doping concentration of the drift region in the BISJ LDMOS is also higher than that of drift region in the conventional LDMOS and the bulk low on-resistance paths still exist when $L_{SJ} < L_D$. Consequently, the $R_{on,sp}$ value of the BISJ LDMOS is smaller than that of the conventional LDMOS. Because the minimum $R_{on,sp}$ for the BISJ LDMOS is obtained at $L_{SJ} = L_D$, $L_{SJ} = L_D$ is used in the discussion below.

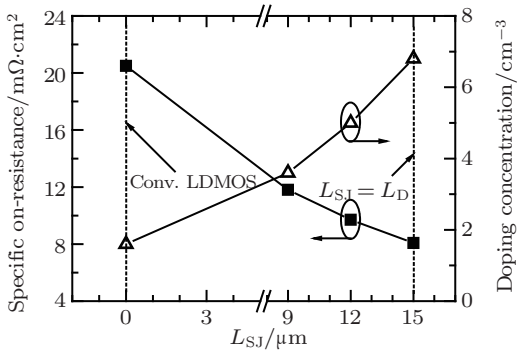


Fig. 6. $R_{on,sp}$ and N_D versus L_{SJ} for the BISJ LDMOS with t_t = 1.5 μm, $L_m = 0.5L_{SJ}$, $N_m = 3.5\times10^{16}$ cm^{-3}, and $N_p = 6.5\times10^{16}$ cm^{-3}.

The influences of L_m and the variation ΔN in the doping concentration of P pillar (i.e., $\Delta N = N_p - N_m$) on BV at different values of t_t for the BISJ LDMOS are shown in Figs. 7(a) and 6(b). In Fig. 6(a), the maximum BV for the BISJ LDMOS is obtained at $L_m = 0.5L_D$. Hence, in the following discussion, L_m is fixed at $0.5L_D$. In Fig. 7(b), the average doping concentration of P pillar $\bar{N} = (N_p + N_m)/2$ is kept unchanged ($\bar{N} = 5\times10^{16}$ cm^{-3} in this case) to ensure the charge balance. A well-designed ΔN makes the modulation effect obvious but prevents the premature breakdown at F_1 interface. It is found that the optimal range of ΔN is 2×10^{16} cm$^{-3} \le \Delta N \le 3\times10^{16}$ cm^{-3}. Due to the modulation effect of the electric field peak at F_1 interface, the maximum BV of the BISJ LDMOS is 35% higher than that of the device with uniform doping P pillar ($\Delta N = 0$). Figure 7(c) shows the dependences of $R_{on,sp}$ and BV on t_t. The reduction in t_t is conductive to the electric field modulation effect. However, if t_t is too low, the D_2 junction breaks down prematurely. To obtain the tradeoff between BV and $R_{on,sp}$, the optimal range is $1 \le t_t \le 2$ μm. In Fig. 7(d), the values of BV and $R_{on,sp}$ for the BISJ LDMOS and the conventional LDMOS at different N_D values are compared. Due to the multiple-directional depletion effect, the optimum N_D value of the BISJ LDMOS is about four times as great as that of the conventional LDMOS. The $R_{on,sp}$ of the BISJ LDMOS is decreased by 60% in comparison with that of the conventional LDMOS.

For the BISJ LDMOS, the fabrication of the buried SJ layer is a key process. The main steps of one feasible fabrication method are given as follows (see Fig. 8): when high temperature processes in field oxide formation, the device is masked to prevent the thick oxide from forming the above N^- drift region. Then a uniform, thin gate oxide is employed, which has a typical thickness of 200–1000 Å. An advantage of using such a thin oxide is that it reduces the required energy for the ions to be implanted to form the buried SJ layer; for phosphorus ions and boron ions to be implanted to form the buried SJ layer; and finally to form the P^+ contact the N^+ source/drain regions and electrodes.

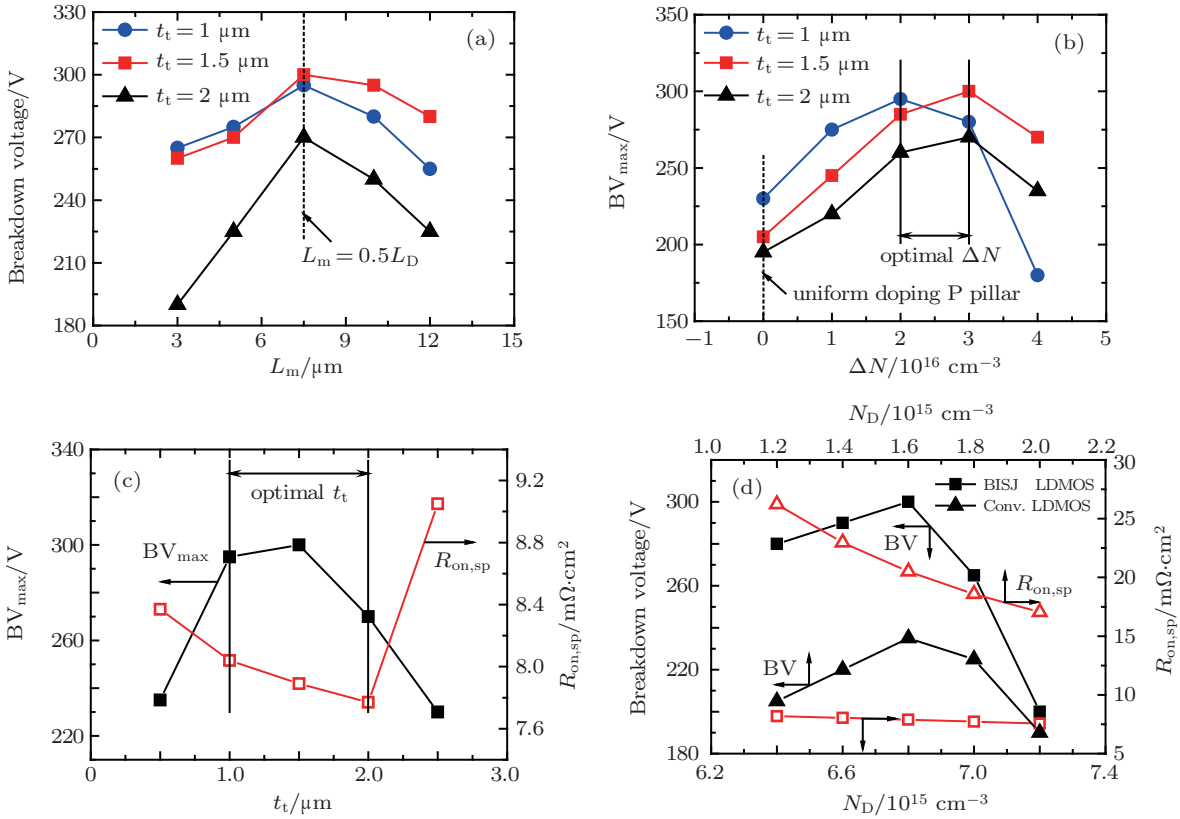


Fig. 7. (color online) BVs and $R_{on,sp}$ versus (a) L_m ($N_m = 3.5 \times 10^{16}$ cm^{-3}, $N_p = 6.5 \times 10^{16}$ cm^{-3}, $N_D = 6.8 \times 10^{15}$ cm^{-3}), (b) ΔN ($L_m = 7.5$ μm, $N_D = 6.8 \times 10^{15}$ cm^{-3}), (c) t_t ($L_m = 7.5$ μm, $N_m = 3.5 \times 10^{16}$ cm^{-3}, $N_p = 6.5 \times 10^{16}$ cm^{-3}, $N_D = 6.8 \times 10^{15}$ cm^{-3}), and (d) N_D ($L_m = 7.5$ μm, $t_t = 1.5$ μm, $N_m = 3.5 \times 10^{16}$ cm^{-3}, $N_p = 6.5 \times 10^{16}$ cm^{-3}).

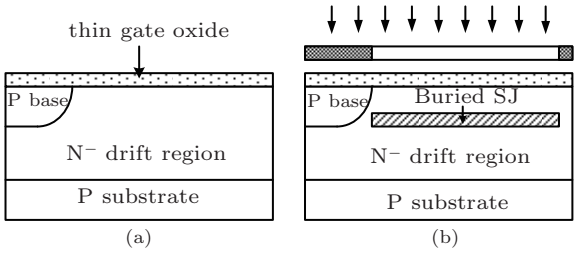


Fig. 8. Process flows of fabrication of the buried SJ layer. (a) Grow gate oxide. (b) Implant ions to form the buried SJ layer.

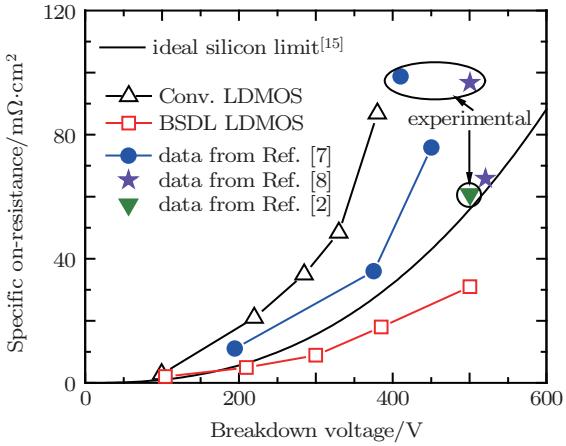


Fig. 9. (color online) Plots of $R_{on,sp}$ versus BV for several bulk silicon n-channel LDMOS.

Figure 9 shows the plots of $R_{on,sp}$ versus BV for the BISJ LDMOS and several bulk Si devices with prior technologies in Refs. [2], [7], and [8]. The reduction in $R_{on,sp}$ of the BISJ LDMOS is limited in BV $\leq$ 100 V because the $R_{on,sp}$ is dominated by the channel resistance in the low voltage device with short drift length. As BV increases, the long drift region resistance becomes a main part of the $R_{on,sp}$. The performance of the BISJ LDMOS therefore is superior to those of the other bulk Si devices which break the silicon limit[15] in BV $\geq$ 200 V. There are three causes: the multiple-directional depletion effect, a bulk low on-resistance path, and the electric field modulation effect caused by the electric field peak appearing at F_1 interface.

4. Conclusion

A new LDMOS with a buried improved super-junction layer is presented and investigated by simulation. The BISJ layer causes the multiple-directional depletion effect and offers a bulk low on-resistance path, reducing the $R_{on,sp}$. The new electric field peak generated by the BISJ layer with the step doped P pillar increases BV. Compared with a conventional LDMOS, the BISJ LDMOS increases BV from 220 to 300 V and reduces $R_{on,sp}$ by 60% at the same drift length.

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