A two-dimensional analytical subthreshold behavior model for junctionless dual-material cylindrical surrounding-gate MOSFETs*

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A two-dimensional analytical subthreshold behavior model for junctionless dual-material cylindrical surrounding-gate (JLDMCSG) metal-oxide-semiconductor field-effect transistors (MOSFETs) is proposed. It is derived by solving the two-dimensional Poisson's equation in two continuous cylindrical regions with any simplifying assumption. Using this analytical model, the subthreshold characteristics of JLDMCSG MOSFETs are investigated in terms of channel electrostatic potential, horizontal electric field, and subthreshold current. Compared to junctionless single-material cylindrical surrounding-gate MOSFETs, JLDMCSG MOSFETs can effectively suppress short-channel effects and simultaneously improve carrier transport efficiency. It is found that the subthreshold current of JLDMCSG MOSFETs can be significantly reduced by adopting both a thin oxide and thin silicon channel. The accuracy of the analytical model is verified by its good agreement with the three-dimensional numerical simulator ISE TCAD.

Keywords: surrounding-gate MOSFET, dual-material gate, junctionless transistor, analytical model

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1. Introduction

Due to the ideal symmetry structure and excellent gate control ability, cylindrical surrounding-gate (CSG) metal-oxide-semiconductor field-effect transistors (MOSFETs) are regarded as the most promising devices for extending the scaling limit of CMOS technology.[1–4] However, the formation of the ultra-sharp source/drain junction of CSG MOSFETs still imposes several challenges on the doping techniques and thermal budget.[5,6] In order to overcome these challenges, junctionless cylindrical surrounding-gate (JLCSG) MOSFETs have been proposed,[7] and their superior characteristics have been demonstrated by experiments and analytical models.[8–10] The doping concentration of JLCSG MOSFETs is constant through the source, channel, and drain regions. Therefore, they demand simpler fabrication processes than conventional CSG MOSFETs. Nevertheless, the high doping concentration in the channel reduces carrier mobility, leading to transconductance degradation of JLCSG MOSFETs.[11,12] For the purpose of improving the carrier transport efficiency and transconductance of JLCSG MOSFETs, a new structure, called a junctionless dual-material cylindrical surrounding-gate (JLDMCSG) MOSFET, has been proposed and its performance investigated by numerical simulations.[13] It has been demonstrated that JLDMCSG MOSFETs have superior short-channel performance and excellent subthreshold current characteristics. In order to better exploit the scaling potential of JLDMCSG MOSFETs, it is necessary to develop an accurate subthreshold behavior model for short-channel JLDMCSG MOSFETs. In addition, physical-based analytical models for JLDMCSG MOSFETs are also needed for fast circuit simulation. Based on solving the one-dimensional (1D) Poisson's equation, several analytical models for long-channel JLCSG MOSFETs have been proposed.[4,14–17] However, these models cannot be used to predict the short-channel performance of JLDMCSG MOSFETs. In our previous work,[18] according to the parabolic potential approximation (PPA), a quasi-two-dimensional (quasi-2D) analytical threshold voltage model for short-channel JLDMCSG MOSFETs was developed. PPA assumes a parabolic potential distribution in the radial direction, leading to errors when the thickness of the silicon is much larger than that of the oxide.[19] Besides, a quasi-2D analytical model cannot offer full 2D electrostatic potential distribution of the entire channel region, and thus we will be unable to obtain a subthreshold current model through the current continuity equation.[20] In this paper, a full 2D analytical subthreshold behavior model for JLDMCSG MOSFETs is presented by exactly solving the 2D Poisson's equation in two continuous cylindrical regions. This model can be used to analyze the short-channel performance and subthreshold behavior of JLDMCSG MOSFETs. By using this model, the effects of varying the device parameters (such as the gate oxide thickness and the radius of the silicon channel) on the electrostatic potential and subthreshold current can be easily investigated. The analytical model is verified by comparison with the simulation results obtained from the three-dimensional (3D) numerical device simulator ISE TCAD.

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2. Model derivation

A schematic cross-sectional view of a JLDMCSG MOSFET is shown in Fig. 1. Considering the gate structure, the channel can be divided into two regions. The lengths of the two regions are L_1 and L_2, respectively. Owing to the symmetry of the structure, the electrostatic potential and the electric field have no angular variation in the plane of the radial direction, hence a 2D analysis is sufficient (only the channel radius direction r and channel length direction z are employed). For simplicity, the source/drain region is assumed to have zero thickness and the source/drain contact is located along the left/right side of the heavily doped silicon channel.

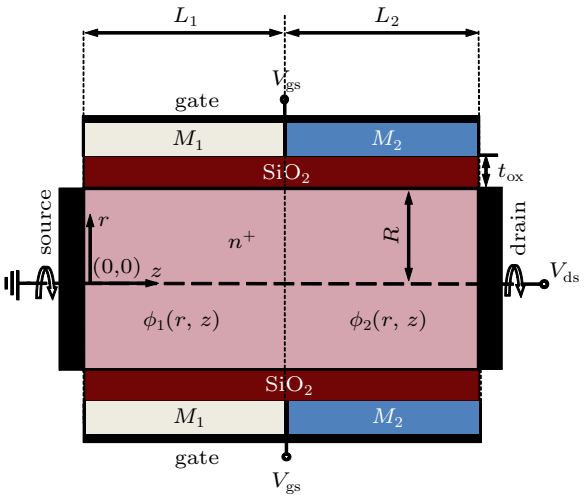


Fig. 1. (color online) A schematic cross-section view of a JLDMCSG MOSFET.

2.1. Potential model

The electrostatic potential distribution in the silicon channel can be derived by solving Poisson's equations in two continuous regions. Assuming that the influence of charge carriers and fixed charges on the electrostatics of the channel can be neglected, the silicon channel is fully depleted under subthreshold conditions. Then Poisson's equation in two regions of the channel can be written as

$$\frac{1}{r}\frac{\partial}{\partial r}\left[r\frac{\partial}{\partial r}\phi_1(r,z)\right]+\frac{\partial^2}{\partial z^2}\phi_1(r,z)=-\frac{qN_{\rm D}}{\varepsilon_{\rm si}},\quad 0\le z\le L_1,\ \ 0\le r\le R, \tag{1}$$

$$\frac{1}{r}\frac{\partial}{\partial r}\left[r\frac{\partial}{\partial r}\phi_2(r,z)\right]+\frac{\partial^2}{\partial z^2}\phi_2(r,z)=-\frac{qN_{\rm D}}{\varepsilon_{\rm si}},\quad L_1\le z\le L,\ \ 0\le r\le R, \tag{2}$$

where q is the electron charge, $N_{\rm D}$ is the donor concentration in the channel, $\varepsilon_{\rm si}$ is the dielectric constant of the silicon channel, and $L=L_1+L_2$ is the total length of the channel. Using the superposition technique, the electrostatic potential in each channel region can be expressed as

$$\phi_j(r,z)=V_j(r,z)+W_j(r),\quad j=1,2, \tag{3}$$

where $W_j(r)$ is the 1D solution to Poisson's equation

$$\frac{\partial^2}{\partial r^2}W_j(r)+\frac{1}{r}\frac{\partial}{\partial r}W_j(r)=-\frac{qN_{\rm D}}{\varepsilon_{\rm si}},\quad j=1,2, \tag{4}$$

and $V_j(r,z)$ is the 2D solution to the homogenous Laplace equation

$$\frac{\partial^2}{\partial r^2}V_j(r,z)+\frac{1}{r}\frac{\partial}{\partial r}V_j(r,z)+\frac{\partial^2}{\partial z^2}V_j(r,z)=0,\quad j=1,2. \tag{5}$$

In the JLDMCSG MOSFET, the electric field at the center of the silicon channel is zero by symmetry

$$\left.\frac{\partial\phi_j(r,z)}{\partial r}\right|_{r=0}=0,\quad j=1,2, \tag{6}$$

and the electric flux at the interface between the gate dielectric and the silicon channel is continuous

$$C_{\rm ox}\left(V_{\rm gs}-\phi_{\rm MS}^{(j)}-\phi_j(r=R,z)\right)=\varepsilon_{\rm si}\left.\frac{\partial\phi_j(r,z)}{\partial r}\right|_{r=R},\quad j=1,2, \tag{7}$$

where $C_{\rm ox}=t'_{\rm ox}/\varepsilon_{\rm ox}$ is the effective gate capacitance, and $t'_{\rm ox}=R\ln(1+t_{\rm ox}/R)$ is the equivalent oxide thickness. The work function difference $\phi_{\rm MS}^{(j)}$ is given as

$$\phi_{\rm MS}^{(j)}=\phi_{\rm M}^{(j)}-\phi_{\rm si},\quad j=1,2, \tag{8}$$

in which, $\phi_{\rm M}^{(j)}$ is the metal work function of M_j, and $\phi_{\rm si}$ is the silicon work function of the channel, which can be written as

$$\phi_{\rm si}=\chi_{\rm si}+\frac{E_{\rm g}}{2q}-\phi_{\rm F}, \tag{9}$$

where

$$\phi_{\rm F}=\frac{kT}{q}\ln\left(\frac{N_{\rm D}}{n_{\rm i}}\right) \tag{10}$$

is the Fermi potential of the channel, $E_{\rm g}$ is the silicon band gap, $\chi_{\rm si}$ is the electron affinity, and $n_{\rm i}$ is the intrinsic carrier concentration.

From Eqs. (4)–(7), the solutions for $W_j(r)$ can be obtained as

$$W_j(r)=-\frac{qN_{\rm D}}{4\varepsilon_{\rm si}}r^2+V_{\rm gs}-\phi_{\rm MS}^{(j)}+\frac{qN_{\rm D}R}{2C_{\rm ox}}+\frac{qN_{\rm D}R^2}{4\varepsilon_{\rm si}}. \tag{11}$$

Using the separation variable method, one can obtain the general solution for $V_j(r,z)$ in the form of the Fourier–Bessel series, i.e.,

$$V_j(r,z)=\sum_{n=1}^{\infty}\left[C_n^{(j)}\exp\left(\frac{\alpha_n z}{R}\right)+D_n^{(j)}\exp\left(-\frac{\alpha_n z}{R}\right)\right]{\rm J}_0\left(\frac{\alpha_n z}{R}\right),\quad j=1,2, \tag{12}$$

where α_n is the eigenvalue and satisfies the equation

$$\frac{\varepsilon_{\rm ox}R}{t'_{\rm ox}\varepsilon_{\rm si}}{\rm J}_0(\alpha_n)-{\rm J}_1(\alpha_n)\alpha_n=0, \tag{13}$$

where ${\rm J}_i(x)$ is the first-kind Bessel function of the order i. Fourier–Bessel series coefficients $C_n^{(1)}$, $D_n^{(1)}$, $C_n^{(2)}$, and $D_n^{(2)}$ are determined by the following boundary conditions.

1) The electrostatic potential at the source end is

$$\phi_1(r,z=0)=0; \tag{14}$$

2) The electrostatic potential at the drain end is

$$\phi_2(r,z=L)=V_{\rm ds}; \tag{15}$$

3) The electrostatic potential at the interface of the two regions is continuous

$$\phi_1(r,z=L_1)=\phi_2(r,z=L_1); \tag{16}$$

4) The electric flux at the interface of the two regions is continuous

$$\frac{\partial\phi_1(r,z)}{\partial z}\Big|_{z=L_1}=\frac{\partial\phi_2(r,z)}{\partial z}\Big|_{z=L_1}. \tag{17}$$

Using these boundary conditions, the resultant expression of Fourier–Bessel series coefficients $C_n^{(1)}$, $D_n^{(1)}$, $C_n^{(2)}$, and $D_n^{(2)}$ can be obtained as

$$\begin{aligned}C_1=&\Big[\exp\Big(\frac{-\alpha_nL}{R}\Big)\Big(V_{\rm gs}S_0^{(n)}-U_1^{(n)}\Big)+\big(V_{\rm ds}-V_{\rm gs}\big)S_0^{(n)}\\&-U_2^{(n)}+\Big(\phi_{\rm MS}^{(2)}-\phi_{\rm MS}^{(1)}\Big)S_0^{(n)}\cosh\Big(\frac{\alpha_nL_2}{R}\Big)\Big]\\&\times[2\sinh(\alpha_nL/R)]^{-1},\end{aligned} \tag{18}$$

$$\begin{aligned}C_2=&\Big[\exp\Big(\frac{-\alpha_nL}{R}\Big)\Big(V_{\rm gs}S_0^{(n)}-U_1^{(n)}\Big)+(V_{\rm ds}-V_{\rm gs})S_0^{(n)}\\&-U_2^{(n)}+\Big(\phi_{\rm MS}^{(2)}-\phi_{\rm MS}^{(1)}\Big)S_0^{(n)}\cosh\Big(\frac{\alpha_nL_1}{R}\Big)\exp\Big(-\frac{\alpha_nL}{R}\Big)\Big]\\&\times[2\sinh(\alpha_nL/R)]^{-1},\end{aligned} \tag{19}$$

$$\begin{aligned}D_1=&\Big[-\exp\Big(\frac{\alpha_nL}{R}\Big)(V_{\rm gs}S_0^{(n)}-U_1^{(n)})-(V_{\rm ds}-V_{\rm gs})S_0^{(n)}\\&+U_2^{(n)}-\Big(\phi_{\rm MS}^{(2)}-\phi_{\rm MS}^{(1)}\Big)S_0^{(n)}\cosh\Big(\frac{\alpha_nL_2}{R}\Big)\Big]\\&\times[2\sinh(\alpha_nL/R)]^{-1},\end{aligned} \tag{20}$$

$$\begin{aligned}D_2=&\Big[-\exp\Big(\frac{\alpha_nL}{R}\Big)\Big(V_{\rm gs}S_0^{(n)}-U_1^{(n)}\Big)-(V_{\rm ds}-V_{\rm gs})S_0^{(n)}\\&+U_2^{(n)}-\Big(\phi_{\rm MS}^{(2)}-\phi_{\rm MS}^{(1)}\Big)S_0^{(n)}\cosh\Big(\frac{\alpha_nL_1}{R}\Big)\exp\Big(\frac{\alpha_nL}{R}\Big)\Big]\\&\times[2\sinh(\alpha_nL/R)]^{-1},\end{aligned} \tag{21}$$

with

$$S_0^{(n)}=\frac{2{\rm J}_1(\alpha_n)}{\alpha_n\big[{\rm J}_1^2(\alpha_n)+{\rm J}_0^2(\alpha_n)\big]}, \tag{22}$$

$$S_j^{(n)}=V_{\rm gs}S_0^{(n)}-U_j^{(n)}, \tag{23}$$

where

$$\begin{aligned}U_j^{(n)}=&\Big(-\phi_{\rm MS}^{(j)}+\frac{qN_{\rm D}t'_{\rm ox}R}{2\varepsilon_{\rm ox}}+\frac{qN_{\rm D}R^2}{4\varepsilon_{\rm si}}\Big)S_0^{(n)}\\&-\frac{qN_{\rm D}\big[R^2\alpha_n{\rm J}_1(\alpha_n)-2R^2{\rm J}_2(\alpha_n)\big]}{2\varepsilon_{\rm si}\big[{\rm J}_1^2(\alpha_n)+{\rm J}_0^2(\alpha_n)\big]\alpha_n^2}.\end{aligned} \tag{24}$$

By differentiating the central potential with respect to z, the central horizontal electric field is given as

$$E_j(z)=\sum_{n=1}^{\infty}\Big[C_n^{(j)}\exp\Big(\frac{\alpha_nz}{R}\Big)-D_n^{(j)}\exp\Big(\frac{-\alpha_nz}{R}\Big)\Big]\frac{\alpha_n}{R},\quad j=1,2. \tag{25}$$

2.2. Subthreshold current model

Using the channel potential solution, the subthreshold current can be calculated. Since the current density J has flowed predominantly in the z direction from source to drain, the electron quasi-Fermi potential $\phi_{\rm n}(z)$ is essentially constant in the r direction, then the current density (both drift and diffusion) can be written as

$$J(r,z)=-q\mu_{\rm n}n(r,z)\frac{{\rm d}\phi_{\rm n}(z)}{{\rm d}z}, \tag{26}$$

where $n(r,z)$ is the carrier concentration and $\mu_{\rm n}$ is the electron mobility. By integrating the current density $J(r,z)$ through the circular cross-section area in polar coordinates, the subthreshold current with respect to z can be expressed as

$$\begin{aligned}I_{\rm ds}(z)=&\,q\mu_{\rm n}\frac{{\rm d}\phi_{\rm n}(z)}{{\rm d}z}\\&\times2\pi\int_0^R rN_{\rm D}\exp\Big\{\frac{q[\phi(r,z)-\phi_{\rm n}(z)]}{kT}\Big\}{\rm d}r.\end{aligned} \tag{27}$$

By integrating the equation with respect to z from 0 to L, the subthreshold current can be obtained as

$$I_{\rm ds}=\frac{2\pi N_{\rm D}\mu_{\rm n}kT\big[1-\exp(-qV_{\rm ds}/kT)\big]}{\displaystyle\int_0^L\Big[\int_0^R r\exp\{q\big[\phi(r,z)\big]/kT\}{\rm d}r\Big]^{-1}{\rm d}z}. \tag{28}$$

Then the subthreshold current can be calculated as a function of $V_{\rm gs}$ and $V_{\rm ds}$. A constant mobility model is used in both the analytical model and numerical simulation.

3. Results and discussion

Using the derived analytical model, the subthreshold behavior of JLDMCSG MOSFETs is examined in terms of channel electrostatics potential distribution, electric field distribution, and subthreshold current. To verify these analytical models, the 3D device simulator ISE TCAD is employed to simulate the device characteristics. The simulated results of the quasi-2D model[18] are also included for comparison. Unless otherwise stated, the silicon channel doping concentration $N_{\rm D}=1\times10^{18}{\rm cm}^{-3}$ and the work functions of M_1 and M_2 are 4.7 eV and 4.4 eV, respectively.

In Fig. 2, the central electrostatic potential distributions along the channel are plotted for JLSMCSG MOSFETs and JLDMCSG MOSFETs with different ratios of $L_1:L_2$. Good agreement between the results calculated from the analytical model and those obtained from the 3D numerical device simulator is observed. It is shown in the figure that a step in the central potential distribution of the JLDMCSG MOSFETs exists, which ensures better screening of the minimum central potential near the source end from the drain voltage, leading to a better immunity to drain-induced barrier lowering (DIBL)

for the JLDMCSG MOSFETs. It is also found that when the length of M_1 is small (such as $L_1 : L_2 = 3 : 7$), the minimum central potential is higher than that when the length of M_1 is large (such as $L_1 : L_2 = 7 : 3$). For junctionless MOSFETs, the threshold voltage is mainly determined by the minimum position of the central potential. Therefore, JLDMCSG MOSFETs with a small ratio of $L_1 : L_2$ will exhibit a small threshold voltage. The tradeoff between DIBL and the threshold voltage should be seriously accounted for when JLDMCSG MOSFETs are designed.

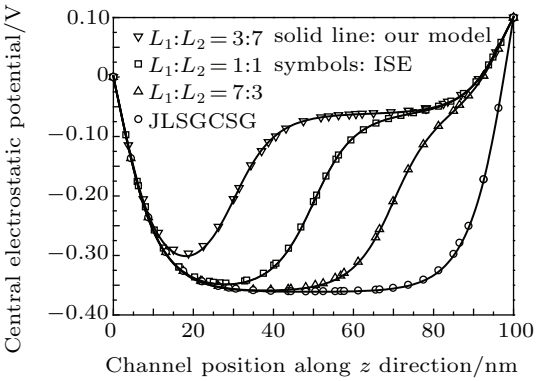


Fig. 2. The channel central electrostatic potential distributions for JLSMCSG MOSFETs and JLDMCSG MOSFETs with different ratios of L_1 to L_2. The simulated device parameters are, $R = 10$ nm, $t_{ox} = 2$ nm, $V_{gs} = 0.1$ V, and $V_{ds} = 0.1$ V.

Figure 3 shows the central electrostatic potential distribution along the channel for JLSMCSG MOSFETs and JLDMCSG MOSFETs with different drain biases. It is clear that, owing to the potential step in JLDMCSG MOSFETs, there is no significant change in the central electrostatic potential of region 1 when the drain bias is increased even up to 2.0 V. Hence, JLDMCSG MOSFETs account for the effective suppression to DIBL, whereas for JLSMCSG MOSFETs, although the minimum central potential is lower than that of JLDMCSG MOSFETs, the central potential is severely affected by the drain voltage. As the drain bias increases, the position of the minimum central potential for JLSMCSG MOSFETs shifts up, leading to intense DIBL.

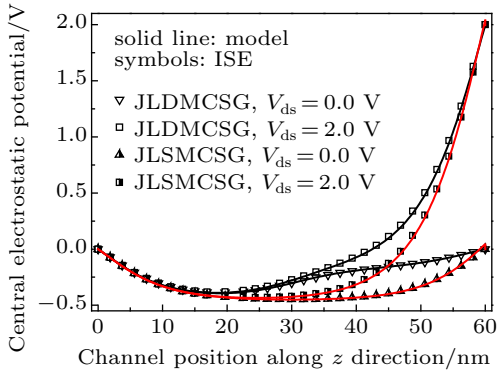


Fig. 3. (color online) Channel central electrostatic potential distributions for different drain voltages. The simulated device parameters are $R = 10$ nm, $t_{ox} = 2$ nm, and $V_{gs} = 0.1$ V.

The central electrostatic potential distribution along the channel for different channel lengths L is shown in Fig. 4. It can be seen that as the channel length decreases, the position of the minimum central electrostatic potential is pulled up, which implies that the minimum central electrostatic potential is seriously affected by the source/drain potential. Therefore, as the channel length decreases, the threshold voltage is reduced, resulting in one of the typical SCEs called "threshold voltage roll-off". It is also found that the quasi-2D method causes a considerable deviation from the numerical simulation results, especially near the source/drain side. In contrast to the quasi-2D potential approach, our model has a better agreement with the 3D numerical simulator.

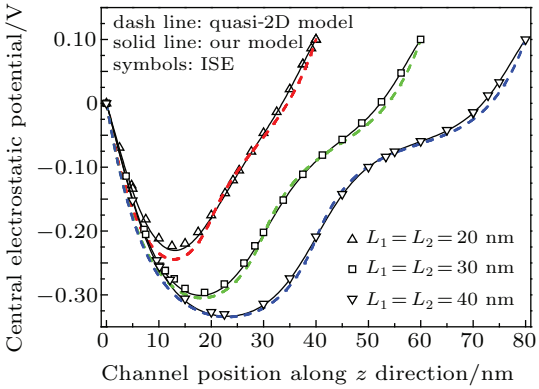


Fig. 4. (color online) Channel central electrostatic potential distribution for different channel lengths. The simulated device parameters are $R = 10$ nm, $t_{ox} = 2$, $V_{gs} = 0.1$ V, and $V_{ds} = 0.1$ V.

Figure 5 shows the central electrostatic potential distribution along the channel for JLDMCSG MOSFETs with different channel radii. It is revealed that a small radius of the silicon channel leads to better electrostatic potential distribution and thus better short-channel performance. It can be seen from the figure that for a quasi-2D model, large errors occur when the thickness of the silicon channel is much larger than that of the oxide.

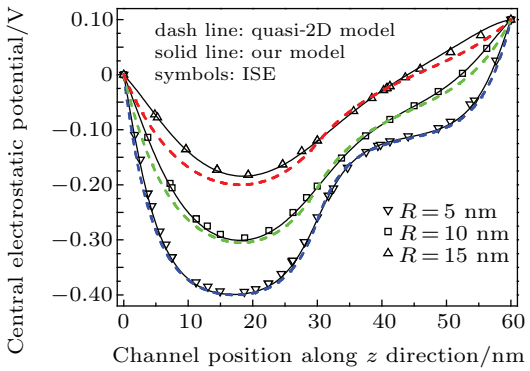


Fig. 5. (color online) The channel central electrostatic potential distribution for different channel radii. The simulated device parameters are $L_1 = L_2 = 30$ nm, $t_{ox} = 2$, $V_{gs} = 0.1$ V, and $V_{ds} = 0.1$ V.

The central horizontal electric field distributions for JLSMCSG MOSFETs and JLDMCSG MOSFETs are shown in Fig. 6. It is found that there is an electric field peak in the middle of channel of JLDMCSG MOSFETs, which ensures

a better average electric field across the channel when compared with JLSMCSG MOSFETs. Therefore, carrier transport efficiency and device speed are increased in JLDMCSG MOSFETs.

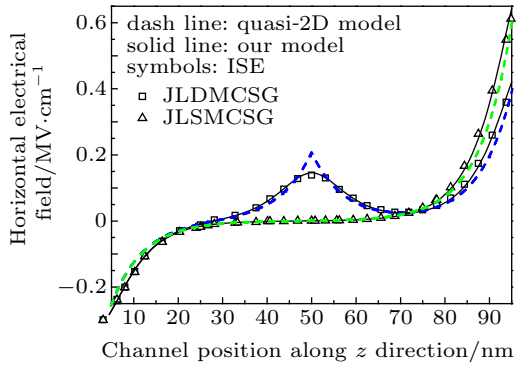


Fig. 6. (color online) Central horizontal electrical field distribution for JLSMCSG MOSFETs and JLDMCSG MOSFETs. The simulated device parameters are $L_1 = L_2 = 50$ nm, $t_{ox} = 2$ nm, $R = 10$ nm, $V_{gs} = 0.1$ V, and $V_{ds} = 0.5$ V.

Two-dimensional analytical potential contours of JLDMCSG MOSFETs are presented in Fig. 7. It is evident that the potential contours of region 1 have a tendency to bend vertically, which implies that the electric fields from M_1 can easily penetrate into the channel and control the threshold behavior. In contrast, the potential contours of region 2 are prone to bending horizontally. This indicates that most of the lateral electric field induced by drain voltage is completely absorbed in region 2, resulting in the effective suppression to DIBL.

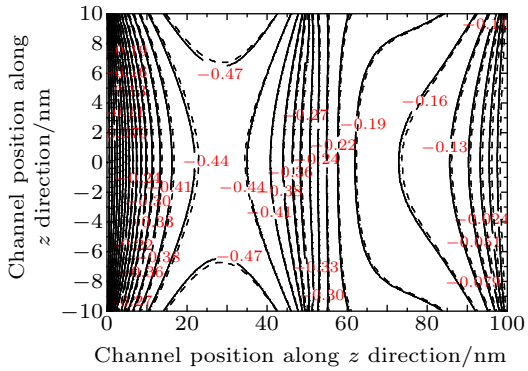


Fig. 7. (color online) The 2D electrostatic potential contours of the channel cut plane along the z direction. The solid lines represent the analytical model, and the dashed lines ISE TCAD. The simulated device parameters are $L_1 = L_2 = 50$ nm $t_{ox} = 2$ nm, $R = 10$ nm, $V_{gs} = 0.0$ V, and $V_{ds} = 0.0$ V.

Figure 8 shows the subthreshold current versus gate voltage for JLDMCSG MOSFETs with different oxide thicknesses. The data from the analytical model show very good agreement with those from the numerical simulation. From this figure, we can see that at the same V_{ds}, JLDMCSG MOSFETs with a thinner oxide give a smaller drain current under the subthreshold region. The reason for this is that in the subthreshold region of JLDMCSG MOSFETs, a thinner oxide thickness makes the electrons more easily depleted under the same biases, resulting in a smaller subthreshold current. Therefore, reducing the oxide thickness of JLDMCSG MOSFETs can be an effective method to decrease the subthreshold current.

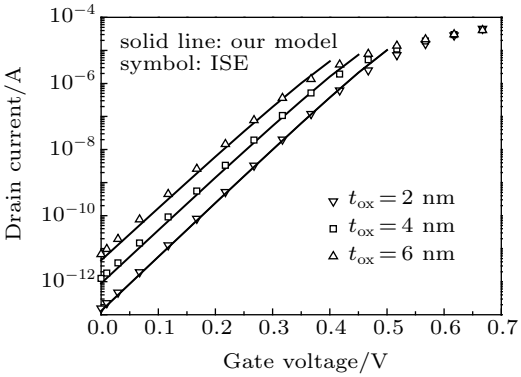


Fig. 8. The subthreshold current versus gate voltage for JLDMCSG MOSFETs with different oxide thicknesses. The simulated device parameters are $L_1 = L_2 = 50$ nm, $R = 10$ nm, $t_{ox} = 2$ nm $V_{gs} = 0.0$ V, and $V_{ds} = 0.5$ V.

Figure 9 shows the subthreshold current versus gate voltage for JLDMCSG MOSFETs with silicon radii as a parameter. From the plot, the smaller silicon radius leads to a smaller subthreshold current, which means that in order to reduce the subthreshold current, a thinner silicon channel is preferred. However, when the radius of the silicon channel is less than 5 nm, the quantum effects that cause different device characteristics will become important.[21] In this paper, we only investigate the device with a silicon channel radius larger than 5 nm. Therefore, quantum effects can be neglected.

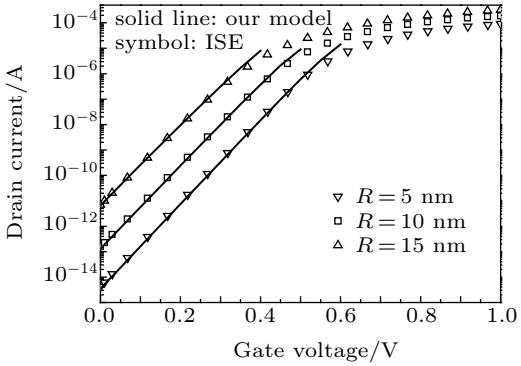


Fig. 9. The subthreshold current versus gate voltage for JLDMCSG MOSFETs with different silicon radii. The simulated device parameters are $L_1 = L_2 = 50$ nm, $t_{ox} = 2$ nm, and $V_{ds} = 0.5$ V.

The dependence of subthreshold current on gate bias for JLDMCSG MOSFETs with different ratios of $L_1 : L_2$ are shown in Fig. 10. It can be seen that the JLDMCSG MOSFETs with a small ratio of $L_1 : L_2$ can have a larger subthreshold current in comparison to those with a large ratio of $L_1 : L_2$. This is because when the length of M_1 is small (such as $L_1 = 30$ nm), the minimum central potential is higher than that when the length of M_1 is large (such as $L_1 = 70$ nm), which means that the potential barrier of the channel is lower when L_1 is small. For junctionless MOSFETs, the subthreshold current is mainly

determined by the height of the potential barrier of the channel. Therefore, JLDMCSG MOSFETs with a small ratio of $L_1 : L_2$ will exhibit a larger subthreshold current.

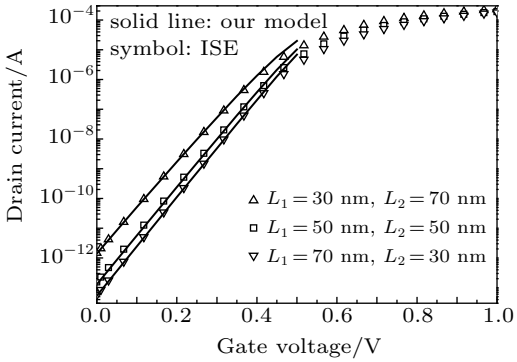


Fig. 10. Subthreshold current versus gate voltage for JLDMCSG MOSFETs with different ratios of $L_1 : L_2$. The simulated device parameters are $L = 100$ nm, $t_{ox} = 2$ nm, $R = 10$ nm, and $V_{ds} = 0.5$ V.

4. Conclusion

Based on the exact 2D resultant solution of Poisson's equation in two continuous channel regions, an analytical subthreshold behavior model for JLDMCSG MOSFETs has been successfully developed. It is shown that JLDMCSG MOSFETs exhibit superior performance over JLSMCSG MOSFETs in terms of channel central potential, carrier transport efficiency, and DIBL. It is revealed that both a thin gate oxide and thin silicon channel are needed to reduce the subthreshold current for JLDMCSG MOSFETs. The results obtained from the analytical models agree well with the simulated results obtained using the 3D numerical simulator ISE TCAD. This paper not only provides accurate analytical models for JLDMCSG MOSFETs, but also flexible design choices for optimizing the performance of JLDMCSG MOSFETs.

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