100-nm T-gate InAlAs/InGaAs InP-based HEMTs with $f_T = 249$ GHz and $f_{max} = 415$ GHz*

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InAlAs/InGaAs high electron mobility transistors (HEMTs) on an InP substrate with well-balanced cutoff frequency f_T and maximum oscillation frequency f_{max} are reported. An InAlAs/InGaAs HEMT with 100-nm gate length and gate width of 2×50 μm shows excellent DC characteristics, including full channel current of 724 mA/mm, extrinsic maximum transconductance $g_{m.max}$ of 1051 mS/mm, and drain–gate breakdown voltage BV_{DG} of 5.92 V. In addition, this device exhibits $f_T = 249$ GHz and $f_{max} = 415$ GHz. These results were obtained by fabricating an asymmetrically recessed gate and minimizing the parasitic resistances. The specific Ohmic contact resistance was reduced to 0.031 Ω·mm. Moreover, the f_T obtained in this work is the highest ever reported in 100-nm gate length InAlAs/InGaAs InP-based HEMTs. The outstanding $g_{m.max}$, f_T, f_{max}, and good BV_{DG} make the device suitable for applications in low noise amplifiers, power amplifiers, and high speed circuits.

Keywords: InP high electron mobility transistor, asymmetrically recessed gate, cutoff frequency f_T, maximum oscillation frequency f_{max}

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1. Introduction

The high electron mobility transistors (HEMTs) have potentials for applications in high-speed digital communication and microwave fields due to their superior transport properties.[1–3] InP-based InAlAs/InGaAs HEMTs have demonstrated high operating frequency, low microwave and millimeter-wave noise, as well as high-gain performance, all of which are very attractive for millimeter and sub-millimeter wave applications, due to the high sheet carrier density, high peak drift velocity, and high low-field electron mobility.[4,5] In recent years, many efforts have been made to improve the high-frequency characteristics of InAlAs/InGaAs HEMTs. A record maximum oscillation frequency (f_{max}) exceeding 1 THz and a record current-gain cutoff frequency (f_T) of 644 GHz have been reported in the sub 50-nm InP HEMTs and the 30-nm InAs HEMTs, respectively.[6,7] These remarkable results stem from the combination of harmonious size scaling and an increase of the indium content in the channel, improving the carrier transport properties. However, the reduction of the gate length increases technology difficulties and leads to a lower yield of the HEMTs. Furthermore, the HEMTs with an indium rich channel usually suffer from a serious kink effect, low breakdown voltage, and high output conductance,[8,9] leading to a much higher electric field under the gate area. Therefore, it is desirable to improve HEMTs' frequency characteristics without sacrificing their breakdown voltages and DC characteristics at a certain gate length, which is of great importance for their applications in low noise amplifiers (LNA), power amplifiers (PA), and high-speed circuits. Other efforts have been made to improve the performance of HEMTs, such as optimizing the side-recess spacing[10] and reducing the parasitic resistances of the source and the drain.[11]

In this paper, we describe the design, fabrication, and characteristics of 100-nm gate-length $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ InP-based HEMTs. An asymmetrical recessed gate and minimized parasitic resistances improved the extrinsic maximum transconductance $g_{m.max}$ and the frequency response of the HEMTs. An InP etching-stopper layer was designed to avoid the kink effect. A lattice-matched $In_{0.53}Ga_{0.47}As$ channel was adopted to improve the f_T and f_{max}. A non-alloyed Ohmic contact technique was used to produce a very low contact resistance and provide sharply defined Ohmic edges, and the gate recess process was optimized to trade off DC characteristics and RF performance. We improved the off-state breakdown voltage (BV_{DG}) of the device to 5.92 V by increasing the distance between the gate and the drain. High f_T/f_{max} values of 249/415 GHz and an extrinsic maximum transconductance $g_{m.max}$ of 1051 mS/mm were achieved at room temperature. These outstanding results are very promising for improving the performance of LNAs, PAs, and high-speed circuits.

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2. Device structure

A cross-sectional view of the InP HEMT is shown in Fig. 1. The epitaxial layer structures were grown by molecular beam epitaxy (MBE) on a 3-inch semi-insulating (100) InP substrate. The epitaxial structure of the HEMTs employed in our study was designed and optimized to balance the tradeoff between high-frequency characteristics and high breakdown voltage. From bottom to top, the epitaxial layers consisted of a 500-nm InAlAs buffer, a 15-nm $In_{0.53}Ga_{0.47}As$ channel layer, a 3-nm InAlAs spacer layer, an 8-nm InAlAs Schottky barrier layer, a 4-nm InP etching stopper layer, and a 20-nm Si-doped composite InGaAs cap layer. A Si-doped plane was inserted between the Schottky barrier layer and the spacer layer to supply the electrons for current conduction. The thick barrier layer was designed to decrease the gate leakage current, and finally enhance the channel current density and the off-state drain–gate breakdown voltage (BV_{DG}). A 10-nm Si-doped $In_{0.6}Ga_{0.4}As$ layer and a 10-nm Si-doped $In_{0.53}Ga_{0.47}As$ transition layer formed the composite cap layer to facilitate the formation of non-alloyed Ohmic contacts. All InAlAs layers were lattice matched with the InP substrate. Hall measurements made at room temperature showed a two-dimensional (2DEG) sheet density of 3.266×10^{12} cm^{-2} and a carrier mobility (μ_n) of 8000 $cm^2/(V{\cdot}s)$.

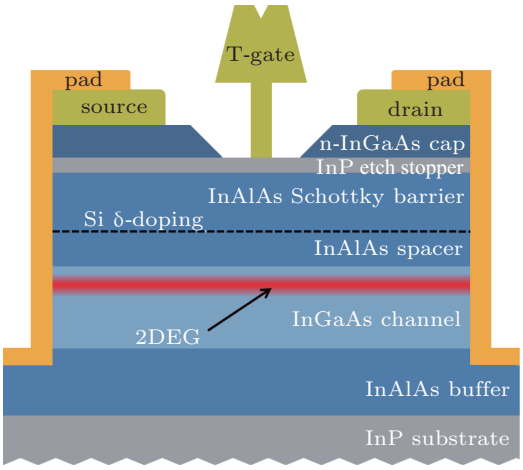


Fig. 1. (color online) Schematic cross-sectional view of the InP-based HEMT.

3. Fabrication process

The device fabrication started with isolating mesas by means of phosphorus acid-based wet chemical etching to expose the $In_{0.52}Al_{0.48}As$ buffer layer. Then, the source and the drain Ohmic contacts were spaced 2.4 μm apart by a lithography process. In the third step, Ti/Pt/Au (15 nm/15 nm/270 nm) was evaporated by electron beam evaporation to achieve Ohmic metallization without annealing. The contact resistance was determined by transmission line method (TLM) measurements to be about 0.031 Ω·mm and the specific contact resistivity was about 1.48×10^{-7} $\Omega{\cdot}cm^{-2}$. Afterward, the Ti/Au (15 nm/300 nm) connection pads were evaporated for on-wafer DC and RF characteristics measurements. Figure 2(a) shows a planar view of the fabricated HEMT with gate width of 2×50 μm. In our devices, the T-gate electrode was located at an offset position from the center toward the source. The spacing between the source and the gate foot was 0.875 μm, and the distance between the drain and the gate foot was 1.525 μm. A wider spacing between the gate and the drain electrodes is effective to obtain a large drain breakdown voltage BV_{DG}.

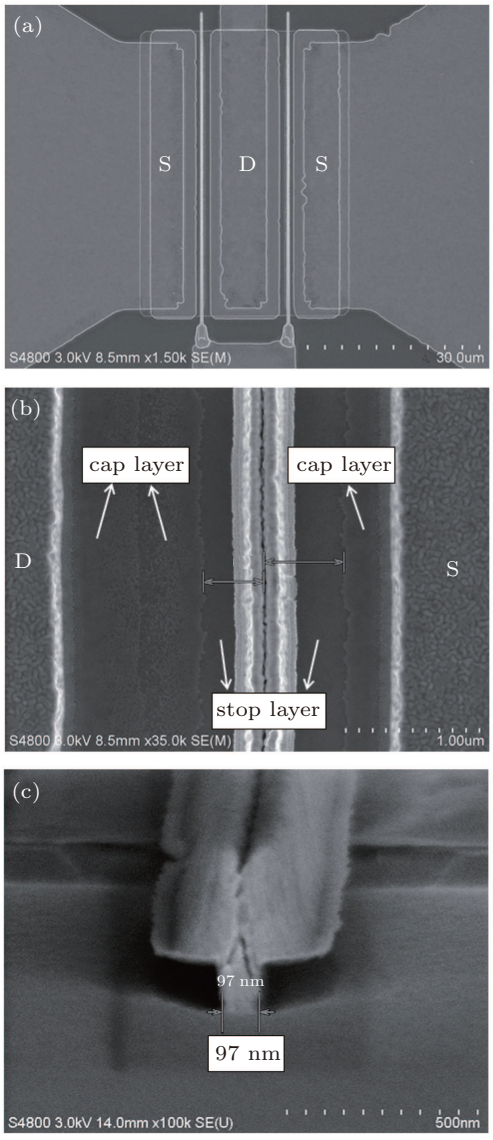


Fig. 2. (a) Photograph of the InP-based HEMT (2×50 μm). (b) SEM image of the device's gate recess region. (c) SEM micrograph of the fabricated 100 nm T-gate.

The gate process, which included gate lithography, recess, and metallization, was the last and the most important process in the HEMT fabrication. First, electron-beam lithography was applied to delineate a T-shaped gate, utilizing the

ZEP/PMGI/ZEP tri-layer e-beam resist stack. Second, the gate recess was formed by a phosphorus acid/hydrogen peroxide wet etching till the InP etching-stopper layer. Then an asymmetrical recessed gate with drain-side lateral recess length $L_{rd} = 404$ nm and source-side lateral recess length $L_{rs} = 550$ nm (see Fig. 2(b)) was fabricated through a certain gate recess etching process. Finally, a Ti/Pt/Au (25 nm/25 nm/300 nm) T-shaped gate metal was evaporated and lifted off. The gate length (L_g) is about 97 nm, as shown in Fig. 2(c). The shorter gate length improves the charge control efficiency and obtains a higher $g_{m.max} = 1051$ mS/mm compared with our previous 150 nm T-gate device with $g_{m.max} = 819$ mS/mm.

4. Results and discussion

4.1. DC characteristics

DC properties were characterized by using a HP4142 semiconductor parameter analyzer at room temperature. Figure 3 shows the current–voltage (I–V) characteristics of the HEMT with $L_g = 97$ nm and gate width $W_g = 2 \times 50$ μm at room temperature. The gate–source voltage (V_{GS}) is increased from −0.6 V to 0.4 V with step of +0.1 V, and the drain–source voltage (V_{DS}) changes from 0 V to 1.7 V. The HEMT presents good pinch-off characteristics, which is attributed to the enhancement of the gate modulation by using the recessed gate technique. Moreover, the kink effect of the device is negligible due to the introduction of the InP etching-stopper layer as the surface passivation, which makes the pinning Fermi level close to the conduction band minimum; thus, the initial density in the channel is high enough to decrease the impact of ionization and the traps in the buffer or barrier.[12,13]

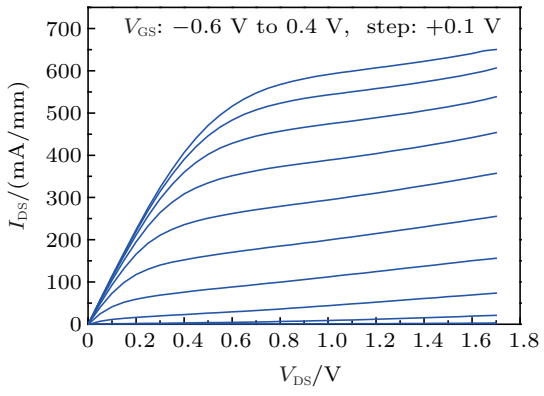


Fig. 3. (color online) DC output characteristics of the HEMT.

The extrinsic transconductance and the drain current of the HMET at the bias of $V_{DS} = 1.8$ V are shown in Fig. 4. The pinch-off voltage is about −0.6 V. A maximum extrinsic transconductance $g_{m.max}$ of 1051 mS/mm is achieved at $V_{GS} = -0.1$ V. It has a measured full channel current of 724 mA/mm at V_{GS} of 0.4 V and a saturation drain-to-source current I_{DSS} of 396 mA/mm at V_{GS} of 0 V.

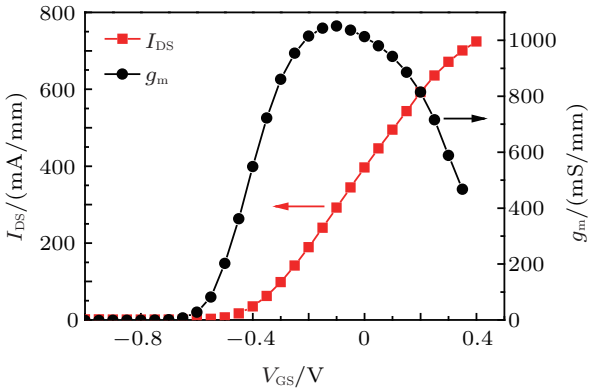


Fig. 4. (color online) Dependences of the extrinsic transconductance and the drain current on the gate bias of the HEMT with $V_{DS} = 1.8$ V.

Figure 5 shows the dependence of the transconductance on V_{DS} and V_{GS}. The intrinsic transconductance $g_{m.int}$ and the extrinsic transconductance $g_{m.ext}$ in the linear region (g_{ml}) and the saturation region (g_{ms}) can be expressed as

$$g_{ml.int} = \frac{\mu_n W \varepsilon_n \varepsilon_0}{L_g d_{GC}} V_{DS}, \tag{1}$$

$$g_{ms.int} = \frac{\mu_n W \varepsilon_n \varepsilon_0}{L_g d_{GC}} (V_{GS} - V_T), \tag{2}$$

$$g_{ml.ext} = \frac{g_{m.int}}{1 + g_{m.int} R_S + g_d (R_S + R_D)}, \tag{3}$$

$$g_{ms.ext} = \frac{g_{m.int}}{1 + g_{m.int} R_S}, \tag{4}$$

where μ_n is the electron mobility, W is the gate width, ε_n is the relative dielectric constant of the material between the channel and the gate, ε_0 is the dielectric constant of the air, L_g is the gate length, and d_{GC} is the distance between the gate and the two-dimensional electron gas.

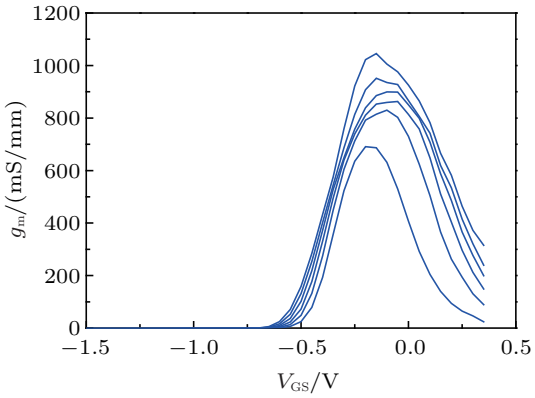


Fig. 5. (color online) Dependence of transconductance on the V_{GS}. The V_{DS} changes from 0.3 V to 1.8 V from the bottom up, and the sweep step is 0.3 V.

The intrinsic transconductances of the HEMT in the linear region ($g_{ml.int}$) and the saturation region ($g_{ms.int}$) are described

in Eqs. (1) and (2), respectively. When the device operates in the linear region, the transconductance increases with increasing V_{DS}, due to the increase of the electron drift velocity in the channel. Then the electron drift velocity will saturate at a certain V_{DS}, while the amount of electrons in the channel will increase with the increase of V_{GS} and finally become constant because of the finite δ Si-doping. So, the channel current increases with increasing V_{GS} and finally keeps constant; as Fig. 5 shows, the transconductance first increases and then decreases with increasing V_{GS}.

As seen in Eqs. (3) and (4), the high extrinsic transconductance of the HEMT is mainly related to the high intrinsic transconductance and the low series parasitic resistance. First, owing to the electron-beam lithography, the ZEP/PMGI/ZEP tri-layer e-beam resist stack was utilized, achieving an L_g = 97 nm T-shaped gate, which was much shorter than that of our previous devices. Also, d_{GC} was set to be 15 nm with the InP etching-stopper layer preserved by MBE. Decreased L_g and d_{GC} were used to improve the intrinsic transconductance. Second, the high dopant and high indium composition pseudomorphic cap layer resulted in a very small non-alloy Ohmic contact resistance of 0.031 Ω·mm, enhancing the extrinsic transconductance. Finally, the short source–drain space minimized the access part of the series parasitic resistance. In conclusion, reduced L_g and d_{GC}, small contact resistance, and short source–drain space are the main reasons for such a high extrinsic transconductance.

The measurement of the gate leakage current in the HEMT was performed using an HP 4142 semiconductor parameter analyzer. Both drain and source electrodes were grounded and a varying voltage from −2.0 V to +0.5 V was applied to the gate electrode. As shown in Fig. 6, this feature of small gate leakage current is extremely useful for the reduction of both DC power consumption and shot noise,[14] which is crucial for the LNA applications.

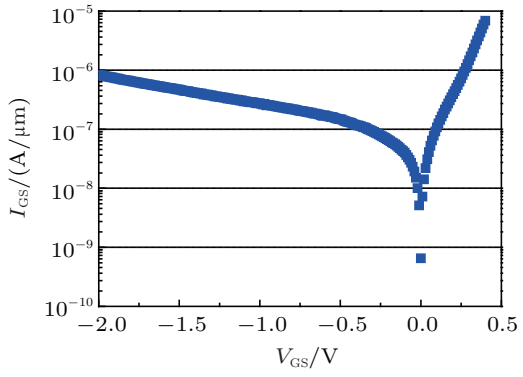


Fig. 6. (color online) Gate leakage current of the HEMT with V_{DS} = 0 V.

The drain-current injection technique was utilized to measure the drain–gate breakdown voltage by using an HP4155B semiconductor parameter analyzer.[15] To characterize the breakdown, a fixed predefined current of I_D = 1 mA/mm was injected into the drain, and the gate–source voltage V_{GS} was scanned from −3 V to 0 V. Then the drain-to-gate voltage V_{DG} and the gate current I_G were monitored. The BV_{DG} defined at $I_G = -I_D = -1$ mA/mm was 5.92 V, as shown in Fig. 7. The excellent BV_{DG} was due to the 15 nm distance from the gate to the channel and the manipulation of gate recess etching. Besides, the wide spacing between the gate and the drain relaxed the concentration of the electric field and suppressed the avalanche multiplication, which resulted in a large drain breakdown voltage.[16] Finally, compared with the reported $In_{0.7}Ga_{0.3}As$-$In_{0.52}Al_{0.48}As$ HEMTs,[17] our lattice matched HEMT (LM-HEMT) with a lower indium composition weakened the impact of ionization in the channel, as a result, the BV_{DG} increased from 3 V to 5.92 V. The higher BV_{DG} in our device brings a larger operating voltage in power applications and a larger logic swing in digital circuits.

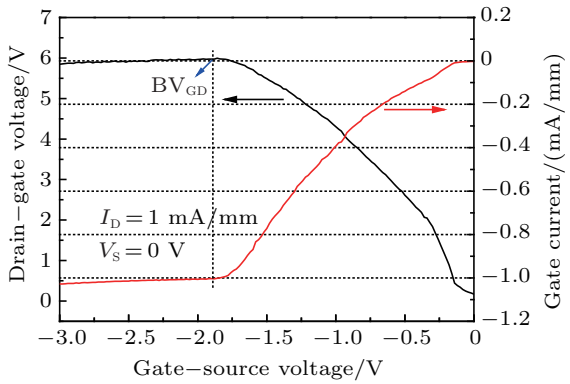


Fig. 7. (color online) Illustration of drain-current injection technique to measure the BV_{DG} of the HEMT.

4.2. RF characteristics

The RF characteristics were measured using an Agilent E8363B PNA vector network analyzer from 0.1 GHz to 40 GHz. On-wafer open and short patterns were used to subtract pad capacitances and inductances from the measured device S parameters. Figure 8 shows the RF characteristics of InAlAs/InGaAs HEMTs with L_g of 100 nm, approximately biased at the peak transconductance point of $V_{GS} = -0.1$ V, V_{DS} = 1.8 V. The values of f_T and f_{max} were determined by extrapolating the current gain (H_{21}) and the maximum available power gain (MAG) using a least-squares fitting with a −20 dB/decade slope after the parasitic parameters were de-embedded. Extrapolated f_T from H_{21} was 249 GHz and the extrapolated f_{max} based on MAG was 415 GHz. However, an MAG of 20.4 dB was measured at the instrumentation limit of 40 GHz, where the device was still potentially unstable ($K < 1$). Extrapolating the gain at −20 dB /decade from this point indicated an actual f_{max} larger than 415 GHz.

The decreased lateral gate-recess length L_r alleviates the kink effect and enhances the electric field in the channel to improve the f_T.[18] However, the reduction in L_r reduces the f_{max} by increasing the gate-to-drain capacitance C_{gd} and other parasitic capacitances.[19,20] Also, decreased drain-side lateral recess length L_{rd} has more critical effect on the increased f_T than source-side lateral recess lengths L_{rs}.[21] Therefore, an asymmetrically recessed gate with $L_{rd} = 404$ nm and $L_{rs} = 550$ nm has been fabricated to balance f_T and f_{max} characteristics. Table 1 shows the comparison between this device and our previous device with a symmetrical recessed gate on the same substructure.[22] The f_T greatly improves from 204 GHz to 249 GHz, although the L_g increases from 88 nm to 97 nm. Meanwhile, the f_T of our device is the highest among the reported 100-nm gate-length InAlAs/InGaAs InP-based HEMTs (see Table 2). In addition, the lattice-matched $In_{0.53}Ga_{0.47}As$ channel is adopted not only to ensure enough indium content in the channel but also to reduce lattice imperfections in the channel, leading to the highest f_T.

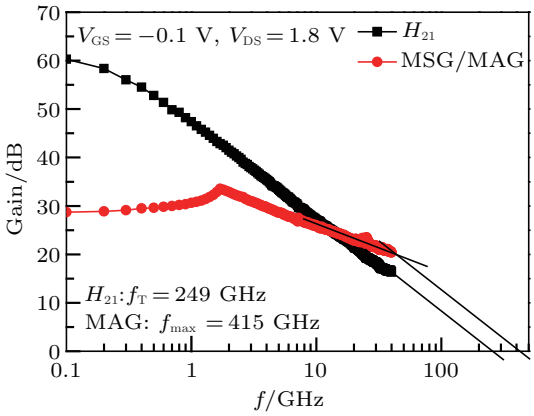


Fig. 8. (color online) The H_{21} and MAG/MSG versus frequency of the 100 nm gate length HEMT.

Table 1. Comparison with our previously reported devices.

Device	Recessed gate	L_g/nm	g_m/mS·mm^{-1}	f_T/GHz	f_{max}/GHz
Previous	symmetrical	88	918	204	352
This work	asymmetrical	97	1051	249	415

Table 2. Comparison with published InP HEMTs with gate length of 100 nm.

Reference	L_g/nm	f_T/GHz	f_{max}/GHz
[23]	100	228	—
[24]	100	208	460
[25]	100	209	220
[26]	100	220	300
[27]	100	209	226
[28]	100	200	220
[29]	100	180	—
[30]	100	183	230
This work	100	249	415

5. Conclusion

100-nm T-gate InAlAs/InGaAs InP-based HEMTs with a well-balanced high f_T of 249 GHz and f_{max} of 415 GHz have been fabricated. The extrinsic maximum transconductance was 1051 mS/mm and the off-state gate-to-drain breakdown voltage defined at a gate current of -1 mA/mm was 5.92 V. This outstanding performance stems from the reduction of parasitic capacitances by optimizing L_r and reducing the parasitic source and drain resistances through an optimized Ohmic contact process. The combination of high extrinsic maximum transconductance, low gate current, and excellent RF performance makes our device a superior candidate for LNA applications at millimeter-wave frequencies.

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