Analysis and modeling of resistive switching mechanism oriented to fault tolerance of resistive memory based on memristor*

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With the progress of the semiconductor industry, resistive memories, especially the memristor, have drawn increasing attention. The resistive memory based on memrsitor has not been commercialized mainly because of data error. Currently, there are more studies focused on fault tolerance of resistive memory. This paper studies the resistive switching mechanism which may have time-varying characteristics. Resistive switching mechanism is analyzed and its respective circuit model is established based on the memristor Spice model.

Keywords: resistive RAM, fault tolerance, resistive switching mechanism, circuit model

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1. Introduction

With increasing requirement in the speed and capacity of data storage, traditional dynamic random access memory (DRAM) encounters its inherent bottleneck. Magnetic random access memory (RAM), resistive RAM, and phase RAM hold the chance of replacing DRAM. Compared to magnetic RAM and phase RAM, resistive RAM has the advantage of programming power and cost-per-cell size.[1] Samsung, Panasonic, Fujitsu, as well as the European interuniversity microelectronics center (IMEC) have been investing effort in the research of resistive RAM based on memristor since 2010.

In 1971, Chua[2] predicted the existence of a fourth circuit component: memristor, which will link the magnetic flux with the electric charge. There are four kinds of basic variables: voltage V, current i, the magnetic flux φ, and the electric charge q. In 2008, Williams *et al*. announced the discovery of memristor-based TiO_2 which shows the two-terminal resistive switching characteristic, and it is the memristor predicted by Chua.[3]

Different from conventional CMOS circuit in which data errors are mainly caused by flip rays and particles, the memristor uses its resistance to store data. Hence, the instantaneous state error is most likely to occur because the slowly changing parameters are caused by the physical changes when the state is constantly changed. It may occur in the following situations: the initial high and low resistance of each memristor is not the same. The high and low resistance of each memristor changes with time. The initial conversion time of each memristor is not the same and the conversion time of memristor also changes slowly with time.

Currently, there are few studies on modeling memristor, where parameters change over time. However, it is important that without this model research into fault tolerance of resistive memory cannot be carried out. Due to the differences of preparing process as well as different material and electrodes used by various laboratories, they have different resistive switching mechanisms. There are studies on the resistive switching mechanisms, while few studies focused on its modeling. Based on the actual test, it is found that the resistive switching of memristor changes over time. However, there are no studies on this modeling yet.

An equivalent circuit model used to analyze the characteristics of a real experiment is commonly found in the physical research. For example, Pan *et al*.[4] constructed the equivalent circuit for the LC resonance giant magnetoimpedance effect, and they verified the correctness of the proposed equivalent circuit through the comparison of the circuit simulation results with the real experimental data. Hu *et al*.[5] used an equivalent circuit model to study the SiGe heterojunction bipolar transistor (HBT), the Pspice simulation results of the study provided an important theoretical guidance to the real experiment.

Based on the analysis of different resistive switching mechanisms, this paper analyzes the memristor whose parameters change over time from the view point of resistive switching mechanism and models of the respective resistive switching mechanism has been established. This work provides a basis for further simulation and research on fault tolerance of resistive memory.

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2. Memristor and its resistive switching mechanism

2.1. Theory of memristor

The memristance M satisfies the relationship between the magnetic flux φ and the electric charge q

$$M = \mathrm{d}\varphi/\mathrm{d}q. \tag{1}$$

Because the magnetic flux φ is the time integral of voltage V and the electric charge q is the time integral of current i, formula (1) can be transformed to

$$M(q(t)) = \int v(t) / \int i(\mathrm{d}t). \tag{2}$$

From Eq. (2), it can be seen that the memristance has the same dimension as the resistance and the resistance of memristor depends on the electric charge past through the memristor. Memristor has the feature of memory and its resistance remains unchanged in the case of the interruption of power supply.

In 1976, Chua and Kang perfected the theory of memristor and proposed the concept of memristive system[6]

$$\dot{\boldsymbol{x}} = \boldsymbol{f}(\boldsymbol{x}, u, t), \tag{3}$$

$$\boldsymbol{y} = g(\boldsymbol{x}, u, t)u. \tag{4}$$

In Eqs. (3) and (4), $y(t)$ and $u(t)$ are input and output variables, such as current $i(t)$, charge $q(t)$, voltage $v(t)$, and flux $\varphi(t)$. The $g(x,u,t)$ is a generalized response, such as memristance M, memductance W, memcapacitance C, and meminductance L. The x is a n-dimensional vector describing the internal state of the memory device, and $\boldsymbol{f}(\boldsymbol{x},u,t)$ is a continuous n-dimensional vector function. It is named memristive system which satisfies Eqs. (3) and (4). It expands the concept of memristor theoretically.

Through the above analysis, it can be seen that memristor has three main features:

1) Compared with the ordinary resistor, the resistance of memristor is continuously adjustable which changes with the electric charge through by.

2) It can be converted into two different resistance states by applying the voltages and the ratio between these two resistance can reach 10^2 to 10^7.

3) It shows characteristics of hysteresis in low frequency and shows a linear resistor in high frequency. Figure 1 shows a typical I–V curve of memristor.

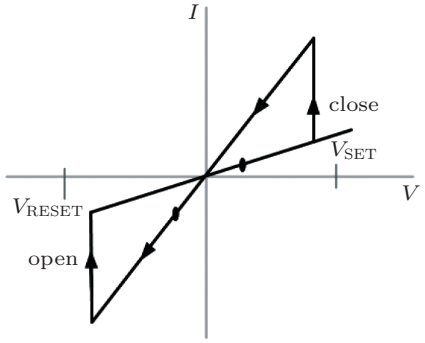


Fig. 1. Typical I–V curve of a memristor.

2.2. Resistive switching mechanism of memristor

More research concentrates on materials with resistive switching, such as SiO_2, NiO, ZrO_2, TiO_2, perovskite, and organic synthetic materials. Materials usually used as electrodes in the structure of metal–insulator–metal (MIM) include Pt, Au, Cu, Ni, W, Al, and TiN.[7] Choosing different kinds of electrodes and using different materials with different doped materials lead to different conductive mechanisms.

Current, there are several resistive switching mechanisms in the following: boundary drift model, filament conducting, ion migration, Schottky barrier model, trap charging and discharging, SCLC model,[8] and so on. Except for the six resistive switching mechanisms mentioned above, there are other models to explain different materials with different doping materials. In fact, not only the material and the doping material selected, but also the chosen electrode and the thickness of the main material may lead to different mechanisms.[9] Much effort has been invested in analyzing from the view of electrochemical and physical principles. In this paper, we try to analyze the differences of these mechanisms from the view of circuitry to establish their respective circuit models.

Boundary drift model proposed by HP Labs has a quantitative description while other models only have qualitative description of resistive switching mechanism. HP labs believed that +2 oxygen vacancies in the TiO_2 and TiO_{2-x} drift up and down in the electric field formed by positive and negative voltage applied on electrodes.[10] In the structure of Pt/TiO_{2-x}/Pt, two conductive parts in series are separated, which have different resistances. Due to the drifting of +2 oxygen vacancies, the boundary of two parts moves, making the overall resistance switching. The boundary drift model requires that

$$R_{\mathrm{total}} = R_{\mathrm{on}} \frac{\omega(t)}{D} + R_{\mathrm{off}} \left(1 - \frac{\omega(t)}{D}\right), \tag{5}$$

where R_{on} and R_{off} presents the resistance of TiO_{2-x} and TiO_2, respectively. The orders of magnitude of on–off ratio is usually greater than three.

2.3. Modeling of resistive switching mechanism

In this section, we propose the unified circuit model oriented to different resistive mechanisms. Resistive mechanisms involve too many actual physical details. When we design the circuit model, we ignore some of the specific details of the various mechanisms. The common characteristics of resistive mechanisms are modeled and manifested. We model and classify resistive switching mechanisms. It is known that the internal electrochemical or physical changes cause the overall resistance changing. Boundary drift model proposed by HP labs has been modeled. The filament conducting has a different circuit model. The resistance of the original dielectric material is high, and the resistance of the filament is low. The two parts are in parallel.

From circuit analysis, the change part of resistance R_x and the fixed part of resistance R_t are in different distribution,[11] typically in the relationship of series and parallel. It is shown in Fig. 2.

Resistive switching is caused by proportion changes of the conductive and the less conductive parts in the above mechanisms, and these changes are in physical or chemical structure of the material. It can be modeled that the distribution of resistor in series or parallel is fixed and only the variable resistor changes with the applied voltage. For the variable resistor R_x, we have

$$V = R_x(q,\varphi)i. \tag{6}$$

We define $R_x(q,\varphi)$ as a function of resistive switching. In further analysis in Section 1, the resistive switching function should satisfy

$$\dot{R_x} = f(u,i,t), \tag{7}$$

where u and i denote the voltage and current at time t.

Function f represents the change related to the excitation of voltage and current as well as time t. The function f used in different mechanisms is similar while it has different parameters and different distribution of resistors in series or parallel.

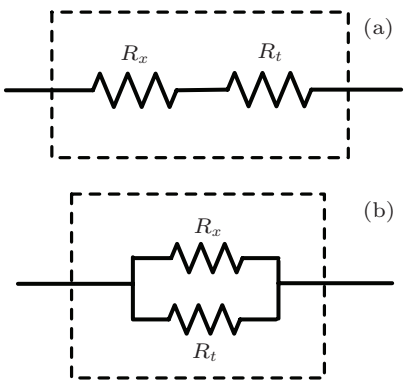


Fig. 2. Schematic of (a) series and (b) parallel resistive switching circuit.

Similar to the filament conducting, the ion migration model is suitable to the circuit model in parallel. In addition, the actual structure of filaments or ion conductive pathways is not necessary to be geometric regular, and there are many nodes, blobs, and links between filaments. The Schottky barrier model, the trap charging, and the discharging model, as well as the SCLC model are different. In fact, they are suitable for the circuit model in series.

To accord with real physical or chemical changes, different mechanisms may be the combination of both resistors in series and parallel by circuit modeling. There are two methods to simplify the model. One is equivalent transformation of the circuit. We can equivalently transform the value of changeless resistor R_t, so the circuit is transformed from a complex circuit to resistors in series or parallel without changing the variable resistor R_x. The other is choosing the dominant distribution of resistors and modeling with resistors in series or parallel.

3. Modeling of resistive switching mechanism oriented to fault tolerance

3.1. Data errors of memristor

Data errors of memristor can be divided into permanent errors and transient errors. Permanent errors refer to memristor which has permanent error. It can no longer possess resistive switching and its possible causes include defect in preparation and being applied the voltage which is too high. The transient error is most likely to occur in data storage. The high and low resistances of memristor usually represent the data "0" and "1" in data storage. When a transient error occurs, the resistance of memristor is in the wrong state. The following is several possible causes.

(i) External factor In the resistive memory read and write strategy, the data is judged by the region of resistance. After the memristor are read and written many times, the drift of resistance of memristor accumulates, which is likely to cause an transient error.

(ii) Internal factor Various parameters of the time-varying memristor change, so read and write strategy which is in accordance with the original parameters of the memristor may bring misunderstanding and misuse write. The possibility grows over time.

We analyze the causes of data errors theoretically. From Eq. (2) in Section 2, we know that the memristance which means the resistance of memristor is determined by the rate of the time integral of voltage and the time integral of current. In the resistive memory, data stored in memristor are read out by applying a small voltage which is not enough to change the state of the memristor. Data are read by the size of current used to determine whether it is in a high resistance state or low resistance state. Therefore, every time the data reading

will bring a small impact on the resistance of memristor because of the applied voltage. When it accumulates to a certain extent, data errors occur.

When switching between high resistance state and low resistance state, the physical characteristic of memeristor does not always return to the original condition accurately. For example, in the boundary drift model boundary does not reach the same position every time. Filament is formed with different shapes in the same state in the model of filament conducting. Some of these differences may vary with time in a certain range, while others are increasing with time. Thus, various parameters of the memristor will change over time.

3.2. Error analysis based on resistive switching mechanism

According to external factor and internal factor of the data error, we analyze from resistive switching mechanism to find its theoretical basis.

The current and voltage of function f should be a linear relationship in boundary drift model, filament conducting model and ion migration model. Although the high resistance region and low resistivity region are not evenly distributed, we consider the resistance should be changed in a linear relationship in the equivalent boundary model. Both a conductive wire in the filament conducting model and an ion channel in the ion migration changes linearly. In the Schottky barrier model, the current–voltage is not linear because it accords with thermionic emission theory. In trap charging and discharging model and SCLC model, resistance changes segmental. There are both linear change segmentation and non-linear change segmentation.

This paper focuses on resistive switching mechanism, so we try to study the internal factor of data error through resistive switching mechanism. Not only the material and the doping material selected, but also the chosen electrode and the thickness of the main material may lead to different mechanisms.[9] Moreover, the external physical characteristics will change with increasing read and write times of memristor-based resistive memory. There are studies on qualitative description of resistive switching mechanism while few studies focus on modeling and its detail. As research on parameters changing over time is important to the fault tolerance of memristor-based resistive memory, so it is necessary to represent the parameter change when modeling resistive switching mechanism.

In conclusion, the results of memristor prepared in laboratory show that after being applied a voltage repeatedly the parameters of the memristor changes mainly because of parameter changes of resistive switching mechanism or changes of distribution of resistor in series or parallel in our modeling of resistive switching mechanism.

3.3. Resistive mechanism switching modeling

This section focuses on establishment of circuit models of resistive mechanism switching based on the existing memristor spice model to represent the parameter of resistive switching mechanism changes. From the previous section we know that the parameter changes of memristor because of changes in the distribution or parameter changes of resistive mechanism switching.

In Eq. (7), function f is related to resistive switching,

$$\dot{R}_x = f(u,i,t). \tag{8}$$

In order to represent parameter changes of resistive mechanism switching, we amend Eq. (7) as

$$\dot{R}_x = f(u,i,t)g(T). \tag{9}$$

The function g is a coefficient of the parameter of resistive switching mechanism changing with time T, which may be divergent with time or converge with time.

At present, the spice model of memristor in circuit modeling studies often refers to a voltage-controlled current source in parallel with a resistor forming a resistive switching device. The voltage-controlled current source is controlled by a sub-circuit, which is determined by the voltage applied on the memristor as well as other resistances, capacitances, voltage-controlled voltage sources, and voltage-controlled current sources. However, this model cannot represent the parameter changes over time and parameter changes of resistive switching mechanism over time.

Finally, we model resistive switching mechanism in two steps. First, we use the existing memristor spice model to exhibit resistive time-invariant part. Then through a time-varying resistance in series the parameter changes is represent over time. Specific experimental details will be described in the next section.

4. Modeling and simulation of memristor-based resistive switching mechanism

Spice model was originally developed at the Electronics Laboratory of the University of California, Berkeley in 1975 by Nagel.[12] Among the commercial spice simulators, HSpice is the most widely adopted and capable of analyzing steady state, transience, and frequency. In the present paper, we adopt HSpice to simulate the modeling of resistive switching. The spice model of memristor is shown in Fig. 3. In this figure, the left part is the circuit model of memristor where the current source circuit G_{mem} is controlled by the voltage at point x in the right sub-circuit. In the right sub-circuit, two current sources charge and discharge the capacitor, which indicates that the memristance is determined by the rate of the time integral of the voltage and the time integral of the current. The circuit model accords with the origin theory of memristor. On

the left-hand side, the resistor in series R_{series} means the constant resistance R_t in the distribution of series. We can change it to parallel distribution by adding an actual resistance in parallel. Thus, the spice model of memristor is able to adapt to different resistive mechanisms.

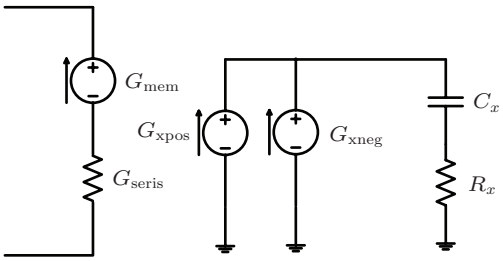


Fig. 3. Spice model of memristor.

In the environment of HSpice, using existing spice models of memristor,[13] the same function f and the same corresponding parameters are presented. In order to exhibit parameter changes of resistive switching mechanism over time, we use a 0.001-Ω resistor in series which is in parallel to a voltage-controlled current source. The voltage-controlled current source changes with the voltage applied to the memristor, which makes it easier to find the variation trends. The distribution of resistor in our experiment is in series. The parameter of resistive switching mechanism changes with time, which makes the resistance of memristor change with time.

Figure 4 shows the experimental results, and figures 4(a) and 4(b) show results of different parameters of the voltage-controlled current source. It can be seen from Fig. 4(a) that the resistance of memristor changes with time. In this process, low state resistance increases. High state resistance also increases, and the rate is not as significant as low state resistance. The high and low resistance switching ratio decrease. It accords with experimental data of prepared memristor, which reflects the durability of memristor as well as parameter changes of resistive switching mechanism over time. Figure 4(b) is slightly different from Fig. 4(a). In Fig. 4(a), it is relatively symmetrical from positive side to negative side, while in Fig. 4(b), it is asymmetric from positive side to negative side. It can be seen that the low state resistance increases significantly from the positive axis as the sinusoidal voltage is applied.

Figures 4(a) and 4(b) both show the characteristics of time-varying parameters of memeristor in this model. The size of change in low resistance state and high resistance state is similar, so the change shown in the low resistance state and high resistance state is different for the different original resistances. Compared to typical I–V curve of memristor, this model is more adaptable and flexible in the studies on fault tolerance of resistive memory. Experimental results show that the model can represent that the parameter of resistive switching mechanism is time-varying.

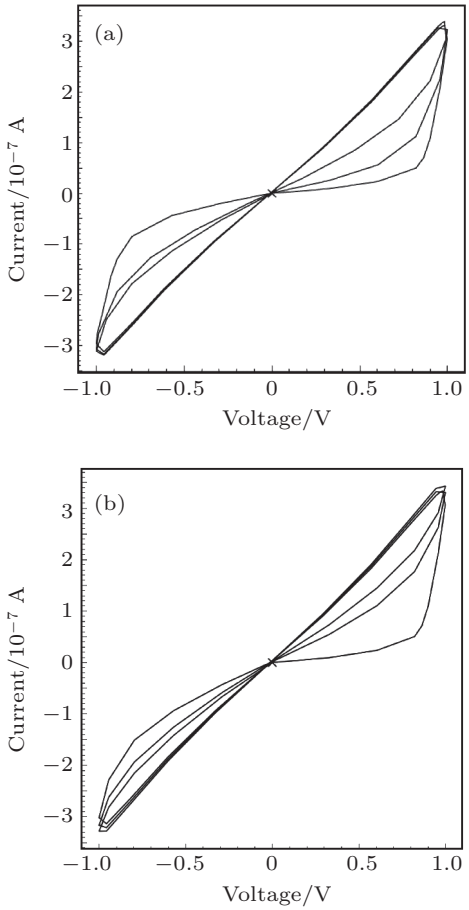


Fig. 4. I–V curve of time-varying memristor.

5. Conclusions

Memristor-based resistive memory will bring remarkable impact on computer. Currently, the first problem about resistive memory[14] is to improve its reliability before commercialization. Studies on resistive switching mechanism are the key to solve the problem. The analysis of resistive switching mechanism can be used to predict the occurrence of the probability distribution of data storage error in resistive memory. Thus, the corresponding error checking and correcting method can be applied to increase the reliability of resistive memory. In this paper, based on existing spice models of memristor, resistive switching mechanism is analyzed and the circuit model of time-varying resistive switching mechanism is established. The experimental results show the correctness of our modeling. This work provides a basis for further simulation and research on fault tolerance of resistive memory.

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