# Through-silicon-via crosstalk model and optimization design for three-dimensional integrated circuits*

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Through-silicon-via (TSV) to TSV crosstalk noise is one of the key factors affecting the signal integrity of three-dimensional integrated circuits (3D ICs). Based on the frequency dependent equivalent electrical parameters for the TSV channel, an analytical crosstalk noise model is established to capture the TSV induced crosstalk noise. The impact of various design parameters including insulation dielectric, via pitch, via height, silicon conductivity, and terminal impedance on the crosstalk noise is analyzed with the proposed model. Two approaches are proposed to alleviate the TSV noise, namely, driver sizing and via shielding, and the SPICE results show 241 mV and 379 mV reductions in the peak noise voltage, respectively.

**Keywords:** three-dimensional integrated circuits, through-silicon-via crosstalk, driver sizing, via shielding

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## 1. Introduction

Through-silicon-via (TSV) based three-dimensional (3D) integration is a promising design for interconnect-centric circuits.[1–4] One of the most important benefits of the 3D architecture over a conventional two-dimensional (2D) system is the reduction in global interconnects and total wire length, thereby providing lower cost, smaller form factor, and higher performance. The signal integrity (SI) is expected to be a major concern for 3D integrated circuits (ICs) due to the high frequency loss and the electromagnetic radiation in such a tiny 3D space. The crosstalk noise induced by TSV is one of the biggest challenges because of its large area and high density. The TSV-induced noise can increase the interconnect delay due to the Miller effect of coupling capacitance. Additionally, it may result in wrong logic function of adjacent digital cells due to the noise injection. It is therefore crucial to evaluate and suppress the crosstalk noise in 3D ICs.

According to the differences in coupling path, the TSV-induced noise can be classified into three different types: (i) TSV landing pad-to-adjacent metal interconnects noise coupling: the coupling mechanism of this crosstalk noise is similar to the conventional wire coupling, it therefore can be analyzed and optimized by existing SI tools;[5] (ii) TSV-to-S/D region of MOSFET coupling noise: this coupling path is mainly on the substrate surface, and it can be effectively suppressed by adding sufficient substrate contacts to the ground;[6,7] (iii) TSV-to-TSV crosstalk noise: since the via goes through the entire substrate, this coupling occurs in the substrate surface and inside the substrate, just adding substrate contacts cannot completely isolate the crosstalk noise. Additionally, since the coupling capacitance between the TSVs is more complicated, which consists of an insulation dielectric and a silicon substrate, the crosstalk noise cannot be controlled by existing SI tools. To electrically characterize the TSV-to-TSV crosstalk noise, Pak *et al.* analyzed the impact of structural parameters such as TSV size, TSV pitch, and the thickness of $SiO_2$ for the DC isolation between the TSV and the silicon substrate, and material parameters of the silicon substrate such as silicon resistivity on the crosstalk noise of adjacent TSVs with the finite element method solver from HFSS.[8] Sun *et al.* simulated the capacitive and inductive coupling between TSVs in a TSV array and presented solutions to decrease the crosstalk.[9] The finite element analysis is more accurate, however, the high computation time and large memory needed make it unsuitable for large scale integrated circuit designs. Engin *et al.* presented analytical formulas to extract an equivalent circuit model for the coupled TSV structures in a 3D integrated system and studied the crosstalk behavior of TSVs with a spice type circuit simulator.[10] Khan *et al.* proposed a SPICE model for simulating TSV-to-TSV and TSV-to-device and investigated the transient response characterization of the crosstalk noise as a function of several design parameters.[11] Using an equivalent lumped model of silicon substrate and TSV, Cho *et al.* estimated the noise transfer functions from TSV to TSV and from

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TSV to the active circuit and simulated the timing jitter degradation on the phase locked loop.[12] However, the impact of the operating frequency on the parasitic, which had a big contribution to the TSV crosstalk in the entire frequency domain, was ignored in the model. Moreover, although the SPICE-based tool accelerates the analysis of TSV coupling, it may need a long time for comprehensive characterization, especially when multiple parameters are involved. It is necessary to find an analytical crosstalk model for fast and accurate estimation of the TSV-to-TSV crosstalk noise.

Based on the frequency dependent equivalent electrical parameters, an analytical crosstalk model is established to capture the crosstalk noise between neighboring TSVs. Two approaches are proposed to alleviate the TSV noise. The rest of the paper is organized as follows. An analytical crosstalk model is presented and compared with HFSS in Section 2, then the impact of various design parameters, including insulation dielectric, via pitch, via height, and silicon conductivity on the coupling noise, is analyzed in Section 3. Two design methodologies, namely driving sizing and via shielding, are introduced to alleviate the crosstalk noise in Section 4. Finally, a conclusion is provided in Section 5.

## 2. TSV-to-TSV crosstalk model

Figure 1 shows a T-type equivalent electrical model and the simplified coupling transfer path for the TSV-to-TSV structure, which consists of a via copper, an insulator dielectric, a silicon substrate, and I/O drivers. Here, the aggressor and the victim are driven by the same I/O ports. Since the height of the TSV, which is around 50–200 μm, is shorter than 1/20 guided wavelength in the silicon substrate ($\lambda = 4.35$ mm at 20 GHz), the lumped elements of $R_{\rm tsv}$, $C_{\rm SiO2}$, and $L_{\rm tsv}$ can be used to model the resistance, the capacitance, and the inductance of the TSV, respectively.[13] The lossy silicon substrate is modeled as an equivalent conductance $G_{\rm Si}$ in parallel with a capacitance $C_{\rm Si}$. Additionally, note that the channel impedance composed of the insulator dielectric and the lossy substrate is higher than the TSV serial impedance, the impact of $R_{\rm tsv}$ and $L_{\rm tsv}$ on the noise coupling is therefore ignored. Using Kirchhoff's law, the simplified coupling model can be expressed as the following circuit matrix:

$$\begin{bmatrix} \frac{1}{Z_0}+\frac{1}{Z_0}+\frac{1}{Z_{\rm C}} & -\frac{1}{Z_{\rm C}} \\ -1 & 1+\frac{Z_{\rm C}}{Z_0}+\frac{Z_{\rm C}}{Z_0} \end{bmatrix} \cdot \begin{bmatrix} V_{\rm in} \\ V_{\rm out} \end{bmatrix} = \begin{bmatrix} \frac{V_{\rm in}}{Z_0} \\ 0 \end{bmatrix}, \quad (1)$$

where $Z_0$ and $Z_{\rm C}$ are the equivalent impedances of the I/O driver and the TSV channel, respectively. By solving Eq. (1), the output crosstalk voltage $V_{\rm out}$ is derived as a function of input excitation $V_{\rm in}$

$$V_{\rm out} = \frac{V_{\rm in}}{4} \cdot \frac{Z_0}{Z_0 + Z_{\rm C}}. \quad (2)$$

To accurately evaluate the TSV coupling characterization in the frequency domain, a little modification is applied in Fig. 1 to include the impact of the operation frequency on the channel impedance

$$Z_{\rm C} = Z_{\rm Si} + 2Z_{\rm SiO2} = 1/\omega C_{\rm equ} + 1/G_{\rm equ}, \quad (3)$$

where $Z_{\rm Si}$ and $Z_{\rm SiO2}$ are the equivalent impedances of the silicon substrate and the isolation dielectric, respectively, and $\omega$ is the radian frequency. Here, equivalent conductance $G_{\rm equ}$ and equivalent capacitance $C_{\rm equ}$ of the TSV coupling channel are functions of the frequency[10,12,14]

$$C_{\rm equ} = \frac{-2\omega^2 C_{\rm SiO2} C_{\rm Si} G_{\rm Si} + \omega^2 C_{\rm SiO2} G_{\rm Si}(2C_{\rm Si} + C_{\rm SiO2})}{4G_{\rm Si}^2 + \omega^2 (2C_{\rm Si} + C_{\rm SiO2})^2}, \quad (4)$$

$$G_{\rm equ} = \frac{2C_{\rm SiO2} G_{\rm Si}^2 + \omega^2 C_{\rm SiO2} C_{\rm Si}(2C_{\rm Si} + C_{\rm SiO2})}{4G_{\rm Si}^2 + \omega^2 (2C_{\rm Si} + C_{\rm SiO2})^2}, \quad (5)$$

$$C_{\rm SiO2} = \frac{2\pi\varepsilon_{\rm ox} l_{\rm tsv}}{\ln((r_{\rm via} + t_{\rm ox})/r_{\rm via})}, \quad (6)$$

$$C_{\rm Si} = \frac{\pi\varepsilon_{\rm Si} \cdot l_{\rm tsv}}{\cosh^{-1}[p_{\rm tsv}/2 \cdot r_{\rm via}]}, \quad (7)$$

$$G_{\rm Si} = \frac{\sigma_{\rm Si} \cdot C_{\rm Si}}{\varepsilon_{\rm Si}}, \quad (8)$$

where $r_{\rm via}$ is the TSV radius, $l_{\rm tsv}$ is the TSV height, $\varepsilon_{\rm ox}$and $t_{\rm ox}$ are the permittivity and the thickness of the insulator dielectric surrounding TSV, respectively, $p_{\rm tsv}$ is the TSV-to-TSV pitch, and $\sigma_{\rm Si}$ and $\varepsilon_{\rm Si}$ are the conductivity and the permittivity of the silicon substrate, respectively.

To verify the proposed TSV crosstalk model, we compare the coupling coefficient $S_{41}$ obtained from the commercial 3D electromagnetic simulator HFSS[15] and from our analytical crosstalk noise model in Fig. 2. The terminal condition of 50 Ω is used to eliminate the effect of signal reflection. As the figure shows, the proposed model is quite accurate in the simulated frequency range, its maximum error and average error are 4.21% and 1.94%, respectively. Moreover, the simulation time required by the proposed model is less than 30 s with a MATLAB program, in contrast to 5 min by the HFSS simulator on the same computer. The proposed analytical model therefore can be applied to the crosstalk noise analysis and the optimization design of TSV-based 3D ICs.

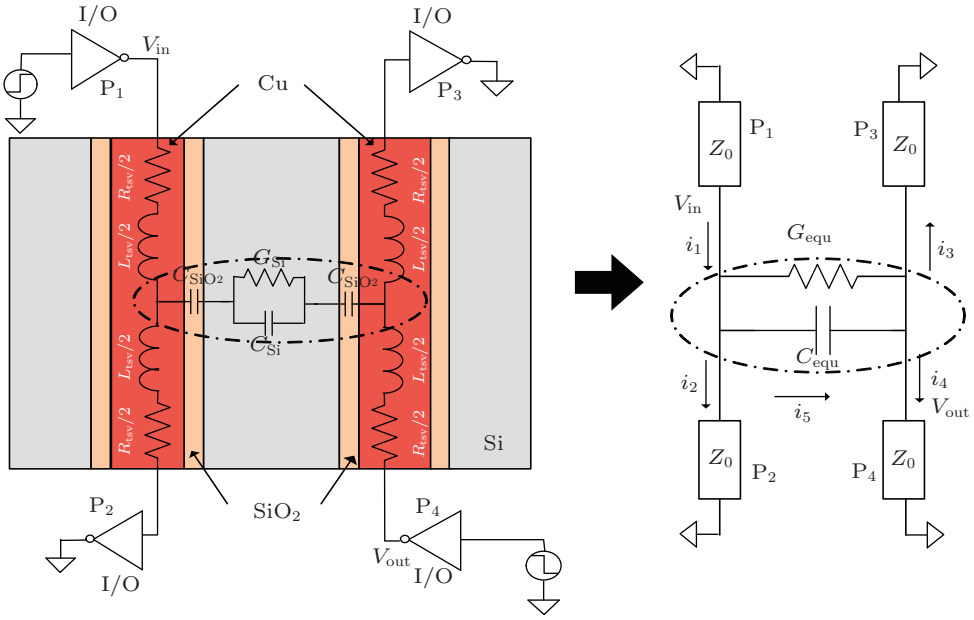



**Fig. 1.** (color online) Equivalent lump electrical model and simplified coupling transfer path for TSV-to-TSV structure.

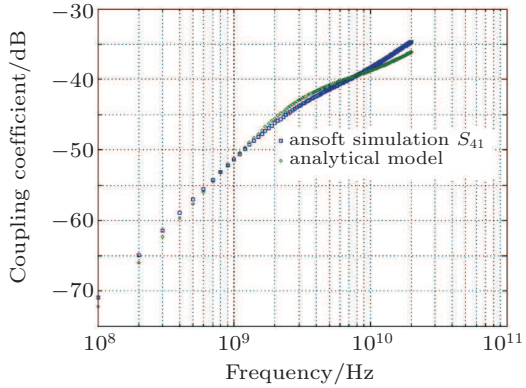



**Fig. 2.** (color online) Comparison of $S_{41}$ obtained from the proposed analytical model and the 3D field simulator, where $r_{via} = 2.5$ μm, $l_{tsv} = 50$ μm, $t_{ox} = 500$ nm, $p_{tsv} = 20$ μm, $\sigma_{Si} = 10$ S/m.

## 3. TSV-to-TSV crosstalk characterization

As mentioned in the previous section, the TSV-to-TSV coupling has a unique channel coupling characteristic. The TSV channel composed of the insulator dielectric and the silicon substrate shows different coupling impedances in the entire frequency domain. To further study and optimize the TSV crosstalk noise, the proposed analytical model is used to investigate the impact of various design parameters on the coupling coefficient in the frequency range from 100 MHz to 20 GHz, where all ports are terminated with a resistance of 50 Ω.

Figure 3 shows the variation of coupling coefficient $S_{41}$ with the thickness of the insulator layer in the entire frequency range of interest. Since the equivalent resistance and capacitance of the silicon substrate are 8 fF and 1314 Ω, respectively, the resistive coupling is the domain coupling path of the substrate in the low frequency range (< 1 GHz), then the channel impedance $Z_C$ can be model as a series connection of $R_{Si}$ and $C_{SiO2}$. Ignore the variation of the silicon conductivity, then the insulator layer plays a determined role in the TSV low-frequency coupling noise. When the thickness of the insulator layer increases from 100 nm to 500 nm, the low-frequency coupling coefficient decreases by an average of 13 dB. It is expected that the high-frequency coupling coefficient is not sensitive to the variation of the insulator thickness.

Figure 4 shows the variation of the peak crosstalk noise with the thickness of the insulator layer when a 1.0 V excited signal is input to port 1. Because the insulator capacitance is a determined factor in the low-frequency TSV channel impedance, the increased insulator thickness leads to a higher coupling impedance and a lower crosstalk noise. When the insulator thickness increases from 100 nm to 300 nm and 500 nm, the peak noise of 100 MHz signal decreases by 92.9 mV and 127.8 mV, respectively. The peak noise becomes less sensitive to the insulator thickness with the increase of the signal frequency, the peak noise of 10 GHz signal only reduces by about 5 mV. Here, the 1X inverter is used as the I/O driver, which can be modeled as an output resistance $R_s$ (∼ 3.16 kΩ) connected to supply the voltage and an input capacitance $C_0$ (∼ 0.45 fF) connected to the ground.[16]

Increasing the distance between the aggressor wire and the victim wire is a common approach to suppress the crosstalk noise in the conventional on-chip interconnects design.[17,18] However, this method is not effective for the TSV-to-TSV coupling due to the limitation of the insulation dielectric. As shown in Fig. 5, the channel coupling impedance $Z_C$ is mainly determined by the insulator capacitance $C_{SiO2}$ in the low-frequency range (< 1 GHz), therefore increasing the distance between TSVs has no significant impact on the coupling

coefficient. However, with the further increase in the signal frequency, capacitive coupling $C_{Si}$ becomes the domain coupling path inside the substrate; the coupling impedance $Z_C$ is then the sum of $C_{Si}$ and $C_{SiO2.}$ Additionally, $C_{Si}$ is smaller than $C_{SiO2}$, and thus the coupling impedance $Z_C$ is mainly determined by the substrate capacitance. When the TSV pitch is increased from 10 μm to 40 μm, the coupling coefficient of 10 GHz signal decreases by about 6 dB.

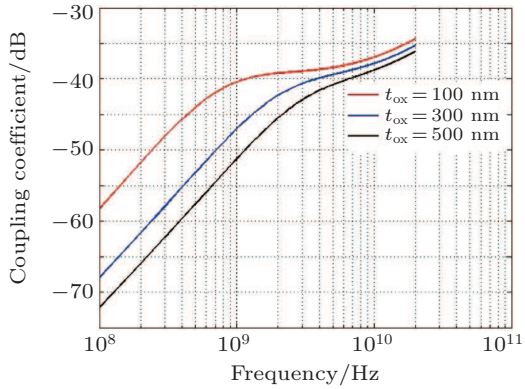



**Fig. 3.** (color online) Coupling coefficient $S_{41}$ versus the thickness of the insulator layer in the entire frequency range of interest, where $r_{via} = 2.5$ μ, $l_{tsv} = 50$ μm, $p_{tsv} = 20$ μm, $\sigma_{Si} = 10$ S/m.

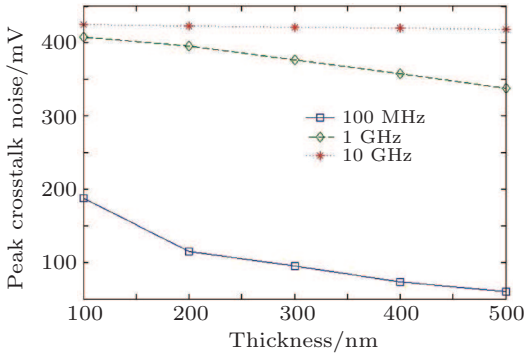



**Fig. 4.** (color online) Peak crosstalk noise versus the thickness of the insulator layer when the signal frequency is 100 MHz, 1 GHz, and 10 GHz.

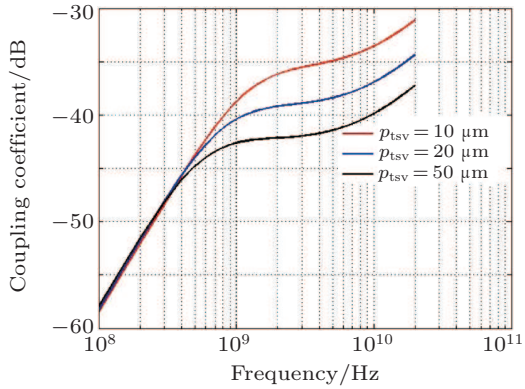



**Fig. 5.** (color online) Coupling coefficient $S_{41}$ versus the TSV pitch in the entire frequency range of interest, where $r_{via} = 2.5$ μm, $l_{tsv} = 50$ μm, $t_{ox} = 100$ nm, $\sigma_{Si} = 10$ S/m.

The peak crosstalk noise shown in Fig. 6 verifies the above analysis. When the TSV pitch increases from 10 μm to 20 μm and 50 μm, the peak crosstalk noise of 10 GHz signal decreases by 22.7 mV and 50.4 mV, respectively. While the variation of the crosstalk noise of 100 MHz signal with the TSV pitch can be neglected.

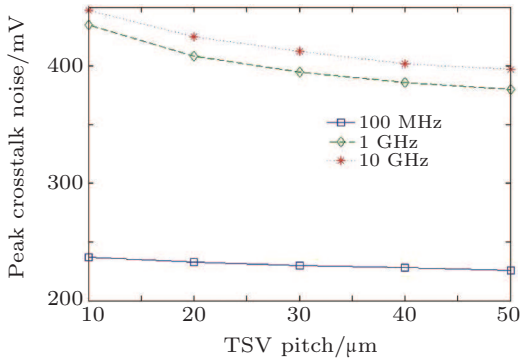



**Fig. 6.** (color online) Peak crosstalk noise versus TSV pitch when the frequency of the excited signal is 100 MHz, 1 GHz, and 10 GHz.

The height of the TSV is set by the thickness of the dies in the 3D stack, which is a critical design parameter for the TSV-to-TSV coupling. Figure 7 shows the variation of the coupling coefficient with the TSV height in the entire frequency range of interest. Since $C_{Si}$ and $C_{SiO2}$ are proportional to the TSV height, as the TSV height increases, the coupling coefficient significantly increases. When the TSV height increases from 15 μm to 25 μm and 50 μm, the coupling coefficient increases by averages of 4.3 dB and 10.1 dB, respectively.

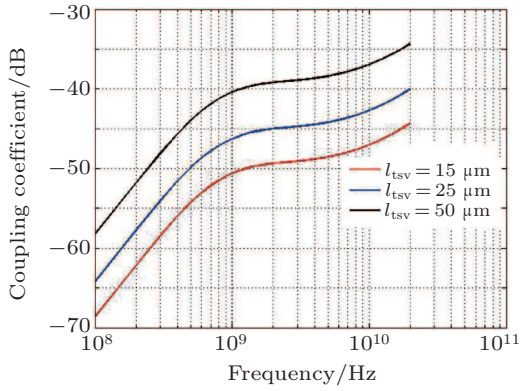



**Fig. 7.** (color online) Coupling coefficient $S_{41}$ versus the TSV height in the entire frequency range of interest, where $r_{via} = 2.5$ μm, $t_{ox} = 100$ nm, $p_{tsv} = 20$ μm, $\sigma_{Si} = 10$ S/m.

Another critical design parameter for the TSV-to-TSV coupling is the electrical conductivity $\sigma_{Si}$, which is mainly determined by the doping concentrations in the silicon substrate. Figure 8 shows the variation of the coupling coefficient with the silicon conductivity. Here, the lightly doped (low conductivity) substrate is usually used to fabricate low cost and low performance devices like memory, while the heavily doped bulk (high conductivity) is mostly adopted in high performance chips like processors.[19] Since the channel impedance is dominated by the capacitance of the insulator layer, it is observed that increasing the silicon conductivity

may have little impact on the TSV low-frequency coupling coefficient. However, the coupling coefficient dramatically increases with the increase of the silicon conductivity in the high-frequency range. It means that high performance devices suffer from more TSV high-frequency noise.

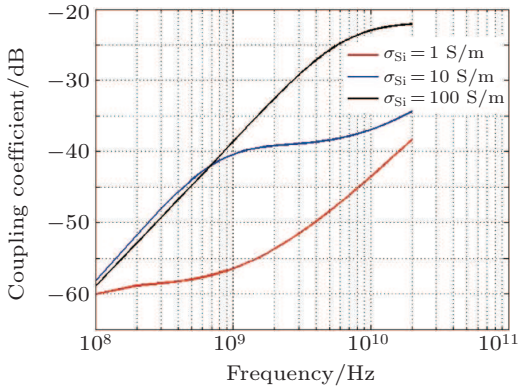



**Fig. 8.** (color online) Coupling coefficient $S_{41}$ versus the silicon conductivity in the entire frequency range of interest, where $r_{via} = 2.5$ μm, $l_{tsv} = 50$ μm, $t_{ox} = 100$ nm, $p_{tsv} = 20$ μm.

## 4. TSV-to-TSV crosstalk optimization

Due to the rapid increase of the signal frequency and the fine pitch integration with TSVs for a smaller form factor, the TSV-to-TSV crosstalk noise has become a serious reliability issue in 3D ICs design and optimization. Increasing the distance between TSVs is not an effective method to reduce the TSV induced noise as discussed in the previous sections; therefore, it is necessary to employ new techniques to suppress the coupling noise.

As illustrated in Eq. (2), the output crosstalk noise is inversely proportional to the terminal impedances of the I/O drivers; a decreased driver impedance leads to lower output noise. Figure 9 shows the variation of the coupling coefficient with the terminal impedance, as the terminal impedance decreases, the coupling coefficient between TSVs significantly decreases. When the terminal impedance decreases from 5000 Ω to 50 Ω, the coupling coefficient of 1 GHz signal decreases from −20 dB to −40 dB. For the I/O driver in TSV-based 3D ICs, increasing the driver size is an effective approach to decrease the output impedance of the I/O driver. Figure 10 compares the peak crosstalk noise of TSVs with different sized inverters. It is observed that the peak noise is reduced by about 73 mV and 241 mV when inverter size varies from 1X to 3X and 10X.[20]

Another effective approach to suppress the TSV induced noise is shielding, including via shielding, guard rings, and silicon on insulator. Figure 11 shows an HFSS structure of via shielding and the *S*-parameter simulation results. Since eight ground TSVs cutoff the coupling path through the silicon substrate, the coupling effect between the aggressor signal and the victim signal is significantly reduced, the full-band coupling coefficient decreases by an average of 10.8 dB. Transient response results shown in Fig. 11 also verify the effectiveness of the proposed approach. When via shielding is adopted, the peak crosstalk noise decreases from 404 mV to 25 mV, which corresponds to a 379 mV improvement in the peak noise observed.

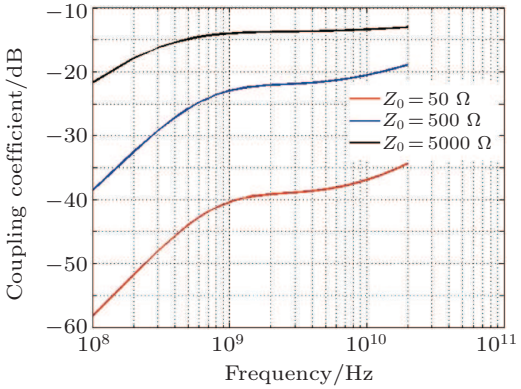



**Fig. 9.** (color online) Coupling coefficient $S_{41}$ versus the terminal impedance in the entire frequency range of interest, where $r_{via} = 2.5$ μm, $l_{tsv} = 50$ μm, $t_{ox} = 100$ nm, $p_{tsv} = 20$ μm, $\sigma_{Si} = 10$ S/m.

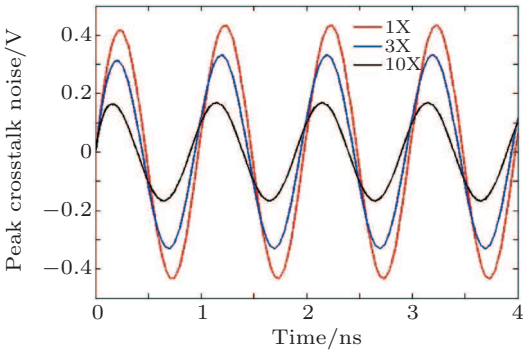



**Fig. 10.** (color online) Peak crosstalk noise of 1 GHz excited signal when the size of the inverter as the driver is 1X, 3X, and 10X.

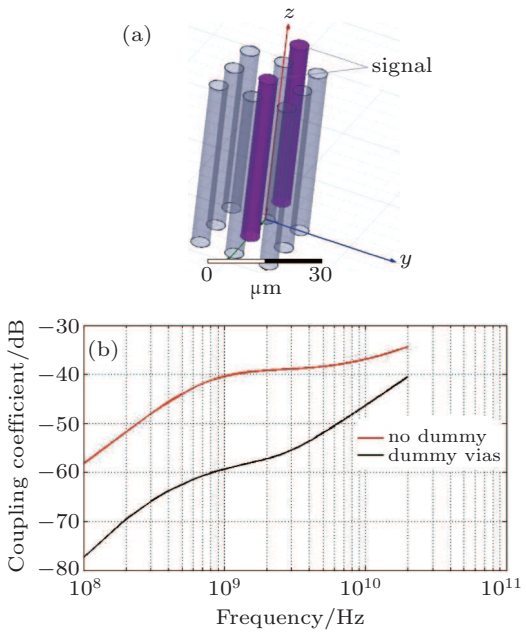



**Fig. 11.** (color online) (a) Via shielding structure for HFSS simulation, (b) coupling coefficient $S_{41}$ versus via shielding, where $r_{via} = 2.5$ μm, $l_{tsv} = 50$ μm, $t_{ox} = 100$ nm, $p_{tsv} = 20$ μm, $\sigma_{Si} = 10$ S/m.

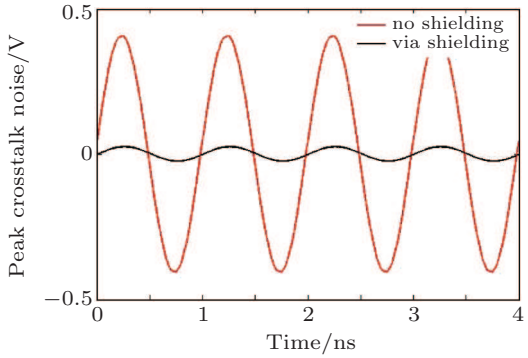



**Fig. 12.** (color online) Peak crosstalk noise of 1 GHz excited signal when the via shielding is adopted.

To further demonstrate the effect of the proposed optimized approaches, Table 1 lists the improvement ratios for peak crosstalk noise acquired with different noise isolation techniques. It is observed that 59.7% and 93.8% reductions in coupling noise are obtained with driving sizing and via shielding, respectively. The improvement ratio is higher than that of the p+ guard rings (38.7%) and the deep n-well guard rings (51.0%), but lower than that of the coaxial TSV design (98.5%). The coaxial TSV appears to be the best solution for noise reducing, however, the immature technology and larger dimensions restrict its usage in 3D integration. The proposed crosstalk model and the optimization techniques facilitate the management of noise tolerance budgets in TSV-based 3D ICs to achieve high noise immunity.

**Table 1.** Noise improvement ratio comparison among different noise isolation techniques.

| Isolation technique | Driving sizing | Via shielding | P+ guard ring[21] | Deep n-well guarding ring[21] | Coaxial TSV[22] |
|---|---|---|---|---|---|
| Improvement ratio | 59.7% | 93.8% | 38.7% | 51.0% | 98.5% |

## 5. Conclusion

Based on the frequency dependent equivalent electrical parameters, an analytical crosstalk model to capture the TSV induced noise is established and validated with the HFSS simulation results. By using the proposed model, the impact of various design parameters including insulator dielectric, via pitch, via height, and silicon conductivity on the crosstalk noise is investigated. Two approaches are proposed to alleviate the TSV noise, namely driver sizing and via shielding, and the SPICE results show 241 mV and 379 mV reductions in the peak noise voltage, respectively. The results presented in this paper are useful for the development of noise-aware design guidelines and tools.

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