Reduction of signal reflection along through silicon via channel in high-speed three-dimensional integration circuit*

Liu Xiao-Xian(刘晓贤)†, Zhu Zhang-Ming(朱樟明), Yang Yin-Tang(杨银堂), Wang Feng-Juan(王凤娟), and Ding Rui-Xue(丁瑞雪)

Microelectronics School, Xidian University, Xi'an 710071, *China*

(Received 21 May 2013; revised manuscript received 18 July 2013; published online 24 January 2014)

The through silicon via (TSV) technology has proven to be the critical enabler to realize a three-dimensional (3D) gigscale system with higher performance but shorter interconnect length. However, the received digital signal after transmission through a TSV channel, composed of redistribution layers (RDLs), TSVs, and bumps, is degraded at a high data-rate due to the non-idealities of the channel. We propose the Chebyshev multisection transformers to reduce the signal reflection of TSV channel when operating frequency goes up to 20 GHz, by which signal reflection coefficient (S_{11}) and signal transmission coefficient (S_{21}) are improved remarkably by 150% and 73.3%, respectively. Both the time delay and power dissipation are also reduced by 4% and 13.3%, respectively. The resistance-inductance-conductance-capacitance (RLGC) elements of the TSV channel are iterated from scattering (S)-parameters, and the proposed method of weakening the signal reflection is verified using high frequency simulator structure (HFSS) simulation software by Ansoft.

Keywords: three-dimensional integrated circuit, through silicon via channel, signal reflection, S-parameters

PACS: 84.30.–r, 84.30.Bv **DOI:** 10.1088/1674-1056/23/3/038401

1. Introduction

Moore's law and its developments still seem to be evolving in recent years. However, scaling the minimum feature size of the transistor has slowed down due to the limitations of interconnect performance, leakage power consumption, process variation, and cost for further advancement.[1–3] Three-dimensional (3D) interconnect, which allows the basic electronic components to be stacked in the third dimension, is a promising alternative solution to overcome those limitations of the component miniaturization dictated by the traditional Moore's law. Through-silicon-via (TSV) is the core technology to achieve 3D interconnect, which electrically connects homogeneous or heterogeneous chips stacked vertically together. Because of the main distinctive feature, the using of TSVs has tremendous advantages, such as the realization of electronic systems with very high packaging efficiency, higher system bandwidth, and lower power consumption. It also increases the number of I/Os and enables the system to transmit a large quantity of data simultaneously at a high signal transmission speed.[4–7]

For a practical 3D circuit, the TSV channel includes not only TSVs, but also bumps and redistribution layers (RDLs). Bumps provide a joint between stacked chips. The RDL is a metal interconnect which provides horizontal interconnections between stacked dies.[8] As the operating frequency goes up to a gigahertz range, the unique non-ideal properties of the TSV channel result in various signal integrity (SI) problems, such as signal reflection, noise, which have an ever-growing adverse effect on the reliability and performance of the circuit. There have been various studies on analyzing the signal performance of a high-speed TSV channel.[1,3,9] However, the detrimental effect of signal reflection in the TSV channel has not attracted much attention so far. Scalable electrical models of TSVs, bumps and RDLs, acting as design parameters such as geometric and material information, at up to 20 GHz, were presented in Ref. [1]. However, the analysis of the corresponding relationship between signal reflection and those electrical models has not been conducted, and no method of reducing the channel loss has been proposed. Kim *et al*[3] measured and analyzed the electrical characteristics of a high-speed TSV channel, but they believed that the signal reflection in TSV channel should be ignored. Cui *et al*[9] used the multilayer RDLs to offset the extra insertion loss brought by TSV insertion. However, they obtained their results in experiment but did not perform the numerical analysis correspondingly. Therefore, there is still room for improving the signal transmission performances along the high-speed TSV channel.

In this paper, a Chebyshev multisection matching transformer is proposed to reduce the signal reflection in the TSV channel when the frequency is 20 GHz. We choose coplanar wave guides with finite width (FW-CPW) as the RDL. Correspondingly, ground-signal-ground (GSG) type TSVs are needed. The RLGC elements per unit length of RDLs and TSVs, which are used to calculate the characteristics of

*Project supported by the National Natural Science Foundation of China (Grant No. 61204044).

†Corresponding author. E-mail: liudou132@163.com

© 2014 Chinese Physical Society and IOP Publishing Ltd

Chebyshev multisection matching transformers, are acquired from S-parameters simulated by Ansoft's HFSS. Reduction of signal reflection with Chebyshev multisection matching transformers is verified by HFSS. What is more, the time delay and power dissipation of the TSV channel are calculated, which identify that the Chebyshev multisection matching transformers are effective to improve the signal performance of TSV channel.

The rest of the paper is composed of the following sections. Section 2 identifies the electrical properties of RDLs and GSG-type TSVs. Calculation of the Chebyshev multisection matching transformers is given in section 3. Section 4 shows the time delay and power dissipation of the TSV channel. Conclusions are given in section 5.

2. Electrical properties of RDLs and GSG-type TSVs

2.1. Electrical properties of RDLs

Depending on the orientations of different stacked circuits, there are multiple approaches to achieving 3D interconnect, including face-to-face (F2F), face-to-back (F2B) or back-to-face (B2F). In this paper, we have chosen face-to-back (F2B) 3D technology as shown in Fig. 1.

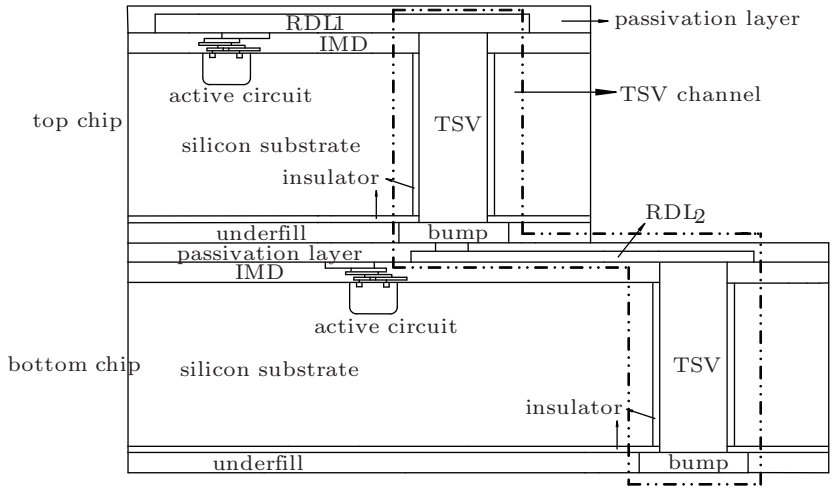


Fig. 1. Cross-sectional view of vertical interconnects through the stacked dies.

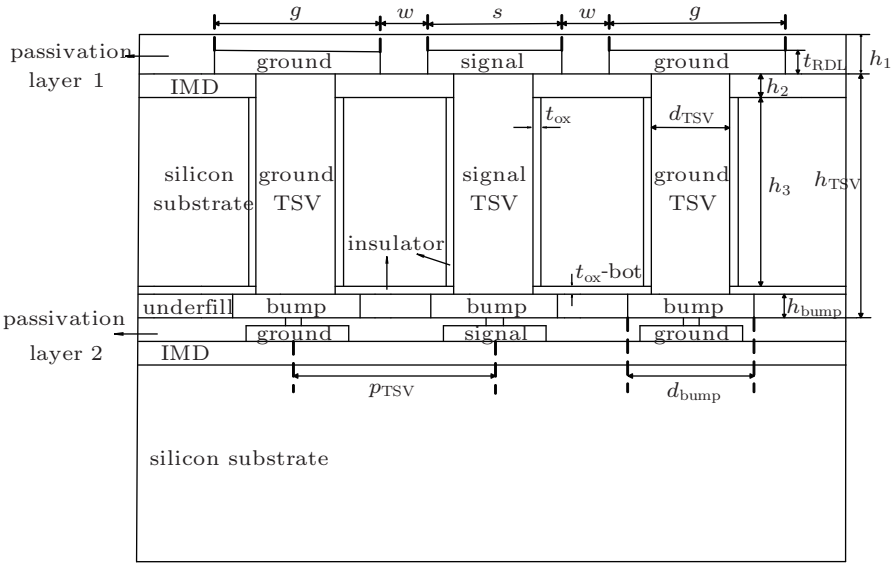


Fig. 2. Vertical-sectional view of vertical interconnects through the stacked dies.

Coplanar waveguide (CPW) is a type of planar transmission line used in microwave integrated circuit (MIC) as well as in monolithic microwave integrated circuit (MMIC). A conventional FW-CPW on a dielectric substrate consists of a center strip conductor with semi-infinite ground planes on either side as shown in Fig. 2. This structure supports a quasi-TEM mode of propagation. Compared with micro stripe line (MSL), CPW fabricated on the lossy low-resistivity silicon (LRS) has almost the lowest transmission loss at up to about 200 GHz, for much more electromagnetic field of MSL is trapped within the silicon substrate and electromagnetic waves suffer higher dielectric loss contributed by LRS.[10]

The design parameters of RDLs are shown in table 1. RDL 1 and RDL 2 are located on the top chip and bottom chip respectively. They are connected by three TSVs. The material used for the passivation layer, RDL and IMD are FR-4, Cu and SiO_2, respectively.

Table 1. Design parameters of RDL.

Parameter	Symbol	RDL 1	RDL 2
Signal RDL width	s/μm	15	5
Ground RDL width	g/μm	20	15
Space between RDL	w/μm	10	17.5
RDL thickness	t_{RDL}/μm	3	2
Passivation layer thickness	h_1/μm	5	4
IMD thickness	h_2/μm	3	2
Silicon substrate thickness	h_3/μm	25	30
Relative permittivity of Passivation layer	$\varepsilon_{\mathrm{r,pl}}$	4.4	
Relative permittivity of IMD	$\varepsilon_{\mathrm{r,IMD}}$	4	
Relative permittivity of Silicon substrate	$\varepsilon_{\mathrm{r,Si}}$	11.8	
RDL length	L/μm	200	

With the research of signal reflection along the TSV channel, a thorough understanding of the electrical properties of RDLs and TSVs are vitally necessary. In this paper, we employ a 3D fullwave EM simulator (Ansoft's HFSS), which is based on the finite element method (FEM) to differentially solve Maxwell's equations for arbitrary structures. S-parameters are obtained by HFSS simulation, and converted into an ABCD matrix as

$$\begin{pmatrix} A & B \\ C & D \end{pmatrix} = \begin{bmatrix} \dfrac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{2S_{21}} & Z_n\dfrac{(1+S_{11})(1+S_{22})-S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}} \\ \dfrac{1}{Z_n}\dfrac{(1-S_{11})(1-S_{22})-S_{12}S_{21}}{2S_{21}} & \dfrac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{2S_{21}} \end{bmatrix}, \tag{1}$$

where Z_n is the port impedance that is assumed to be 50 Ω. The ABCD matrix for a lossy transmission line is[11]

$$\begin{pmatrix} A & B \\ C & D \end{pmatrix} = \begin{pmatrix} \cosh(\gamma L) & Z_0\sinh(\gamma L) \\ \sinh(\gamma L)/Z_0 & \cosh(\gamma L) \end{pmatrix}, \tag{2}$$

where L is the length of transmission line, γ and Z_0 are the propagation constant of signal waveform and the characteristic impedance of the line, respectively, which can be deduced directly from the ABCD matrix

$$\gamma = \cosh^{-1}(A)/L, \tag{3}$$

$$Z_0 = \sqrt{B/C}. \tag{4}$$

With the definitions of γ and Z_0, we can obtain

$$R_{\mathrm{u}} + \mathrm{j}wL_{\mathrm{u}} = \gamma Z_0, \quad G_{\mathrm{u}} + \mathrm{j}wC_{\mathrm{u}} = \gamma/Z_0,$$

where j is the imaginary unit; R_{u}, L_{u}, G_{u}, and C_{u} are the resistance, inductance, conductance, and capacitance per unit length of the line. These RLGC elements per unit length are given as

$$R_{\mathrm{u}} = \mathrm{Re}(\gamma Z_0), \tag{5}$$

$$L_{\mathrm{u}} = \mathrm{Im}(\gamma Z_0)/w, \tag{6}$$

$$G_{\mathrm{u}} = \mathrm{Re}(\gamma/Z_0), \tag{7}$$

$$C_{\mathrm{u}} = \mathrm{Im}(\gamma/Z_0)/w. \tag{8}$$

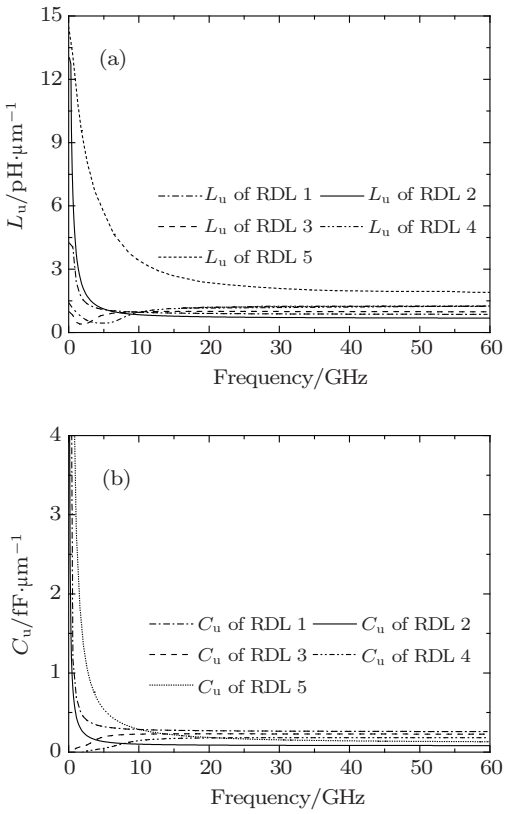


Fig. 3. Inductances (a) and capacitances (b) per unit length of RDLs used in this paper.

Simulation results are shown in Fig. 3, where RDL 3,

RDL 4, and RDL 5 are FW-CPWs used for Chebyshev multisection matching transformers. Parasitic extraction of RDLs should be composed of not only serial inductance and resistance, but also silicon substrate with the effects of capacitance and conductance. These elements are necessary to calculate the performances of the TSV channel, including time delay and power dissipation.

2.2. Properties of GSG-type TSVs

A two- or three-TSV system is the basic unit used in a 3D IC for signal transmission. It is important to study those basic units to understand fully the TSV characteristics. The high-speed single-ended GSG type TSV is analyzed in this paper. Figure 2 also shows the structures of a signal TSV, two ground TSVs and bumps with the via-middle process in 45 nm technologies. Two ground TSVs are used as the returning current paths. TSVs are surrounded by a thin layer of insulator (SiO_2 in this paper) which serves as the isolation layer between the silicon (Si) substrate and TSV. The isolation dielectric is surrounded by a depletion region when the TSV gate bias voltage increases. In this paper, we neglect the parasitic effect of the depletion region. The design parameters of TSV are shown in table 2.

Table 2. Design parameters of TSV.

Parameter	Symbol	Value
TSV diameter	$d_{\mathrm{TSV}}/\mu\mathrm{m}$	5
TSV height	$h_{\mathrm{TSV}}/\mu\mathrm{m}$	25
Underfill height	$h_{\mathrm{underfill}}/\mu\mathrm{m}$	3
Bump diameter	$d_{\mathrm{bump}}/\mu\mathrm{m}$	10
Bump height	$h_{\mathrm{bump}}/\mu\mathrm{m}$	3
Relative permittivity of underfill	$\varepsilon_{\mathrm{r,underfill}}$	4.3
TSV-to-TSV pitch	$p_{\mathrm{TSV}}/\mu\mathrm{m}$	27.5
Bottom SiO_2 thickness	$t_{\mathrm{ox_bottom}}/\mu\mathrm{m}$	0.5
Conductivity of silicon	$\sigma_{\mathrm{Si}}/\mathrm{S\cdot m}$	10
Insulator thickness	$t_{\mathrm{ox}}/\mu\mathrm{m}$	0.5
loss tangent of silicon	$\tan\delta_{\mathrm{c,Si}}$	0.004

GSG-type TSVs are modeled with the equivalent circuit with design parameters and material properties in Refs. [12]–[14]. However, parasitic effects of bumps, underfill and the IMD layer are missed, of which the influences increase as operating frequency increases. The S-parameters of TSV with and without bumps are shown in Fig. 4, from which we can find that the influence of bumps is notable. Therefore, bumps are essential components that should be considered in the case with the TSV, and so should the parasitic effect of underfill which acts as the bonding layer, especially in high-speed circuits with operating frequencies up to gigascale range. Although the parasitic effects of IMD, bumps and underfill are all considered in Ref. [1], ground-signal (GS) type TSVs are employed. There are no accurate electrical models for GSG-type TSVs yet. In the fast-switching circuits produced by deep-submicrometer technologies today, the GSG-type TSV pair had better to be treated as a lossy transmission line.[2] Hence, the electrical properties of TSV could be deduced by theories of the transmission line above. The RLGC elements per unit length of TSVs are shown in Fig. 5.

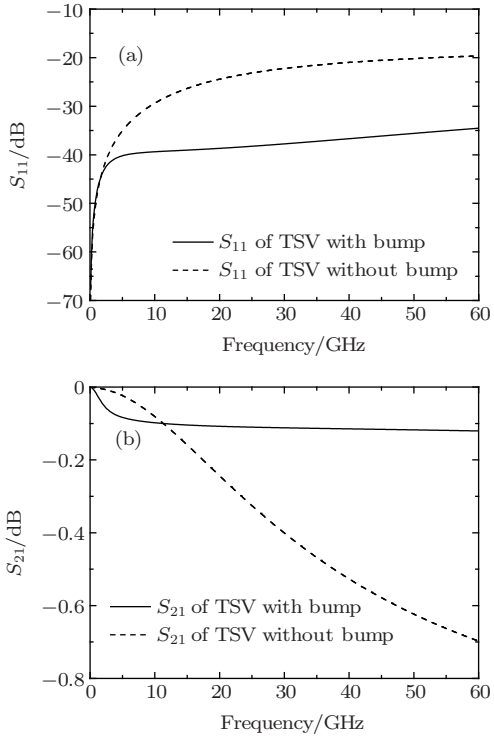


Fig. 4. S-parameters of TSVs with and without bumps: (a) S_{11}, (b) S_{21}.

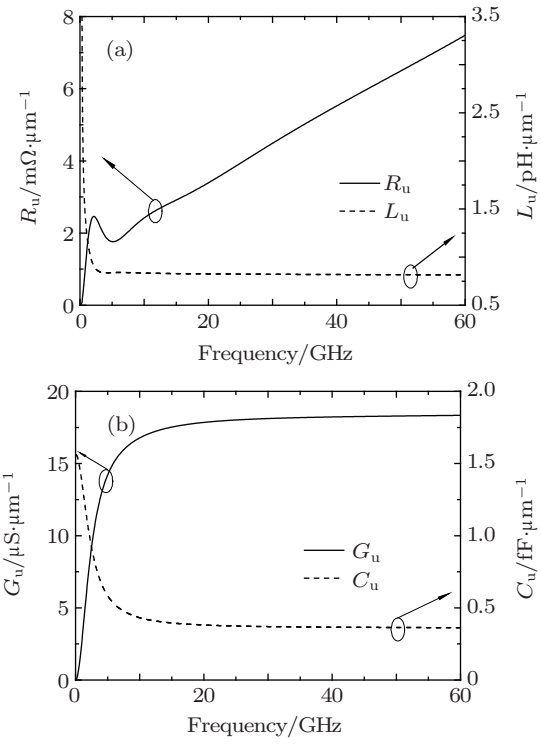


Fig. 5. Results of RLCG per unit length of TSVs: (a) R_{u}, L_{u}; (b) G_{u}, C_{u}.

3. Chebyshev multisection matching transformers

In order to reduce the insertion loss of the TSV channel, the Chebyshev multisection matching transformers are employed. This method is generally referred to as the theory of small reflections, based on which the Chebyshev multisection transformers are designed by equating $\Gamma(\theta)$ to a Chebyshev polynomial that has the optimum characteristics needed for this type of transformer. We will first discuss the properties of a multisection transformer and Chebyshev polynomials. Then, the design procedure for Chebyshev multisection matching transformers is derived.

3.1. Multisection transformer

Consider the multisection transformer shown in Fig. 6, which consists of N equal-length sections of transmission lines. Partial reflection coefficients can be defined at each junction as follows:[15]

$$\Gamma_0 = \frac{Z_1 - Z_0}{Z_1 + Z_0},$$
$$\Gamma_n = \frac{Z_{n+1} - Z_n}{Z_{n+1} + Z_n},$$
$$\Gamma_N = \frac{Z_L - Z_N}{Z_L + Z_N}.$$

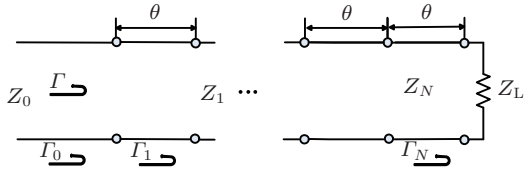


Fig. 6. Partial reflection coefficients on multisection transformer.

We assume that all Z_n increase or decrease monotonically across the transformer and that Z_L is real. We further assume that the transformer can be made symmetrical, so that $\Gamma_0 = \Gamma_N$, $\Gamma_1 = \Gamma_{N-1}$, $\Gamma_2 = \Gamma_{N-2}$, etc. The overall reflection coefficient Γ can be written in the form of a finite Fourier cosine series in the frequency domain (θ) as[15]

$$\Gamma(\theta) = 2\mathrm{e}^{-\mathrm{j}N\theta}[\Gamma_0 \cos N\theta + \Gamma_1 \cos(N-2)\theta + \cdots + \Gamma_n \cos(N-2n)\theta + \cdots]. \quad (9)$$

3.2. Chebyshev polynomials

The n-th-order Chebyshev polynomial is a polynomial of degree n, denoted by $T_n(x)$. The first four Chebyshev polynomials are[15]

$$T_1(x) = x, \quad (10a)$$
$$T_2(x) = 2x^2 - 1, \quad (10b)$$
$$T_3(x) = 4x^3 - 3x, \quad (10c)$$
$$T_4(x) = 8x^4 - 8x^2 + 1. \quad (10d)$$

Higher order polynomials can be found using the following recurrence formula:[15]

$$T_n(x) = 2xT_{n-1}(x) - T_{n-2}(x). \quad (11)$$

For the first three Chebyshev polynomials, $|T_n(x)| \le 1$ when $-1 \le x \le 1$. In this range the Chebyshev polynomials oscillate between ± 1. This is the equal-ripple property, and this region will be mapped to the passband of the matching transformer. Let $x = \cos\theta$ for $|x| < 1$, then it will be shown that the Chebyshev polynomials can be expressed as[15]

$$T_n(\cos\theta) = \cos n\theta. \quad (12)$$

We desire equal ripple for the passband response of the transformer, so it is necessary to map θ_m to $x = 1$ and $\pi - \theta_m$ to $x = -1$, where θ_m and $\pi - \theta_m$ are the lower and upper edges of the passband, respectively. This can be accomplished by replacing $\cos\theta$ in Eq. (12) with $\cos\theta / \cos\theta_m$ as[15]

$$T_n\left(\frac{\cos\theta}{\cos\theta_m}\right) = T_n(\sec\theta_m \cos\theta) = \cos n\left[\cos^{-1}\left(\frac{\cos\theta}{\cos\theta_m}\right)\right]. \quad (13)$$

Then $|\sec\theta_m \cos\theta| \le 1$ for $\theta_m < \theta < \pi - \theta_m$, so $|T_n(\sec\theta_m \cos\theta)| \le 1$ over this same range. Because $\cos^n\theta$ can be expanded into a sum of terms in the form of $\cos(n-2m)\theta$, the Chebyshev polynomials of Eq. (10) can be rewritten in the following useful form:[15]

$$T_1(\sec\theta_m \cos\theta) = \sec\theta_m \cos\theta, \quad (14a)$$
$$T_2(\sec\theta_m \cos\theta) = \sec^2\theta_m (1 + \cos 2\theta) - 1, \quad (14b)$$
$$T_3(\sec\theta_m \cos\theta) = \sec^3\theta_m (\cos 3\theta + 3\cos\theta) - 3\sec\theta_m \cos\theta, \quad (14c)$$
$$T_4(\sec\theta_m \cos\theta) = \sec^4\theta_m (\cos 4\theta + 4\cos 2\theta + 3) - 4\sec^2\theta_m (\cos 2\theta + 1) + 1. \quad (14d)$$

These results can be used to design matching transformers with up to four sections.

3.3. Design of Chebyshev multisection matching transformer

We can now synthesize a Chebyshev equal-ripple passband by making $\Gamma(\theta)$ proportional to $T_N(\sec\theta_m \cos\theta)$, where N is the number of sections in the transformer. Thus, using Eq. (9), we have[15]

$$\Gamma(\theta) = 2\mathrm{e}^{-\mathrm{j}N\theta}[\Gamma_0 \cos N\theta + \Gamma_1 \cos(N-2)\theta + \cdots + \Gamma_n \cos(N-2n)\theta + \cdots] = A\mathrm{e}^{-\mathrm{j}N\theta} T_N(\sec\theta_m \cos\theta), \quad (15)$$

where the last term in the series of Eq. (15) is $(1/2)\Gamma_{N/2}$ for even N and $\Gamma_{(N-1)/2\cos\theta}$ for odd N. We can find the constant A by letting $\theta = 0$, correspond to zero frequency. Thus[15]

$$\Gamma(0) = \frac{Z_L - Z_0}{Z_L + Z_0} = AT_N(\sec\theta_m), \tag{16}$$

so we have

$$A = \frac{Z_L - Z_0}{Z_L + Z_0}\frac{1}{T_N(\sec\theta_m)}. \tag{17}$$

If the maximum allowable reflection coefficient magnitude in the passband is Γ_m, then from Eq. (15) we will have $\Gamma_m = |A|$ since the maximum value of $T_n(\sec\theta_m\cos\theta)$ in the passband is unity. Then Eq. (17) gives[15]

$$T_N(\sec\theta_m) = \frac{1}{\Gamma_m}\left|\frac{Z_L - Z_0}{Z_L + Z_0}\right| \approx \frac{1}{\Gamma_m}\left|\ln\frac{Z_L}{Z_0}\right|. \tag{18}$$

In our paper, the GSG-type TSVs and RDL 2 on the bottom chip, which are connected in series, are treated as a load of RDL 1 on the top chip. Therefore, the load impedance is $Z_L = Z_{0TSV} + Z_{0RDL2}$, where Z_{0TSV} and Z_{0RDL2} are the characteristic impedances of TSV and RDL 2 respectively. By the above theory, a three-section Chebyshev transformer is designed, of which the subject is to match Z_L to a transmission line whose characteristic impedance is Z_{0RDL1}. The maximum reflection coefficient Γ_m is assumed to be 0.02 in this paper.

From Eq. (14c) with $N = 3$

$$\begin{aligned}\Gamma(\theta) &= 2e^{-j3\theta}(\Gamma_0\cos 3\theta + \Gamma_1\cos\theta)\\ &= Ae^{-j3\theta}T_3(\sec\theta_m\cos\theta).\end{aligned} \tag{19}$$

Then, $A = \Gamma_m = 0.02$. Using Eq. (14c) for T_3 gives

$$\begin{aligned}&2(\Gamma_0\cos 3\theta + \Gamma_1\cos\theta)\\ &= A\sec^3\theta_m(\cos 3\theta + 3\cos\theta) - 3A\sec\theta_m\cos\theta.\end{aligned} \tag{20}$$

Equating similar terms in $\cos(n\theta)$ gives the following results:

$$\cos 3\theta : 2\Gamma_0 = A\sec^3\theta_m, \quad \Gamma_0 = 0.0664;$$
$$\cos\theta : 2\Gamma_1 = 3A(\sec^3\theta_m - \sec\theta_m), \quad \Gamma_1 = 0.1429.$$

From symmetry, we also have that

$$\Gamma_3 = \Gamma_0 = 0.0664, \quad \Gamma_2 = \Gamma_1 = 0.1429.$$

Then the characteristic impedances are

$$n = 0 : \ln Z_1 = \ln Z_0 + 2\Gamma_0, \quad Z_1 = 66.24\ \Omega;$$
$$n = 1 : \ln Z_2 = \ln Z_1 + 2\Gamma_1, \quad Z_2 = 88.16\ \Omega;$$
$$n = 2 : \ln Z_3 = \ln Z_2 + 2\Gamma_2, \quad Z_3 = 117.33\ \Omega.$$

The characteristic impedances of the needed Chebyshev sections, RDL 3, RDL 4, RDL 5, are 66.24 Ω, 88.16 Ω, and 117.33 Ω, respectively. Consequently, the widths of signal lines of RDL3, RDL4, and RDL5 are 11 μm, 4.7 μm, 1.5 μm, respectively. The structure of the Chebyshev multisection transformer is shown in Fig. 7(b). Simulation results of S-parameters of the TSV channel with and without the Chebyshev transformer are shown in Fig. 8. Unlike the uniform RDL 1 in Fig. 7(a),

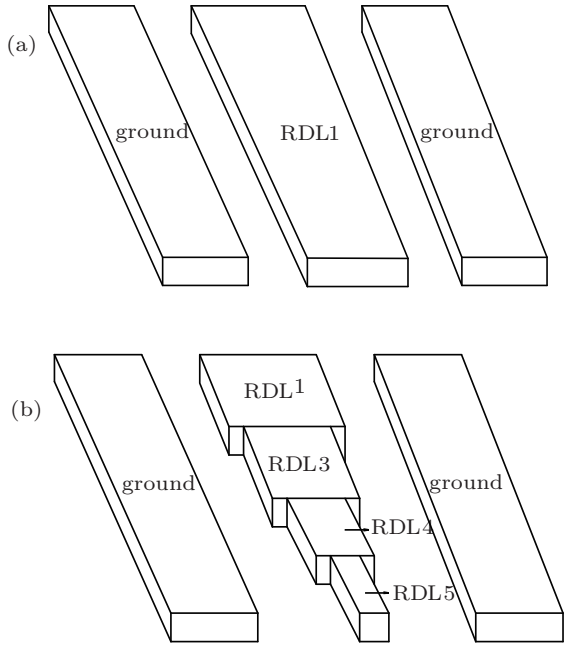


Fig. 7. Structures of RDLs on top chip (a) uniform RDL 1 before Chebyshev matching, (b) Chebyshev multisection matching transformers.

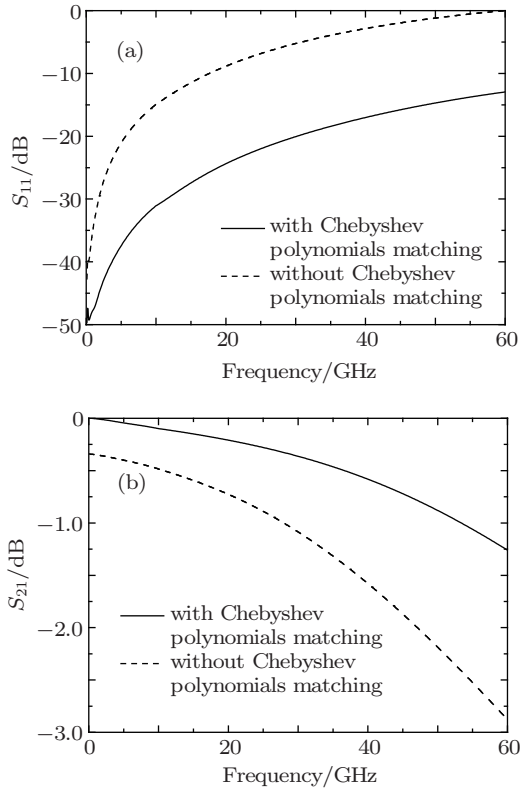


Fig. 8. Simulation results of S-parameters of TSV channel: (a) S_{11}, (b) S_{21}.

the Chebyshev multisection matching transformer weakens the signal reflection (S_{11}) in the TSV channel remarkably, S_{11} decreases from -10 dB to -25 dB, which shows 150% improvement, S_{21} of the TSV channel increases from -0.75 dB to -0.2 dB, which displays 73.3% improvement. Compared with uniform RDL 1 in Fig. 7(a), RDL 3, RDL 4, and RDL 5 in the Chebyshev transformer together constitute a tapered transmission line, as shown in Fig. 7(b). Therefore, no more area penalty is needed to achieve the matching.

4. Time delay and power dissipation of the TSV channel

4.1. Time Delay of the TSV channel

For a better illustration of the effect of the Chebyshev multisection matching transformers on signal timing, a comparative analysis of the time delay (TD) for the TSV channel is conducted. The time delay of a transmission line is the amount of time it takes for a signal to propagate over the entire length of the line, which can be determined from the equivalent circuit model of the transmission line as[16]

$$\mathrm{TD}=\sqrt{LC}, \tag{21}$$

where L is the total series inductance for the length of the line and C is the total shunt capacitance for the length of the line, obtained by the EM field simulations. Since the TSV is modeled as a lossy transmission line, the TD of TSV can also be calculated by Eq. (21).[2] Then the total TD of the TSV channel can be computed by

$$\mathrm{TD}_{\mathrm{total}} = \mathrm{TD}_{\mathrm{RDL}} + \mathrm{TD}_{\mathrm{TSV}}, \tag{22}$$

where $\mathrm{TD}_{\mathrm{RDL}}$ and $\mathrm{TD}_{\mathrm{TSV}}$ are the total time delay of RDLs and that of TSV, respectively. The inductances and capacitances per unit length of RDLs and TSV are obtained from Eqs. (6) and (8) as shown in Fig. 3. Before Chebyshev multisection transformer matching, the TD of the TSV channel in Fig. 1 is 5.417 ns, and it is 5.19 ns after matching. There is a 4.2% improvement of the time delay.

4.2. Power dissipation of the TSV channel

In practical 3D technology, the long interconnect and TSV channel are always driven by plenty of buffers, which can reduce the interconnect delay and power dissipation. Hence, power consumption in the TSV channel usually includes the power dissipations of interconnect, repeater, TSV, and logic gate. Considering the design parameters in our paper, we calculate the power consumption of the TSV channel including the effects of interconnect (RDLs) and TSV, only. The total power P_{total} is calculated from

$$P_{\mathrm{total}} = P_{\mathrm{CPW}} + P_{\mathrm{TSV}}, \tag{23}$$

where P_{CPW} and P_{TSV} are the power consumption of CPWs and that of TSV, respectively, and calculated as[17]

$$P_{\mathrm{TSV}} = \frac{\alpha}{2} C_{\mathrm{TSV}}(w)\, h_{\mathrm{TSV}} V_{\mathrm{dd}}^2 f, \tag{24}$$

$$P_{\mathrm{CPW}} = \frac{\alpha}{2} C_{\mathrm{RDL}}(w)\, L V_{\mathrm{dd}}^2 f, \tag{25}$$

where V_{dd}, α, and f are power supply voltage, operating frequency, and switching factor (or activity factor) respectively. The value of V_{dd} is 0.6 V in 45-nm CMOS technology.[17] The value of α can be taken to be 0.15, $C_{\mathrm{RDL}}(\omega)$ and $C_{\mathrm{TSV}}(\omega)$ respectively are the capacitances per unit length of the RDL and TSV, which vary with operating frequency as shown in Figs. 3(b) and 5(b), respectively.

For an RLCG line, Chebyshev multisection matching transformer reduces not only the propagation delay, but also the total power dissipation compared with for the case of uniform wire sizing. Simulation results show that the total power consumption of the TSV channel decreases from 43.95 μW to 38.2 μW after the Chebyshev matching. There is a 13.1% improvement of power dissipation of the TSV channel.

5. Conclusion

At low frequency, the loss for the TSV channel is caused mainly by the material loss of the silicon (Si) substrate due to its low resistivity. However, in a millimeter wave (mm-wave) frequency range, especially above 10 GHz, in addition to the insertion loss (S_{21}), the return loss (S_{11}) becomes significant due to impedance matching. These losses become a serious setback for the Si interposer in mm-wave applications. The Chebyshev multisection matching transformer is presented to weaken the signal reflection along the TSV channel which includes RDLs, TSVs, and bumps when the operating frequency is 20 GHz in this paper; S_{11} of the TSV channel decreases from -10 dB to -25 dB, which shows a 150% improvement of the signal reflection by exploring the Chebyshev matching. The RLGC elements of CPWs and TSV are acquired by HFSS simulation. What is more, there are 4% and 13.3% reductions of time delay and power dissipation, respectively. It can be seen that the Chebyshev multisection matching transformer is an effective way to lessen the signal integrity problems in high speed 3D ICs, without additional area penalty.

References

[1] Kim J, Pak J S, Cho J H, Song E, Cho J, Kim H, Song T, Lee J, Lee H, Park K, Yang S, Suh M S, Byun K Y and Kim J H 2011 *IEEE Trans. Compon. Pack. Manuf. Technol.* **1** 181

[2] Katti G, Michele S, Velenis D, Thangaraju S, Meyer K, Dehaene W and Beyne E 2011 *IEEE Electron Dev. Lett.* **32** 946

[3] Kim H, Cho J, Kim M, Kim K, Lee J, Lee H, Park K, Choi K, Bae H C, Kim H J and Kim J 2012 *IEEE Trans. Compon. Pack. Manuf. Technol.* **2** 1672

[4] Zhu Z M and Liu S B 2012 *Chin. Phys. B* **21** 028401

[5] Zhang Y, Dong G and Yang Y T 2013 *Acta Phys. Sin.* **62** 016601 (in Chinese)

[6] Yu Y, Zhang C and Han X J 2013 *Acta Phys. Sin.* **62** 020508 (in Chinese)

[7] Qian L B, Zhu Z M and Yang Y T 2011 *Chin. Phys. B* **20** 108401

[8] Lee M, Cho J, Kim J, Pak J S, Lee H, Lee J, Park K and Kim J H 2012 *Proceedings of* 62*th Electronic Components and Technology Conference (ECTC),* May 29–June 1, 2012, San Diego, America, p. 816

[9] Cui Q H, Sun X, Zhu Y H, Ma S L, Chen J, Miao M and Jin Y F 2011 *Proceeding of* 12*th Electronic Packaging Technology & High Density Packaging,* August 8–11, 2011, Shanghai, China, p. 1

[10] Hu S, Wang L, Xiong Y Z, Lim T G, Zhang B, Shi J L and Yuan X J 2011 *IEEE Trans. Compon. Pack. Manuf. Technol.* **1** 260

[11] Xu Z and Lu J Q 2011 *IEEE Electron Dev. Lett.* **32** 1278

[12] Lu K C, Horng T S, Li H H, Fan K C, Huang T Y and Lin C H 2012 *Proceedings of* 62*th Electronic Components and Technology Conference (ECTC)*, May 29–June 1, 2012, San Diego, America, p. 816

[13] Wang R, Charles G and Franzon P 2012 *Proceedings of* 3*D Systems Integration Conference (3DIC)* , January 31–Febrary 2, 2012, Osaka, Japan, p. 1

[14] Lim T G, Khoo Y M, Selvanayagam C S, Ho D S W, Li R, Zhang X W, Gao S and Yong X Z 2011 *Proceedings of* 61*th Electronic Components and Technology Conference (ECTC)*, May 32–June 3, 2011, Lake Buena Vista, America, p. 557

[15] David M P 2012 *Microwave Engineering* (4th edn.) (New York: John Wiley & Sons) pp. 256–259

[16] Hall S H, Hall G W and Call J 2000 *High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices* (New York: John Wiley& Sons)

[17] Davis J A and Meindl J D 2003 *Interconnect Technology and Design for Gig Scale Integration* (Netherlands: Springer) p. 184