High-efficiency S-band harmonic tuning GaN amplifier*

Cao Meng-Yi(曹梦逸)[a], Zhang Kai(张 凯)[a], Chen Yong-He(陈永和)[a], Zhang Jin-Cheng(张进成)[a], Ma Xiao-Hua(马晓华)[a)b)†], and Hao Yue(郝 跃)[a]

[a] *Key Laboratory for Wide Band-Gap Semiconductor Materials and Devices, School of Microelectronics, Xidian University, Xi'an* 710071, *China*
[b] *School of Technical Physics, Xidian University, Xi'an* 710071, *China*

(Received 3 June 2013; revised manuscript received 14 August 2013; published online 24 January 2014)

In this paper, we present a high-efficiency S-band gallium nitride (GaN) power amplifier (PA). This amplifier is fabricated based on a self-developed GaN high-electron-mobility transistor (HEMT) with 10 mm gate width on SiC substrate. Harmonic manipulation circuits are presented in the amplifier. The matching networks consist of microstrip lines and discrete components. Open-circuited stub lines in both input and output are used to tune the 2nd harmonic wave and match the GaN HEMT to the highest efficiency condition. The developed amplifier delivers an output power of 48.5 dBm (∼70 W) with a power-added efficiency (PAE) of 72.2% at 2 GHz in pulse condition. When operating at 1.8–2.2 GHz (20% relative bandwidth), the amplifier provides an output power higher than 48 dBm (∼ 65 W), with a PAE over 70% and a power gain above 15 dB. When operating in continuous-wave (CW) operating conditions, the amplifier gives an output power over 46 dBm (40 W) with PAE beyond 60% over the whole operation frequency range.

Keywords: power amplifier, GaN high-electron-mobility transistor (HEMT), high efficiency, harmonic manipulation

PACS: 73.61.Ey, 84.30.Bv, 84.30.Le **DOI:** 10.1088/1674-1056/23/3/037305

1. Introduction

In S-band communication systems, power amplifiers (PAs) with high power-added efficiencies (PAEs), high output powers, and wideband operations are strongly required. The efficiency of the amplifier is limited by the characteristics of the transistor.[1] In recent years, GaN-based high-electron-mobility transistors (HEMTs) have attracted much attention due to their outstanding properties of high breakdown voltage, high carrier density, high saturation velocity, and excellent thermal conductivity of the SiC substrate,[2–5] which make them promising candidates for high-power microwave device applications such as wireless base-stations.

With the development of material growth and device fabrication technologies, a number of manufacturers and researchers have reported GaN HEMTs with high efficiencies, output powers, and power densities. In 2009, Gil *et al.*[6] reported a class-E Doherty power amplifier with 62.6% PAE at 2.85 GHz. In 2012, Cheron *et al.*[7] designed a 55-W (3.82 W/mm) GaN-based PA with the PAE greater than 60% at 2.7 GHz. Although there are many high-power high-efficiency GaN-based amplifiers for S band, most of them operate in a pulsed mode and are restricted to narrow bandwidths.

The harmonic tuning technique[8–10] that makes use of harmonic manipulation is one of the solutions to realize high efficiency. To achieve high efficiency and simultaneously high output power, many GaN amplifiers adopt the harmonic impedance control technique using resonance circuits such as LC networks. However, for an amplifier with large gate-width FET, the highly precise impedance control of harmonics is required for high efficiency. Since the control is very sensitive, it is hard to realize high efficiency with discrete components.

In this work, we design and fabricate a single-stage power amplifier based on a self-developed GaN HEMT with 10 mm gate width technology on a SiC substrate. With the S parameter and load-pull measurement results, we design microstrip matching circuits using an advanced design system (ADS). In order to obtain high efficiency at broadband, we use multi-stage microstrip open-circuited stub lines to form harmonic manipulation circuits both in the input and output matching networks. To maintain the stability of the amplifier, we add an RC network at the input and a resistor between the DC power source and the gate of the transistor.[11] The amplifier is designed to operate from 1.8 GHz to 2.2 GHz. To obtain the highest efficiency, we adjust the microstrip open-circuited stub lines to control the 2nd harmonic wave and match the device to the highest efficiency impedance. When tested at 2 GHz under pulse mode, the amplifier presents an output power of 48.5 dBm (∼ 70 W) with a power-added efficiency of 72.2% and power gain of 15.9 dB. Under $V_{DS} = 28$ V pulsed mode from 1.8 GHz to 2.2 GHz (20% relative bandwidth), the saturated output power of the amplifier is larger than 48 dBm (∼ 65 W) with the power gain over 15 dB, and the PAE is

*Project supported by the National Natural Science Foundation of China (Grant No. 61203211), the Natural Science Foundation of Jiangsu Higher Education Institutions of China (Grant No. 13KJB140006), and the Foundation for Outstanding Young Teachers of Nanjing University of Information Science & Technology, China (Grant No. 20110423).

†Corresponding author. E-mail: xhma@xidian.edu.cn

© 2014 Chinese Physical Society and IOP Publishing Ltd

greater than 70%. When operating in continuous wave (CW) operating conditions, the amplifier provides an output power over 46 dBm (40 W) with power-added efficiency over 60% over the whole designed frequency range.

2. Growth epitaxy and device processing

Figure 1(a) shows a cross section of the GaN HEMT. The undoped AlGaN/AlN/GaN heterostructure layers were grown on a 3-inch semi-insulating 4H-SiC substrate by metal–organic chemical vapor deposition (MOCVD) at the University of Xidian. A 100-nm-thick high-temperature (HT) AlN nucleation layer was deposited next. Then, a 2-μm-thick GaN buffer layer was grown, followed by a 24-nm-thick undoped AlGaN barrier layer. At room temperature, the sheet resistance is approximately 320 Ω/□. The sheet carrier density and the electron mobility are 1.3×10^{13} cm^{-2} and 2050 cm^2/(V·s), respectively. The device processing started with isolation accomplished by Cl_2-based dry etching with an etching depth of about 150 nm. The RF power of RIE was 100 W and the etching rate was 60 nm/min. Ti/Al/Ni/Au source and drain electrodes were formed by electron-beam evaporation and annealed at 870 °C for 30 s. Then SiN passivation was achieved with plasma-enhanced chemical vapor deposition (PECVD)[12] and the thickness was 60 nm. The gate recess was achieved by plasma etching. The gate footprint ($L_g = 0.25$ μm) was opened by etching SiN using CF_4 plasma. The Schottky gate was formed by Ni/Au/Ni next. Finally, we used PECVD to deposit a 200-nm SiN passivation layer to protect the device. The photograph of a unit cell of the device is shown in Fig. 1(b). The gate width is 10×125 μm and the G–G spacing is 40 μm.

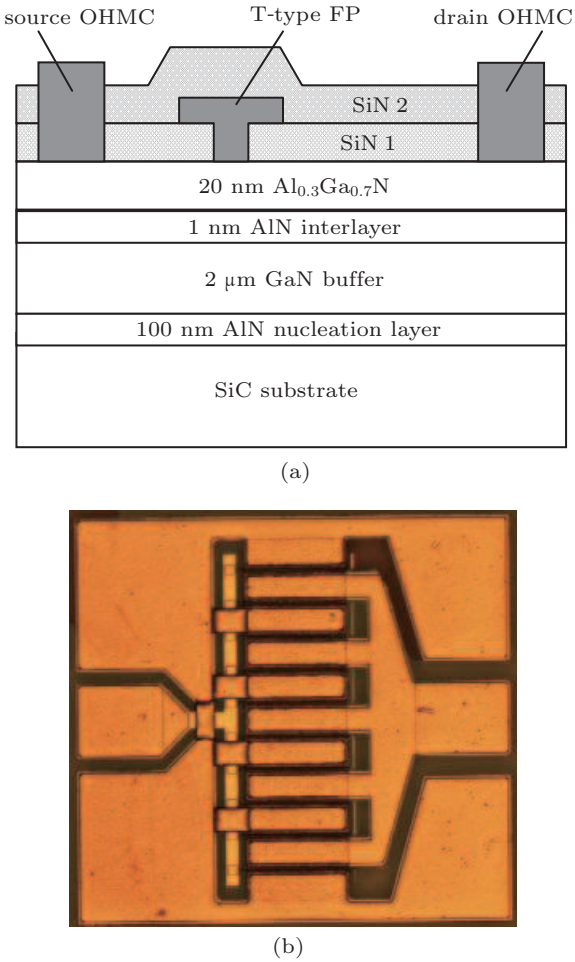


Fig. 1. (color online) (a) Structure and (b) photograph of the GaN FET.

A device with a gate length of 0.25 μm and a gate width of 10×125 μm is tested and the DC and pulse *I*–*V* characteristics are shown in Fig. 2. The saturation current density of the device is 1.6 A/mm at $V_{gs} = 1$ V and the peak transconductance is 650 mS/mm at 10 V drain bias. The threshold voltage is about −2.7 V. In the pulse test, the quiescent bias is (V_{ds0}, V_{gs0}) = (20 V, −8 V) and a 500-ns pulse is applied to the gate and drain. As shown in Fig. 2(b), the transistor has no current dispersion in pulsed *I*–*V* measurements.

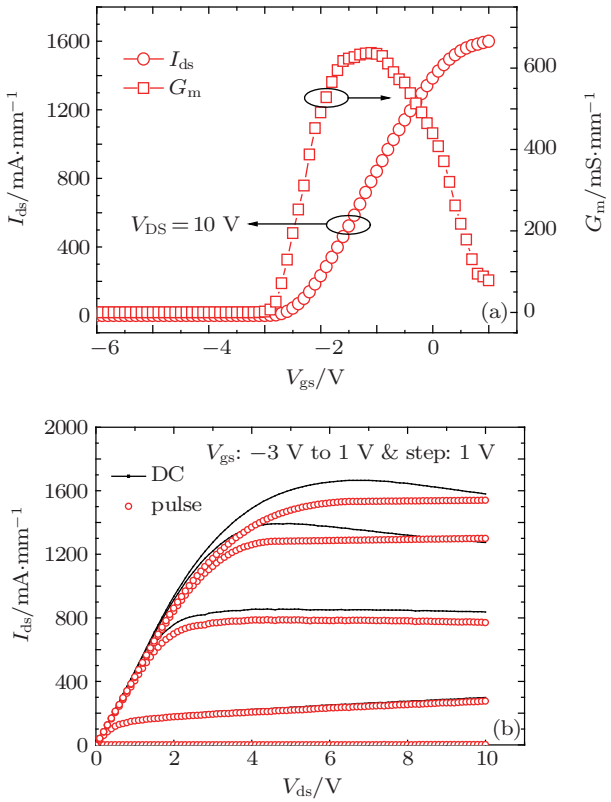


Fig. 2. (color online) (a) Transfer and transconductance characteristics; (b) DC and pulsed *I*–*V* curves of the device with a gate length of 0.25 μm and a gate width of 10×125 μm.

3. Design and fabrication of amplifier

The device in the amplifier has a gate periphery of 10 mm composed of eight unit cells of 1.25 mm gate width and is mounted to a Cu–Mo–Cu package as seen in Fig. 3. The gate and drain of the device are connected to the input and output of the device, respectively, by 1 mil gold wires. On-

wafer S-parameter and load-pull measurements are performed on the unit cell to obtain the RF characteristics and the optimum impedance for PAE. The tested highest-efficiency load impedance is $21.6 + j24$ at 2 GHz. Thus, we can estimate that for a 10-mm device, the best load impedance for PAE is $2.7 + j3$.

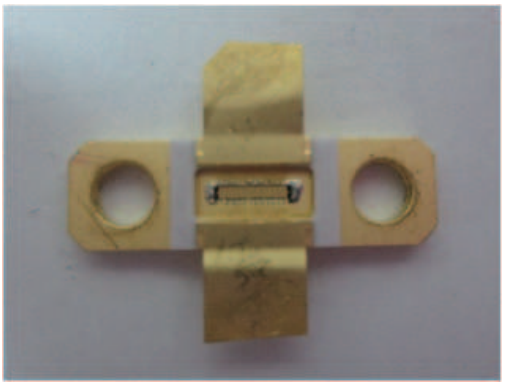


Fig. 3. (color online) External view of the packaged GaN HEMT.

Based on the measured S parameter and impedance, we design the matching circuit of the amplifier by ADS. The schematic of the amplifier is shown in Fig. 4 and the bipolar power supply is used. C_0 denotes a DC blocking capacitance to isolate the DC current. C_1, C_2, C_3, C_4, and C_5 are decoupling capacitances filtering the noise from the power source. The characteristic impedances of Z_1 and Z_2 are 128 Ω and 97 Ω, respectively. The length is 1/4 microstrip wavelength.

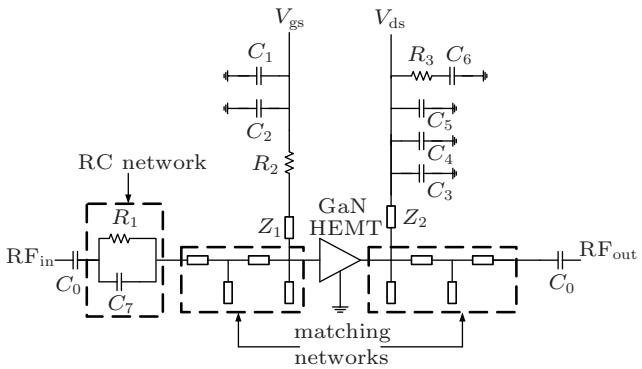


Fig. 4. Schematic of the GaN amplifier.

To achieve high efficiency in broadband, we use multistage microstrip lines to form the input and output harmonic tuning matching networks to control the 2nd harmonic wave. The output matching circuit consists of a two-stage microstrip matching network. Figure 5(a) shows the schematic of the output matching circuit. We present two open-circuited stub lines here. The stub line close to the HEMT makes the 2nd harmonic short and the other one is used to tune the phase of the 2nd harmonic. The equivalent circuits at the fundamental frequency and the 2nd harmonic frequency are shown in Figs. 5(b) and 5(c), respectively. The 2nd harmonic manipulation open-circuited stub line can be neglected at the fundamental frequency because its electric length is short.[13]

Because the 2nd harmonic manipulation open-circuited stub line has no effect on the fundamental frequency, the multistage transmission lines perform as an LCT network. During simulation, the phase tuned stub line is set to be short at the 2nd harmonic frequency. We tune the transmission lines to obtain a good match at the fundamental frequency. The manipulation stub line is adjusted to tune the short impedance into the target impedance at the 2nd harmonic frequency for the highest PAE. We also present two open-circuited stub lines in the input matching network to tune the 2nd harmonic. The function of the matching circuit is the same as that of the output one.

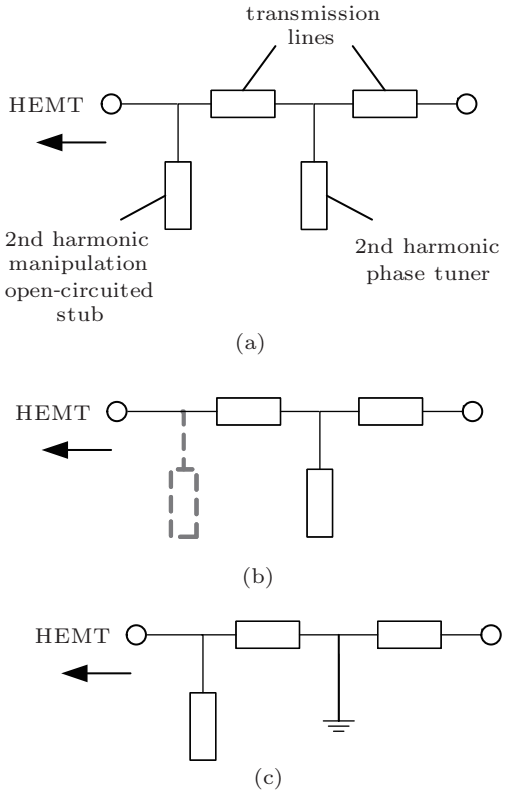


Fig. 5. (a) Output matching circuit and equivalent circuits at (b) fundamental frequency and (c) 2nd harmonic frequency.

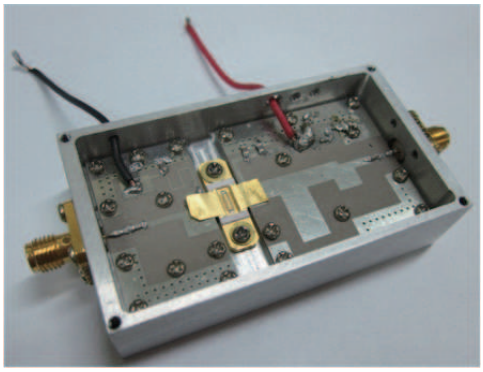


Fig. 6. (color online) Photograph of the power amplifier.

An RC network at the input, a resistor between the power supply and the gate of the transistor are added to improve the stability of the amplifier. An RC series network between the power supply and ground is used to eliminate the low-frequency oscillation of the amplifier. The amplifier is fabricated using a Teflon substrate (manufactured by Taconic Inc.) with a dielectric constant of 3.5 and a thickness of 0.762 mm. Figure 6 is the photograph of the built amplifier and the size is only 68 mm ×38 mm × 17 mm. During large signal tests, we adjust the length and width of the microstrip stub lines in the matching networks to maximize the PAE of the amplifier.

4. Large-signal measurements

First, we test the amplifier in pulsed mode. The RF input power is pulsed at a pulse width of 100 μs and 10 % duty cycle while bias voltage is continuous. To obtain high PAE, the gate is biased slightly above the pinch-off voltage and the drain bias voltage is 28 V. Figure 7 shows the measured microwave power performance of the amplifier. The small-signal gain is 17.4 dB and the saturated power is 48.5 dBm (∼ 70 W). At this time, the PAE of the amplifier is 72.2% and the power gain is 15.9 dB. From 1.8 GHz to 2.2 GHz, power sweeps are performed at five discrete frequencies with a drain voltage of 28 V in the pulsed mode. Figure 8 shows the results of the

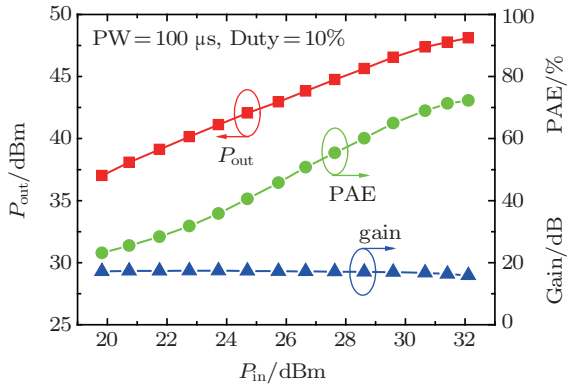


Fig. 7. (color online) Measured microwave power performances of the amplifier in pulse mode at 2 GHz and $V_{ds} = 28$ V.

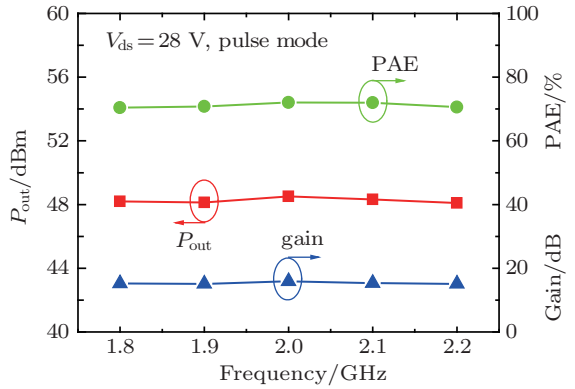


Fig. 8. (color online) Power measurements of the amplifier in pulsed mode in a frequency range from 1.8 GHz to 2.2 GHz.

power measurements. In the whole band, the output power of the amplifier is higher than 48 dBm (∼ 65 W) with a PAE over 70% and a power gain above 15 dB.

After pulsed measurements, the amplifier is tested in CW conditions. In Fig. 9, the large signal measurements are performed. The gate and drain bias voltages are the same as those set in the pulsed test. From Fig. 9, we can see that the maximum output power is 46.5 dBm (44.7 W) with 64.7% PAE and 14.5 dB power gain at 2 GHz.

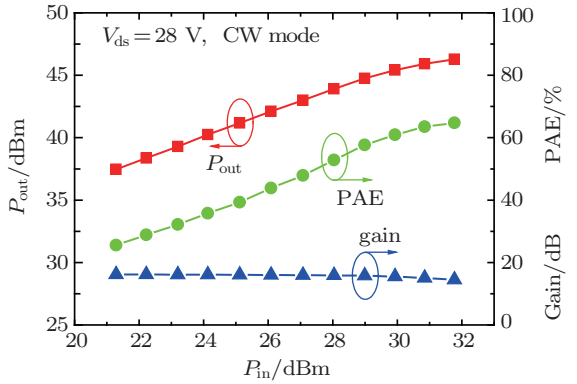


Fig. 9. (color online) Measured microwave power performances of the amplifier in CW mode at 2 GHz.

Figure 10 shows the measured output power, gain and efficiency characteristics of the amplifier in a frequency range from 1.8 GHz to 2.2 GHz. Power sweeps are performed at five discrete frequencies within the band with a drain voltage of 28 V. As can be seen, the amplifier presents an output power higher than 40 W, 13.3 dB gain, and 60 % PAE over the whole operation band.

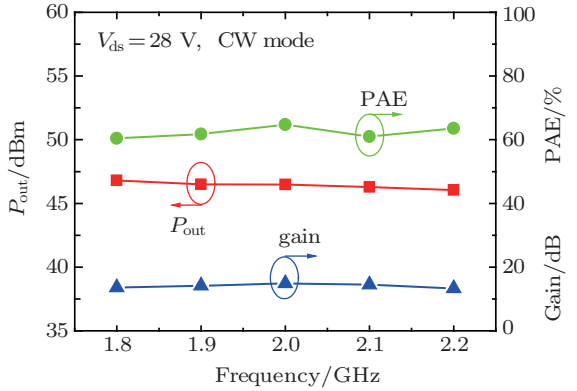


Fig. 10. (color online) Power measurements of the amplifier in CW mode in a frequency range from 1.8 GHz to 2.2 GHz.

5. Conclusion

In this paper, an S-band GaN HEMT high-power high-efficiency amplifier is developed. The amplifier is designed based on *S* parameter, and the multistage microstrip matching networks are used to achieve wideband performance. To realize high PAE, we adjust the lengths and widths of the open-circuited stub lines in the input and output matching networks

to tune the 2nd harmonic wave and match the packaged device to the highest efficiency condition. The amplifier gives an output power of 70 W, a PAE of 72.2%, and power gain of 15.9 dB at 2 GHz under 100-μs pulsed mode. When operating from 1.8 GHz to 2.2 GHz, the amplifier delivers an output power greater than 48 dBm (∼ 65 W) with a power-added efficiency over 70%, and a power gain above 15 dB. In CW mode, the PA gives an output power higher than 40 W, 13.3 dB power gain, and 60% PAE in a frequency range of 1.8–2.2 GHz (20% relative bandwidth). At 2 GHz, we obtain a high PAE of 64.7% and an output power of 44.7 W for the CW operation.

References

[1] Bumjin K, Derickson D and Sun C 2007 *Proceedings of the Asia-Pacific Microwave Conference*, December 11–14, 2007, Bangkok, Thailand, p. 1

[2] Trew R J, Bilbro G L, Kuang W, Liu Y and Yin H 2005 *Microwave Magazine* **6** 56

[3] Mishra U K, Parikh P and Wu Y F 2002 *Proceeding of the IEEE* **90** 1022

[4] Xie G, Xu E, Lee J, Hashemi N, Zhang B, Fu F Y and Ng W T 2012 *IEEE Electron Dev. Lett.* **33** 670

[5] Xie G, Edward X, Niloufar H, Zhang B, Fred Y F and Wai T N 2012 *Chin. Phys. B* **21** 086105

[6] Gil W C, Hyoung J K, Woong J H, Suk W S, Jin J C and Sung J H 2009 *Microwave Symposium Digest IEEE MTT-S International*, June 7–12, 2009, Boston, MA, p. 925

[7] Cheron J, Campovecchio M, Barataud D, Reveyrand T, Mons S, Stanislawiak M, Eudeline P and Floriot D 2012 *Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMIC)*, September 3–4, 2012, Dublin, Ireland, p. 1

[8] Colantonio P, Giannini F, Giofre R, Limiti E, Serino A, Peroni M, Romanini P and Proietti C 2006 *IEEE Transactions on Microwave Theory and Techniques* **54** 2713

[9] Maeda M, Masato H, Takehara H, Nakamura M, Morimoto S, Fujimoto H, Ota Y and Ishikawa O 1995 *IEEE Transactions on Microwave Theory and Techniques* **43** 2952

[10] Raab F H 1997 *IEEE Transactions on Microwave Theory and Techniques* **45** 2007

[11] Chen C, Hao Y, Feng H, Yang L A, Ma X H, Duan H T and Hu S G 2009 *J. Semiconductors* **30** 57

[12] Yang L, Hu G Z, Hao Y, Ma X H, Quan S, Yang L Y and Jiang S G 2010 *Chin. Phys. B* **19** 047301

[13] Otsuka H, Yamanaka K, Noto H, Tsuyama Y, Chaki S, Inoue A and Miyazaki M 2008 Microwave Symposium Digest, 2008 *IEEE MTT-S International*, June 15–20, 2008, Atlanta, America, p. 311