Large-scale SiO_2 photonic crystal for high efficiency GaN LEDs by nanospherical-lens lithography*

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Wafer-scale SiO_2 photonic crystal (PhC) patterns (SiO_2 air-hole PhC, SiO_2-pillar PhC) on indium tin oxide (ITO) layer of GaN-based light-emitting diode (LED) are fabricated via novel nanospherical-lens lithography. Nanoscale polystyrene spheres are self-assembled into a hexagonal closed-packed monolayer array acting as convex lens for exposure using conventional lithography instrument. The light output power is enhanced by as great as 40.5% and 61% over those of as-grown LEDs, for SiO_2-hole PhC and SiO_2-pillar PhC LEDs, respectively. No degradation to LED electrical properties is found due to the fact that SiO_2 PhC structures are fabricated on ITO current spreading electrode. For SiO_2-pillar PhC LEDs, which have the largest light output power in all LEDs, no dry etching, which would introduce etching damage, was involved. Our method is demonstrated to be a simple, low cost, and high-yield technique for fabricating the PhC LEDs. Furthermore, the finite difference time domain simulation is also performed to further reveal the emission characteristics of LEDs with PhC structures.

Keywords: InGaN light-emitting diodes (LEDs), photonic crystal, nanosphere lithography, FDTD simulation

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1. Introduction

GaN-based light-emitting diodes (LEDs) have been used for general illumination/decoration, traffic lights, and LCD backlight units.[1–4] Future demands for more extensive applications require higher brightness and lower power consumption. The LED quantum efficiency is determined by both internal quantum efficiency (IQE) and light extraction efficiency (LEE). Owing to great progress in crystal quality and structure design of active layers, the IQE for blue LED has reached as high as 70%.[5] However, the EQE of LED is still limited by the total internal reflection (TIR) between LED die and external medium. Various techniques, including surface-roughening[6] and patterned sapphire substrates,[7] have been adopted to improve the light extraction from LED device, which relies on the formation of non-parallel surface to minimize reflection. Specifically, the use of photonic crystal (PhC) structure in LED has drawn much attention, since it provides a novel method of controlling optical modes to improve the light extraction by efficiently coupling guided modes out of light-emitting diodes.[5] Generally, PhC structures have been fabricated directly in the p-GaN layer or ITO layer.[8–11] The plasma dry etching process has been reported to produce various defects, such as vacancies, impurities, and residuals, resulting in the degradation of LED electrical properties. To alleviate this degradation, an additional passivation process will be needed to polish the etching damages. On the other hand, it is worthy to note that applying PhC structure in p-GaN or ITO layer needs thick p-GaN or ITO to bear the plasma etching. Otherwise, leakage current will take place, accelerating the LED device degradation. However, a very thick p-GaN layer, with a poor crystalline quality,[12] will lead to lower optical transmission and higher working voltage, resulting in a decrease of the overall efficiency.

In addition, the height and the period of PhC structure is known to be on the order of its wavelength.[9,13] Therefore, traditional optical lithography will be inoperative to achieve this nanoscale patterning because of the optical diffraction effect. The frequently used nano-pattering methods, such as e-beam laser holography,[13] self-organized porous anodic alumina,[14] nanoimprint,[15] are used to fabricate PhC LED devices. However, the drawbacks of these three techniques include low throughput, high cost, and hardly patterning at full wafer level. As for nanoimprint, it is required to make improvement, that is, producing fewer defects, minimizing patterns at low cost and full wafer level.

In this study, we introduce a nanospherical-lens photolithography (NLP) method to fabricate SiO_2 PhC structures in GaN-based LEDs. The nanospheres are not directly used as etching masks, in which the space ratios of the nanospheres are hardly independently controlled, and the remnants are not

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easily eliminated. The proposed method has the advantages of low cost, high throughput, and full wafer level. Moreover, hexagonal-lattice SiO_2 PhC structures are directly processed on the wafers, which have been fabricated after the metal electrode deposition, avoiding the degradation of the electrical performance. Moreover, the SiO_2 PhC arrays can also act as passivation layer for the LEDs. The optical and electrical performances of dual structure SiO_2 PhCs LEDs are analyzed and discussed in detail. Finally, the finite-difference time-domain (FDTD) is employed to simulate the optical field distributions of the LEDs incorporating SiO_2 PhC structures.

2. Experiment

The blue InGaN/GaN LEDs with the wavelength of 445 nm were grown on *c*-plane sapphires by metal–organic chemical vapor deposition (MOCVD). The epitaxial LED structure is similar to that in our previous report.[16] After a 280-nm-thick ITO transparent conductive layer was deposited on the wafer, photolithography and inductively coupled plasma (ICP) etching were used to fabricate metal electrodes composed of Cr/Pt/Au (50 nm/50 nm/1500 nm) evaporated onto the ITO transparent conductive layer and the n-GaN layer by an e-beam evaporator. Figure 1 shows the schematics of the PhC LED fabrication process. For LED sample A, as shown in Fig. 1(a), the current electrode over wafer was deposited about 300-nm thick SiO_2 layer using plasma enhanced chemical vapor deposition (PECVD). Then, the surface was coated by 600-nm photosensitive resist (PR) AR-P 3120, followed by a hot plate bake for 15 min at 95 °C. Successively, nanospherical-lens were spin-coated on the PR, which was hexagonal close-packed monolayer of polystyrene spheres (PSs) with a diameter of 500 nm. After UV exposure about 5 s and developing about 5 s, holes each with a diameter of about 250 nm on PR were fabricated, using a conventional photolithography instrument, followed by the elimination of PS by ultrasonication in deionized water. Subsequently, the patterned PR was then baked at 110 °C for 10 min for bearing the followed ICP etching of SiO_2 dielectric. The ICP etching was performed using CF4 (532 mPa) at a radio-frequency power of 40 W, for duration 110 s by STS Multiplex AOE etching. Then, the SiO_2 with air-hole PhC LED (SiO_2-hole PhC) with 500-nm period lattice and about 250-nm air holes was successively completed. In Fig. 1(b), inverse SiO_2 structure PhC LEDs (sample B), were also fabricated, which consisted of SiO_2 nanopillars on the surfaces (called SiO_2-pillar PhC). After the above NLP process of developing, 250-nm thick SiO_2 layer was sputtered on patterned PR using an oxford ion beam sputter at room temperature and a pressure of approximately 1.3×10^{-2} Pa. A lift-off process was then carried out by dissolving the PR in acetone for 30 min, retaining the arrays of SiO_2 nanodisk. In the lift-off process, 250-nm SiO_2 on the photoresist can be well lifted off, remaining the arrays of SiO_2 nanodisk perfectly. Afterwards, these wafers were processed into chips with a square mesa of 45 mil^2 (1 mil = 0.0254 mm) in size. For comparison, an un-patterned LED with identical dimensions is also fabricated. All of the devices were fabricated from the same LED wafer, in order to eliminate the variations in the device characteristics found from wafer to wafer.

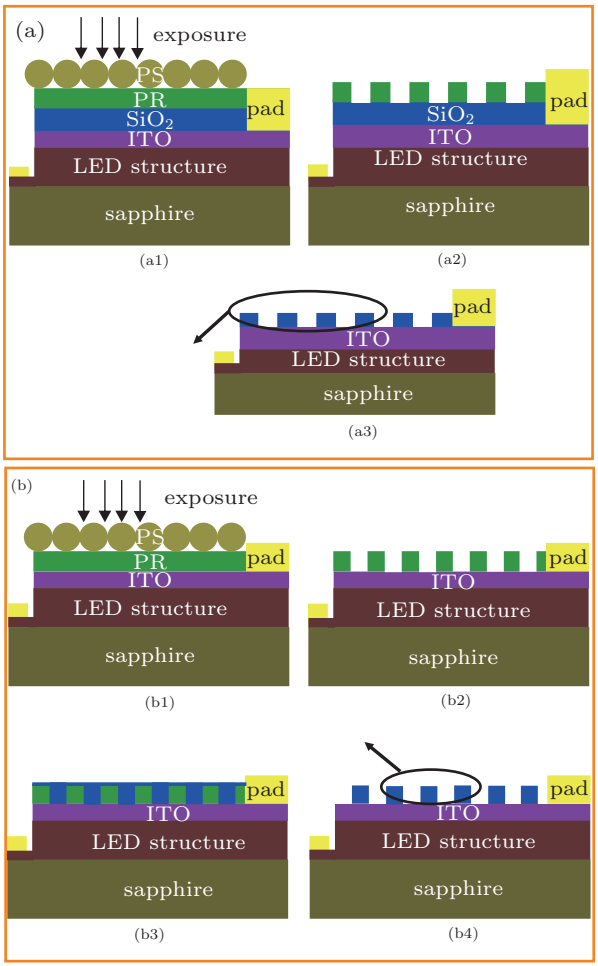


Fig. 1. (color online) Schematic diagrams showing the fabrication process flow chart of SiO_2 PhC structures in LEDs: (a) SiO_2 hole PhC LEDs: a(1) exposure for the current electrode over wafer with PS arrays, a(2) after developing, a(3) after dry etching; (b) SiO_2-pillar PhC LEDs: b(1) exposure for the current electrode over wafer with PS array, b(2) after developing, b(3) SiO_2 deposition at room temperature, b(4) SiO_2 pillar arrays after PR lift-off in acetone.

3. Results and discussion

Figure 2(a) shows the optical photographs of 2-inch LED wafer (1 inch = 25.4 mm) with full spin coating PS on PR. In the close view SEM images, the hexagonally close-packed of monolayer PS arrays of 500-nm lattice can be found. The SiO_2 hole PhC and SiO_2-pillar PhC are shown in Figs. 2(b) and 2(c), respectively, with a periodic lattice of 500 nm determined by the diameter of PS nanospheres, which is on the order of wavelength of blue LED, leading to higher LEE.[17] In experiment, we found that if the diameter of the PS is too much small (for example, 400 nm), then the NLP method cannot work because

of diffraction effect in UV-exposure process. The diameter for hole and SiO_2 nanopillar trimmed with about 250 nm, are turned by the UV-exposure and developing time. So, the duty cycle was set to be a special value of 1:1, its other value will be discussed elsewhere.

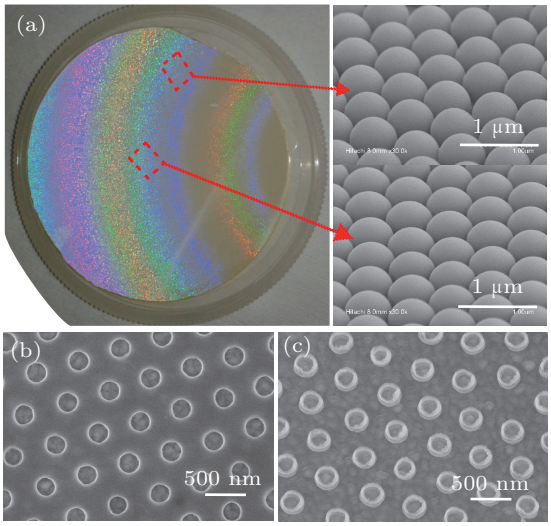


Fig. 2. (color online) SEM images showing (a) ordered hexagonal monolayer arrays of PS on RF surface, and partial enlarged drawings of the inner and outer of the wafer; (b) the surface of SiO_2 hole PhC LED; (c) the surface of SiO_2-pillar PhC LED.

Figure 3(a) shows the light output power (LOP) of the blue LEDs with and without SiO_2 PhC structures, with collecting the emitted light with a 2-inch (1 inch = 25.4 mm) integrating sphere optically coupled to a radiometrically calibrated spectrometer. The LOP of LEDs with SiO_2 hole PhC, and SiO_2-pillar PhC is increased by as great as 40.5% and 61%, compared with those of reference LEDs at an input current of 350 mA, respectively. The insets of Fig. 3(a) show the emission images of the corresponding LEDs operating at a low injection current of 2 mA. The SiO_2-pillar PhC LED is brighter than the LEDs with SiO_2 hole PhC and without PhC. The improvement is attributed to the increase in LEE due to the PhC effect, which creates the cut-off frequency for the guided modes. The modes above the cut-off frequency are leaky and couple to free space.[18] The current–voltage (I–V) characteristics of the LEDs are plotted in Fig. 3(b). The forward voltages at 20-mA current are 2.70, 2.71, and 2.70 V, for SiO_2-pillar PhC, SiO_2-hole PhC, and without PC LED, respectively. The slopes of the I–V curves in the linear region, the series resistance, are also identical. This is due to the fact that SiO_2 PhC structures were fabricated on ITO current electrode over wafers. The LOP and I–V data have testified the fact that the fabrication process, corresponding to SiO_2-pillar PhC LED, leaves the ITO intact and free of any etching damages, demonstrating a promising simple technique to improve the LEE of LEDs without any degradation of electrical properties.

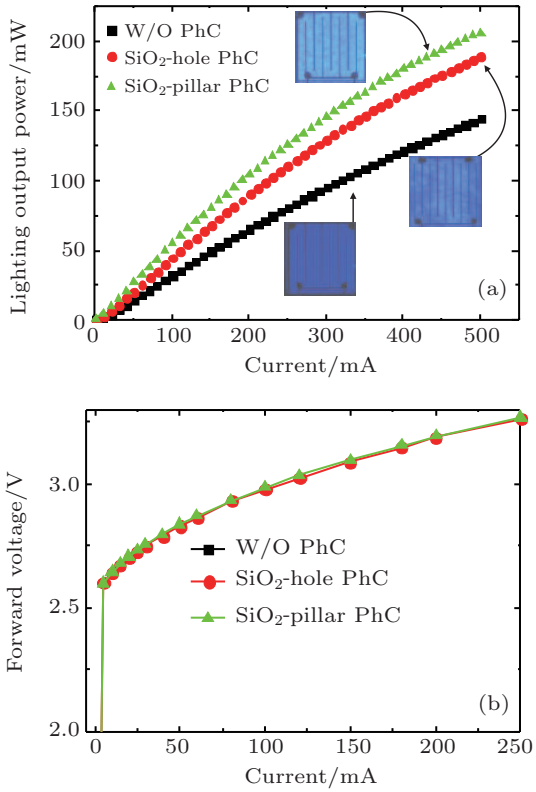


Fig. 3. (color online) (a) Plots of light output power versus injection current and the insets show the corresponding optical microphotographs of the above LEDs operated at a low injection current of 2 mA; (b) I–V characteristics of the SiO_2 hole PhC LED, SiO_2-pillar one, and as grown LED.

To investigate the effect of SiO_2 PhC on the LED angular emission profile, the chips were loaded on an aluminum-base plate and bonded with Au-wire without epoxy encapsulation. As shown in Fig. 4(a), the full-width at half-maximum (FWHM) divergence angles are 135.7°, 146.3°, and 162.2°, for the SiO_2-pillar PhC LEDs, SiO_2-hole PhC LEDs, and without PhC LEDs, respectively. The light from SiO_2-pillar PhC LEDs exhibits more converging effect over the others and a divergence angle reduction of 26.5° compared with the light from the conventional LEDs. The divergence angle reduction is ascribed to the SiO_2 PhC structure to inhibit the light radiating from lateral direction, which leads to a molded flow of light rather than randomly scattered one.

Because of the symmetrical characteristic of SiO_2 PhC structure, a two-dimensional (2D) FDTD simulation was conducted to show the light field distribution of PhC LEDs. The model used in simulation was simplified into the one that consisted of a 150-μm sapphire substrate, a 4-μm GaN layer, a 280-nm ITO layer, followed by SiO_2 PhC structure being the top surface. The point radiant sources of 460-nm wavelength were set below the SiO_2 hole or SiO_2-pillar at 3.06 μm away from GaN/sapphire interface right at the center of active layers. Only transverse electric (TE) polarization was taken into consideration, which is absolutely dominant in the GaN-based LEDs.[19] Figures 4(b)–4(d) show that the distributions of light electrical field intensities from the cross sections of LEDs with

SiO_2-pillar PhC, SiO_2 hole PhC, and without PhC LEDs, respectively. It should be noted that the field intensity of SiO_2-pillar PhC LED below the top surface appeared to be weaker, and that of SiO_2-pillar PhC LED over the top surface showed more converging effect than those of SiO_2 hole PhC LEDs and those without PhC.

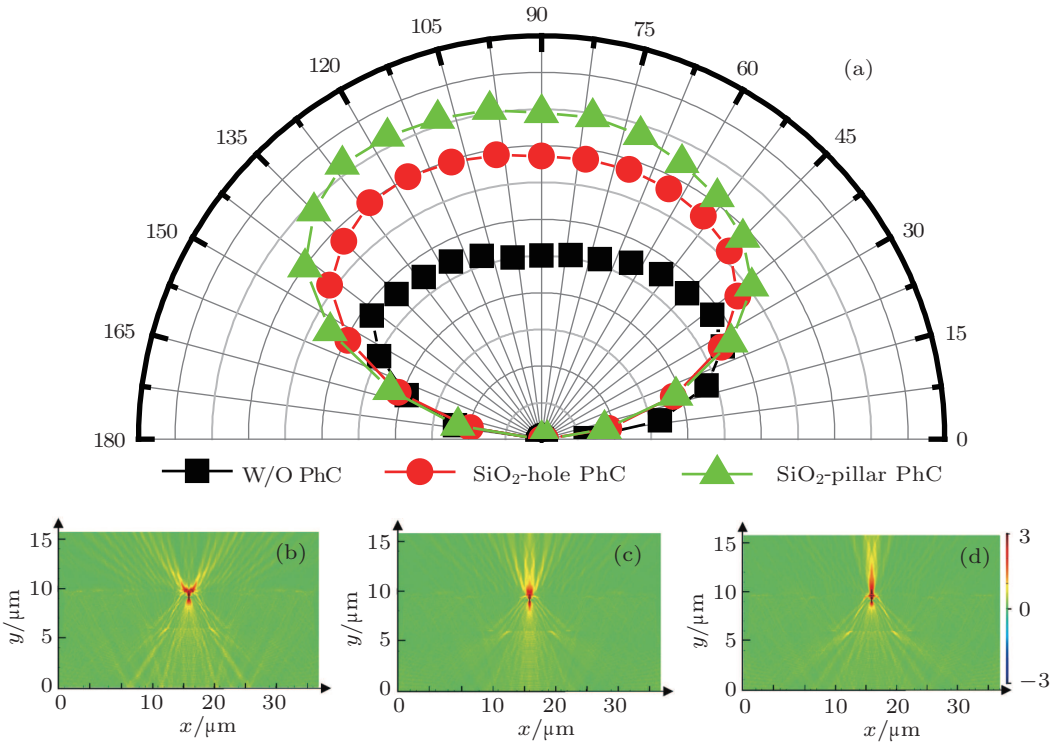


Fig. 4. (color online) (a) Far-field emission patterns of the LEDs SiO_2 hole PhC LED, SiO_2-pillar, and without PhC LEDs; FDTD simulation of light propagation in (b) LED without PhC, (c) with SiO_2 hole PhC LED, and (d) SiO_2-pillar PhC LED.

4. Conclusions

In this paper, high-quality wafer-scale SiO_2 PhC structures on ITO layer of GaN-based light-emitting diodes (LEDs) are fabricated via a novel NLP process unitizing the focusing behavior of PS nanospheres. Significant improvement in the light output power is observed over as-grown LEDs. The proposed method demonstrates that it will not introduce any degradation to the electrical properties of the fabricated LEDs. The LEDs with SiO_2 pillar PhC structure exhibits the highest light output power and the most significant focusing effect, which are consistent with FDTD simulation result. This damage-free method, with great advantages of low cost and high-yield, enables them to be a promising technique for commercial production.

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