Impact of multiplexed reading scheme on nanocrossbar memristor memory's scalability*

Zhu Xuan(朱 玄)[a)b)], Tang Yu-Hua(唐玉华)[a)b)], Wu Chun-Qing(吴纯青)[b)†], Wu Jun-Jie(吴俊杰)[a)b)], and Yi Xun(易 勋)[a)b)]

[a)] *State Key Laboratory of High Performance Computing, National University of Defense Technology, Changsha* 410073, *China*
[b)] *School of Computer, National University of Defense Technology, Changsha* 410073, *China*

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Nanocrossbar is a potential memory architecture to integrate memristor to achieve large scale and high density memory. However, based on the currently widely-adopted parallel reading scheme, scalability of the nanocrossbar memory is limited, since the overhead of the reading circuits is in proportion with the size of the nanocrossbar component. In this paper, a multiplexed reading scheme is adopted as the foundation of the discussion. Through HSPICE simulation, we reanalyze scalability of the nanocrossbar memristor memory by investigating the impact of various circuit parameters on the output voltage swing as the memory scales to larger size. We find that multiplexed reading maintains sufficient noise margin in large size nanocrossbar memristor memory. In order to improve the scalability of the memory, memristors with nonlinear *I*–*V* characteristics and high LRS (low resistive state) resistance should be adopted.

Keywords: nanocrossbar, memristor, multiplexing, reading circuit, voltage swing

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1. Introduction

In recent years, as the market of consumer electronics enters into a fast growth period, the requirement for high capacity non-volatile memory has become unprecedentedly strong. However, as the feature size of CMOS technology scales down to 22 nm, promoting memory density through traditional technology such as FLASH etc. it is facing increasingly severe challenges.[1] To satisfy the ever-increasing demand, many novel memory technologies have been exploited.

In 2008, HP laboratory announced the physical fabrication of the predicted 'memristor' using a two-terminal titanium dioxide nanoscale device.[2] As the research on memristor memory continuously progresses, memristor memory integrated in nanocrossbars has attracted increasing attention.[3–8] Nanocrossbar is a memory architecture based on nanowire, which has ultra-high potential in memory density with the minimum cell size of $4F^2$ (F is the minimum feature size).[9] It shows natural parallelism in spacial structure, and the fabrication process has also been developed to be compatible with CMOS technology.[5] Currently, nanocrossbar memory is potentially one of the most promising architecture for future non-volatile high-density memory technology.

Scalability is the key to the design of nanocrossbar memory because the larger the size the nanocrossbar could be scaled to, the lower the overhead peripheral circuits take on average and the more density advantages it shows. Taking scalability as one of the main targets, many read and write circuits have been proposed, and many conclusions have been made.[10–12] However, in the published research, evaluation of the scalability of nanocrossbar memory only concerns the nanocrossbar component, leaving the impact of the peripheral circuits unconsidered. Actually, based on the currently widely-adopted parallel reading scheme, scalability of the nanocrossbar memory is limited since the overhead of the reading circuits is in proportion with the size of the nanocrossbar component. Thus, increase in size does not promote the overall density of the nanocrossbar memory.

An effective method to promote the average memory density of the nanocrossbar memory is to multiplex the reading circuits among the bit lines. In this manner, increasing the size of the nanocrossbar will not incur extra circuit overhead. However, previous research conclusions may not be adaptable again, since new problems may rise from interference among the bit lines. Thus, based on multiplexed reading circuits, we reanalyze scalability of the nanocrossbar array in this paper. We investigate the impact of various circuit parameters on the output voltage swing as the array scales to larger size, and draw several useful conclusions from HSPICE simulation.

2. Circuit structure and analysis

In this section, we will give a short description of the difference between the parallel and the multiplexed reading scheme, and then discuss the scalability of the nanocrossbar memory based on the multiplexed reading scheme. A CMOS interface circuit for parallel reading of nanocrossbar memristor memory has been fabricated and demonstrated in Ref. [12].

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†Corresponding author. E-mail: wuchunqing@nudt.edu.cn
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As shown by Fig. 1(a), the selected word line is driven by a high voltage V_R and the unselected word lines are grounded. Each bit line is connected with an operational amplifier (OPA) which holds the bit line voltage to virtual ground and thus eliminates the sneak current. Based on this parallel structure, a multiplexed version can be obtained by sharing the reading circuits among all the bit lines, as shown by Fig. 1(b). In the following discussion, we will use this circuit structure as the base of our analysis and simulation. The other proposed reading circuits can be analyzed in the same way.

Under an ideal assumption of the circuit when voltage drop on wires and column-access transistors can be neglected, current through the accessed memory cell is converted to voltage output of the OPA circuit, which is given by

$$V_{OUT} = -V_R \times R_F / R_{MEM}, \tag{1}$$

where R_F is the resistance of the feedback resistor of the OPA circuit and R_{MEM} is the resistance of the accessed memory cell. It can be seen that the output is unrelated to either of the other cells' states or the size of the array.

In the real case where the voltage drop on wires and column-access transistors cannot be neglected, output of the circuit may deviate from the ideal estimation and scalability of nanocrossbar may be affected. On the one hand, due to the voltage drop on the column-access transistor, leaky current exists on the unselected cells within the accessed column, which may reduce the readout voltage of a low resistive state (LRS) cell, as shown in Fig. 2(a). Moreover, the previous assumption becomes more imprecise as the number of word lines increases. On the other hand, due to the resistance of the wires, grounding word lines become less effective to inhibit sneak current at the center of the nanocrossbar. When the bit line extends to large numbers, sneak path might happen, which may increase the readout voltage of a high resistive state (HRS) cell, as shown in Fig. 2(b).

These nonideal effects will lead to the shrinking of the difference between the readout voltage of LRS and HRS (also referred to as voltage swing), and hinder the correct reading of the cell's state. Unfortunately, when these two factors are put together it is difficult to quantitatively describe their effects on the readout voltage. In the following discussion, we will use HSPICE simulation to analyze the impact of these factors as well as other parameters on the scalability of the circuit.

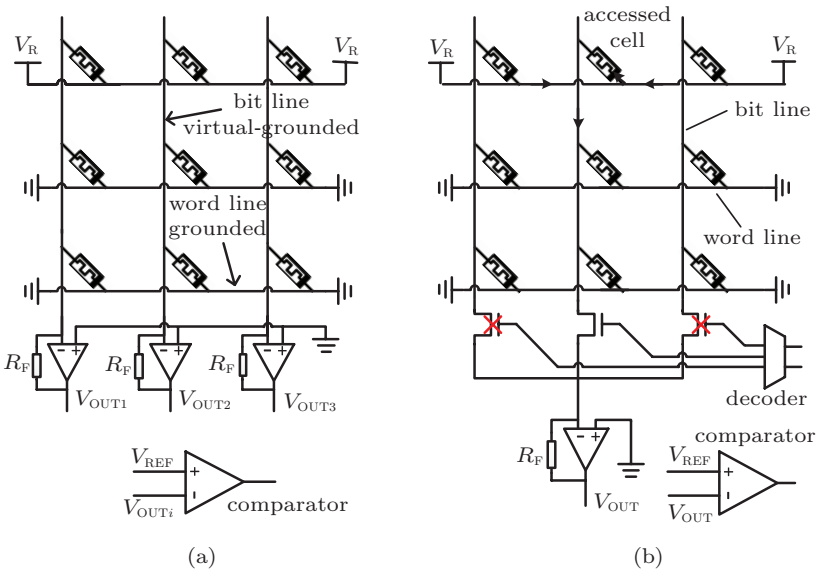


Fig. 1. Reading circuit structure.

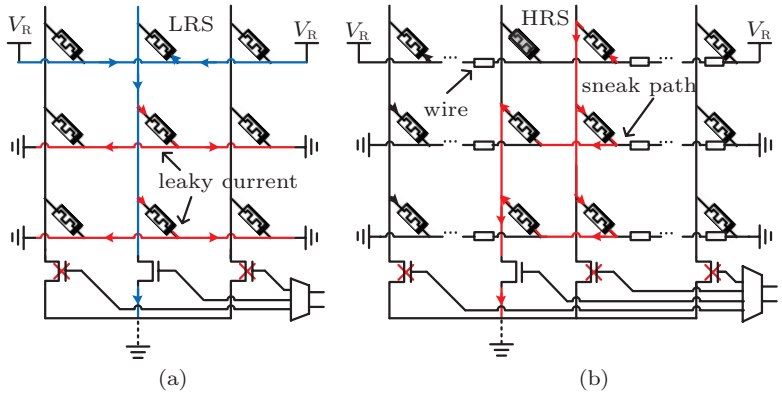


Fig. 2. (color online) (a) Leaky current reduces the readout voltage of an accessed LRS cell. (b) Sneak paths increase the readout voltage of an accessed HRS cell.

3. Simulation setup

3.1. Circuits model

At present, many circuit models for memristor have been proposed. To exclude the impact of device model on the conclusion, we use two different models to carry out simulation, the I–V characteristics of which are shown in Fig. 3. The first model we adopt is based on Ref. [13], since this model depicts several details of the actual devices' characteristics, and can be applied to a wide range of memristors. Using this model, the I–V characteristics of memristor, shown in Fig. 3(a), are expressed by the following nonlinear relationship

$$I(t) = \begin{cases} a_1 x(t) \sinh(bV(t)), & V(t) \geq 0, \\ a_2 x(t) \sinh(bV(t)), & V(t) < 0, \end{cases} \tag{2}$$

where $x(t)$ is the state variable which defines the resistive state of the memristor. $x(t)$ is composed of two factors as expressed by

$$\frac{\mathrm{d}x}{\mathrm{d}t} = g(V(t))f(x(t)). \tag{3}$$

Here, $g(V(t))$ describes the threshold effect of some of the memristor, which holds the memristor's state unchanged when a voltage smaller than a certain threshold is applied

$$g(V(\mathrm{t})) = \begin{cases} A_\mathrm{p}(\mathrm{e}^{V(t)} - \mathrm{e}^{V_\mathrm{p}}), & V(t) > V_\mathrm{p}, \\ -A_\mathrm{n}(\mathrm{e}^{-V(t)} - \mathrm{e}^{V_\mathrm{n}}), & V(t) < -V_\mathrm{n}, \\ 0, & -V_\mathrm{n} \leq V(t) \leq V_\mathrm{p}, \end{cases} \tag{4}$$

$f(x)$ reflects the relationship between the changing rate of $x(t)$ and its current state

$$f(x) = \begin{cases} \mathrm{e}^{-\alpha_\mathrm{p}(x-x_\mathrm{p})} \dfrac{1-x}{1-x_\mathrm{p}}, & x \geq x_\mathrm{p}, \\ 1, & x < x_\mathrm{p}, \end{cases} \quad \text{when } V(t) > 0, \tag{5}$$

$$f(x) = \begin{cases} \mathrm{e}^{\alpha_\mathrm{n}(x+x_\mathrm{n}-1)} \dfrac{x}{1-x_\mathrm{n}}, & x \leq 1-x_\mathrm{n}, \\ 1, & x > 1-x_\mathrm{n}, \end{cases} \quad \text{when } V(t) < 0. \tag{6}$$

Here, V_p, V_n, A_p, A_n, x_p, x_n, α_p, α_n, a_1, a_2, b are all parameters that are used to fit the characteristic curve of specific devices. It is clear that when applying a reading voltage that is smaller than the threshold, the memristor's state will not be changed.

The second model describes the memristor's I–V characteristic as a linear relationship. As shown in Fig. 3(b), the memristor could be treated as a linear resistor of either HRS or LRS. Parameters setting could be found in Table 1.

The nanowire is simulated using a distributed pi model. According to Ref. [11], the interconnect resistance between two adjacent cells is set to 2.5 Ω. The parasitical capacitance of nanowire is set to 2 pF·cm^{-1}. OPA circuit is simulated using an ideal behavioral model. The read voltage V_R is set to 1 V.

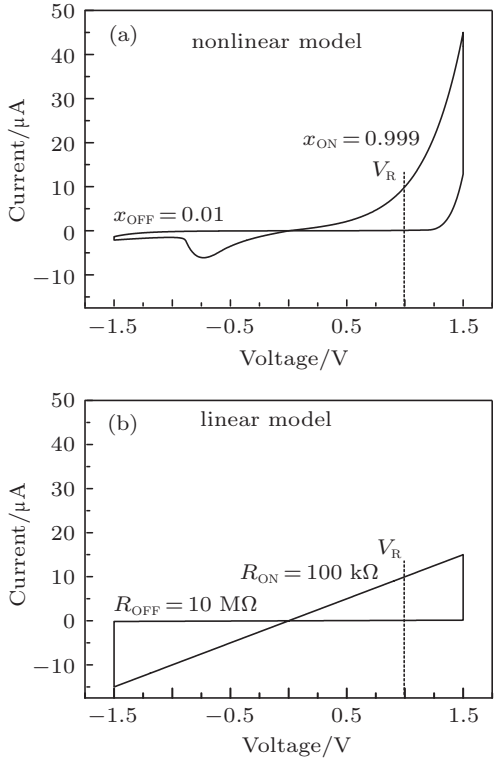


Fig. 3. I–V characteristic of (a) nonlinear model and (b) linear model.

Table 1. Parameter setting.

Parameter name	Value	Parameter name	Value
V_p	1.2 V	b	3
V_n	0.6 V	a_1	1×10^{-6}
A_p	5	a_2	1.65×10^{-6}
A_n	30	x_{ON}	0.01
x_p	0.7	x_{OFF}	0.999
x_n	0.8	R_{ON}	100 kΩ
a_p	4	R_{OFF}	10 MΩ
a_n	24	V_R	1 V

3.2. Memory pattern

As the circuits' output is highly related to the state of cells in the nanocrossbar, memory pattern is a key factor that will influence the readout voltage. In the following discussion, only the worst case scenario is considered where two criterions must be satisfied. Firstly, it should be located at the memory cell which is the furthest to the driving voltage source and column-access transistors, as the error induced by voltage drop on wires is most prominent over there. Secondly, all the non-accessed cells of the nanocrossbar are at LRS, as the disturbances caused by the non-accessed cells are all incurred by cells of LRS as analyzed in Section 2.

To exclude the linear amplification effect of the feedback resistor R_F on output voltage, we normalize the interrogated output voltage to the maximum output voltage V_{MAX} of the memory array which is defined as output of the best case. To the contrary of the worst case, the best case should be located

at the memory cell which is the closest to the driving voltage source and column-access transistors. It should be at LRS with all the non-accessed cells at HRS.

4. Results and discussion

4.1. Geometry dependence

Here we aim at figuring out the dependence of the nanocrossbar memory's output on either the bit line number or the word line number using the multiplexed reading circuit.

Figures 4 and 5 reveal the impact of the number of word lines and bit lines on the output voltage of both HRS and LRS, respectively. In Fig. 4, number of bit lines is fixed at 16, while the word line number increases from 8 to 256. Readout voltages of both LRS and HRS decrease as the word line number increases. At the size of 256 word lines, the LRS readout voltage drops to less than 10% of V_{MAX} in the linear case and about 30% of V_{MAX} in the nonlinear case. This is in accordance with the previous analysis on the impact of word line number.

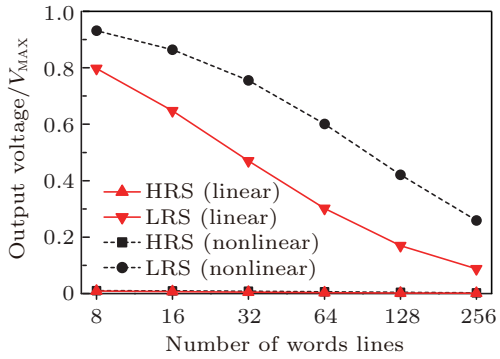


Fig. 4. (color online) Output voltage of both HRS and LRS as a function of the number of word line.

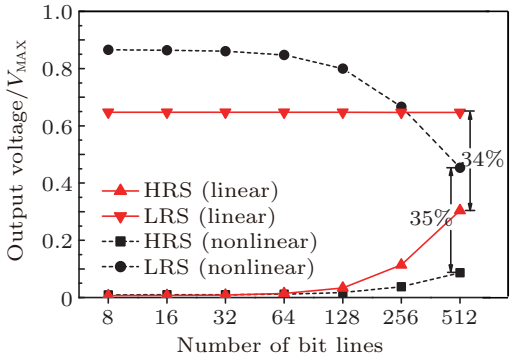


Fig. 5. (color online) Output voltage of both HRS and LRS as a function of the number of bit line.

In Fig. 5, the number of word lines is fixed at 16, while the bit line number varies from 8 to 512. Readout voltage of HRS increases as the bit line number rises in both cases. When the bit line number extends to 512, readout voltage swing reaches about 30% of V_{MAX} in both the linear case and the nonlinear case. This also verifies the analysis on the impact of bit line number. It can also be seen that the output voltage is more sensitive to word line number as the curve varies faster in Fig. 4 than in Fig. 5.

Figure 6 shows the percentage change of output voltage swing of the circuit with respect to the size of a square nanocrossbar array. It can be seen that output voltage swing declines linearly with the exponential increase of the nanocrossbar size, and a margin of above 15%V_{MAX} in the linear case (35%V_{MAX} in the nonlinear case) can be attained at the size of 128×128.

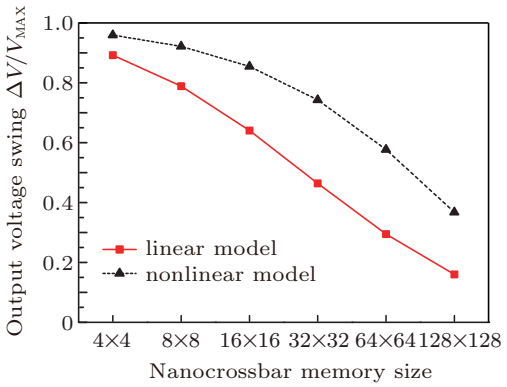


Fig. 6. (color online) Output voltage swing as a function of memory size.

4.2. Nonlinear *I–V* characteristic dependence

In Fig. 4, dropping of the LRS readout voltage in the nonlinear case is much slower than the linear case with a voltage swing of more than 25% at the size of 256×16 (compared to less than 10% in the linear case). This can be explained by the nonlinear *I–V* characteristic which impresses the leaky current bypassed from the unselected word lines, as shown in Fig. 2(a). Since less current leaks, a higher readout voltage of LRS is acquired in the nonlinear case.

In Fig. 5, HRS output using the nonlinear model exhibits a similar but slower rising trend to the linear case. This is because the sneak current injected from the neighboring bit lines, as shown in Fig. 2(b), is reduced as a result of the nonlinearity. The LRS output in the nonlinear case keeps a higher level when the bit line number is less than 128, but declines to lower than the linear case when the bit line number reaches about 256. This can be explained that as the bit line number extends, driving voltage on the accessed memristor cell is reduced. According to the nonlinear *I–V* characteristic, readout current of the accessed cell therefore decreases.

In Fig. 6, the overall declining of output voltage swing is much slower in the nonlinear case, which maintains above 35% of V_{MAX} at the size of 128×128. In general, introducing a 0memristor with nonlinear *I–V* characteristic in memory design does not better the output when bit line number increases. However, scalability of the word line dimension is clearly improved.

4.3. Circuit parameter dependence

Figure 7 shows the percentage change of output voltage swing with respect to an increasing number of bit lines and the different resistance of LRS. Only the linear model is used here. The resistance ratio between HRS and LRS is fixed at 100, while the resistance of LRS is set to 200 kΩ, 100 kΩ, 50 kΩ, and 10 kΩ, respectively. At the size of 16×512, output voltage swing shrinks to no more than 1% for LRS of 10 kΩ, while it remains above 50% for LRS of 200 kΩ. Thus, a conclusion can be made that the scalability of the multiplexed circuit could be improved by adopting a memristor with the higher resistance value of LRS. Besides, it could be conceived that the high resistance value of LRS will become more crucial as continuous scale-down of the circuits brings higher resistance of the interconnect nanowire.

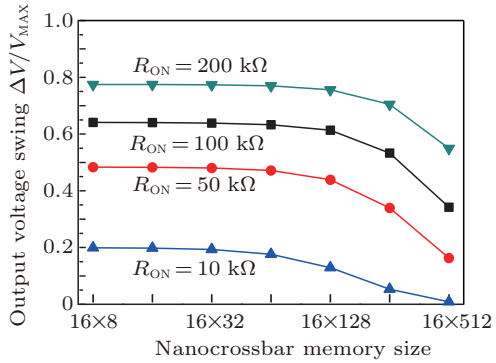


Fig. 7. (color online) Impact of LRS resistance on output voltage swing.

Figure 8 shows the impact of resistance ratios between HRS and LRS on the output voltage swing, for a given LRS of 100 kΩ. As the LRS resistance is fixed, variance in resistance ratio actually reveals the influence of HRS resistance on output voltage swing. It can be concluded that the impact of resistance of HRS is not obvious when extended to large size. This is easy to understand as all the possible sneak paths are made up by non-accessed cells at LRS.

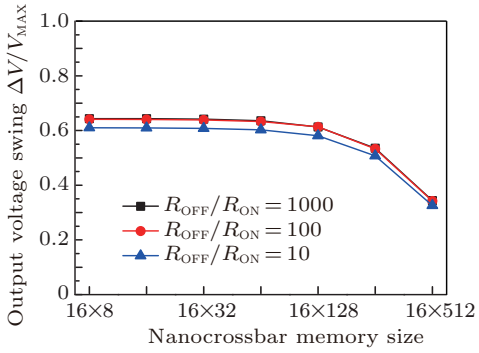


Fig. 8. (color online) Impact of ratio between HRS and LRS on output voltage swing.

5. Conclusion

To take full advantage of the high density potential and maximize the proportion of the nanocrossbar area in memristor memory, multiplexing of peripheral CMOS circuits is a simple but effective approach. In this paper, we analyzed the impact of the multiplexed reading scheme on nanocrossbar memory's scalability through HSPICE simulation. Useful conclusions can be made that multiplexed reading provides sufficient noise margin in large size nanocrossbar memristor memory. In order to improve scalability of the memory, memristors with nonlinear I–V characteristics and high LRS resistance should be adopted.

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