Effects of annealing process on characteristics of fully transparent zinc tin oxide thin-film transistor*

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Annealing effect on the performance of fully transparent thin-film transistor (TTFT), in which zinc tin oxide (ZnSnO) is used as the channel material and SiO_2 as the gate insulator, is investigated. The ZnSnO active layer is deposited by radio frequency magnetron sputtering while a SiO_2 gate insulator is formed by plasma-enhanced chemical vapor deposition. The saturation field-effect mobility and on/off ratio of the TTFT are improved by low temperature annealing in vacuum. Maximum saturation field-effect mobility and on/off ratio of 56.2 $cm^2/(V\cdot s)$ and 3×10^5 are obtained, respectively. The transfer characteristics of the ZnSnO TFT are simulated using an analytical model and good agreement between measured and the calculated transfer characteristics is demonstrated.

Keywords: zinc tin oxide, thin-film transistors, mobility, annealing

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1. Introduction

Thin-film transistors (TFTs) have pervaded our daily life as indispensable elements in a myriad of electronic products.[1] Wide band gap oxide semiconductors have attracted considerable attention in these areas because of their superior high-field transport properties, optical transparencies, and low light sensitivities. Oxide TFTs in which the In_2O_3,[1] ZnO,[2–5] SnO_2,[6,7] In–Zn–O,[8–11] Ga–Zn–O,[12] In–Ga–Zn–O[13] are used as active channels have been widely studied. Most of these oxide TFTs require high temperatures and complex production processing to obtain good electrical performances.[7,8]

In the fabrication of oxide TFTs, zinc tin oxide (ZnSnO) compounds as channels of TFTs have recently garnered considerable attention.[14] Gorrn *et al.*[15] studied the influence of visible light irradiation on ZnSnO TFTs with varying compositions and processing temperatures, which proved that ZnSnO-based transparent TFTs are attractive candidates for pixel drivers in active-matrix organic light emitting diode (OLED) displays. Seok-Jun *et al.*[16] fabricated ZnSnO TFTs by a simple and low-cost precursor solution process through spin-coating. Jackson *et al.*[17] fabricated flexible transistors by sputtering deposition of zinc tin oxide on flexible polyimide substrates. Chiang *et al.*[18] reported that the zinc tin oxide-active layer was grown using magnetron sputtering, and that field-effect mobility was enhanced by high temperature annealing (300 °C–600 °C). However, high-temperature annealing may become an incumbrance for actual production process. The gate insulator in TFT also significantly affects the TFT performance. The SiO_2 gate insulator is still a good insulator due to its higher stability than those of the HfO_2 and SiN_x.[19–22] SiO_2 can be deposited uniformly and has higher interface quality than Al_2O_3.[23] In this paper, we develop a simple and low temperature process to prepare highly transparent ZnSnO TFTs by using magnetron sputtering technique with a conventional SiO_2 gate insulator. The electrical properties of ZnSnO TFTs are studied using an analytical model.

2. Experimental details

The TFTs fabricated in this work each have a bottom gate configuration, which is shown in Fig. 1(a). Alkaline-free glass was used as a substrate on which a 60-nm thick indium tin oxide film (ITO) had been deposited. The gate insulator of SiO_2 was grown by plasma-enhanced chemical vapor deposition at 150 °C and had a thickness value of ∼ 100 nm. ZnSnO films were deposited with the ZnSnO alloy target (a mixture of ZnO and SnO_2 powder with a ZnO:SnO_2 mass ratio of 1:1) by radio frequency (RF) magnetron sputtering. The sputtering was performed in the ambience of Ar and O_2 mixed gas with a chamber pressure of 1 Pa. The partial pressure of oxygen was 0.1 Pa. The thickness values of the ZnSnO channel layers were 30 nm–40 nm. Source/drain electrodes were deposited with 100-nm thick indium oxide (In_2O_3) by RF magnetron sputtering. The width/length of the channel was $W/L = 200$ μm/50 μm. The TFT devices were patterned using lithography. To explore the annealing influence on the performance of TFTs, the TFT devices were annealed for 1 hour in vacuum at different temperatures of 150 °C, 200 °C, and

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250 °C, respectively.

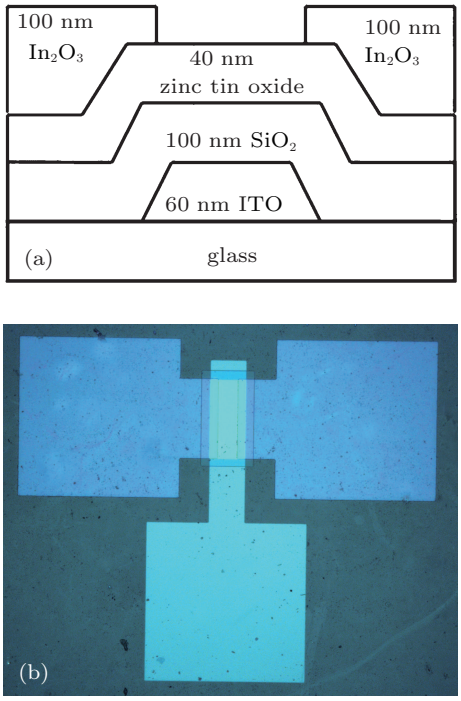


Fig. 1. (color online) (a) Schematic diagram of ZnSnO TFT structure and (b) optical image of the device structure (×100).

The crystal structural properties of the ZnSnO films were characterized by a D/max-A X-ray diffractometer (XRD) using CuK$_\alpha$ radiation. The surface morphologies of the films were measured by a scanning electron microscopy (SEM) with a Hitachi S-4800 model. The optical transmission was measured using the UV-3150 UV visible spectrophotometer. The electrical characteristics of the TFTs were measured using a Keithley 2612A semiconductor parameter analyzer. All the measurements were carried out at room temperature (RT).

3. Results and discussion

The SEM observation shows that the ZnSnO thin film deposited at room temperature by sputtering consists of small grains with several tens of nanometers (Fig. 2(a)). Figure 2(b) shows that the grains of the semiconductor channel layer annealed at 250 °C tend to aggregate. As shown in Fig. 2(c), the X-ray diffraction patterns of ZnSnO/ITO/glass demonstrate that the ZnSnO thin films annealed at different temperatures (from 150 °C to 250 °C) are amorphous. The broad peaks at around $2\theta = 25°$ originate from the glass substrate. ZnSnO films have optical band gaps of 3.3 eV–3.9 eV for different Zn compositions, appreciable electron mobility values, and high transparencies in the visible region, which indicates their potential applications in the fabrication of electronic devices.[17] The optical transmittance of the ZnSnO film is shown in Fig. 3(a), indicating that its average transmittance is ∼80% in the visible region. The high-transparency of TFT in which ZnSnO thin film is used as the channel presents a clear top-view of the optical image of "ZJU" that is under the TFT as shown in the inset of Fig. 3(a). The ZnSnO optical band gap is estimated from the transmittance data by extrapolating the linear part of the plot of $(\alpha E)^2$ versus E to $\alpha = 0$ (Fig. 3(b)), yielding 4.0 eV, which is close to that reported in Ref. [17].

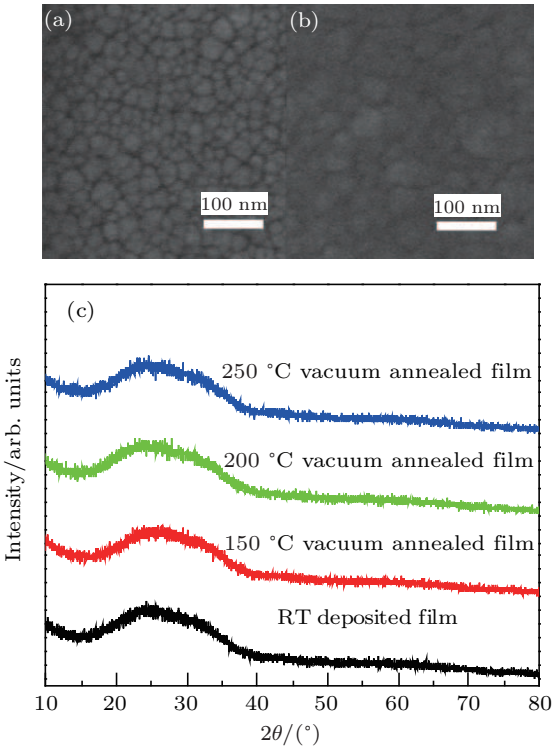


Fig. 2. (color online) SEM images of (a) as-deposited zinc tin oxide thin film and (b) zinc tin oxide film annealed at 250 °C, and (c) XRD patterns of ZnSnO thin films on glass.

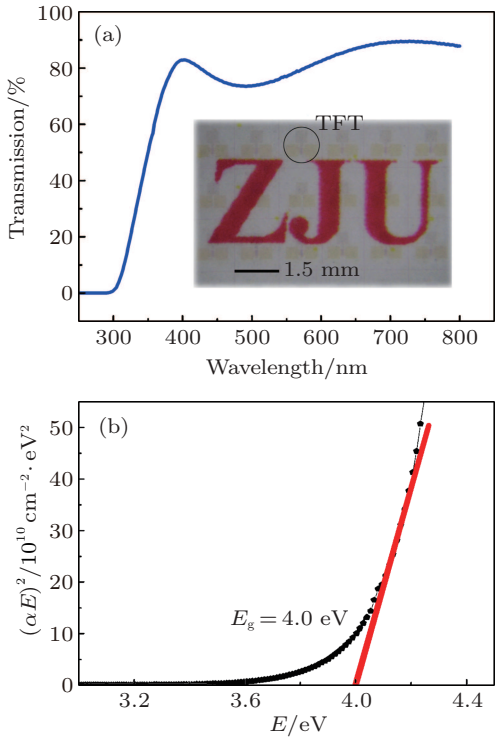


Fig. 3. (color online) (a) The transmission spectra of ZnSnO film deposited on a glass substrate, and a corresponding top-view optical image of "ZJU" underneath the TFT (inset). (b) Derivation of the optical band gap.

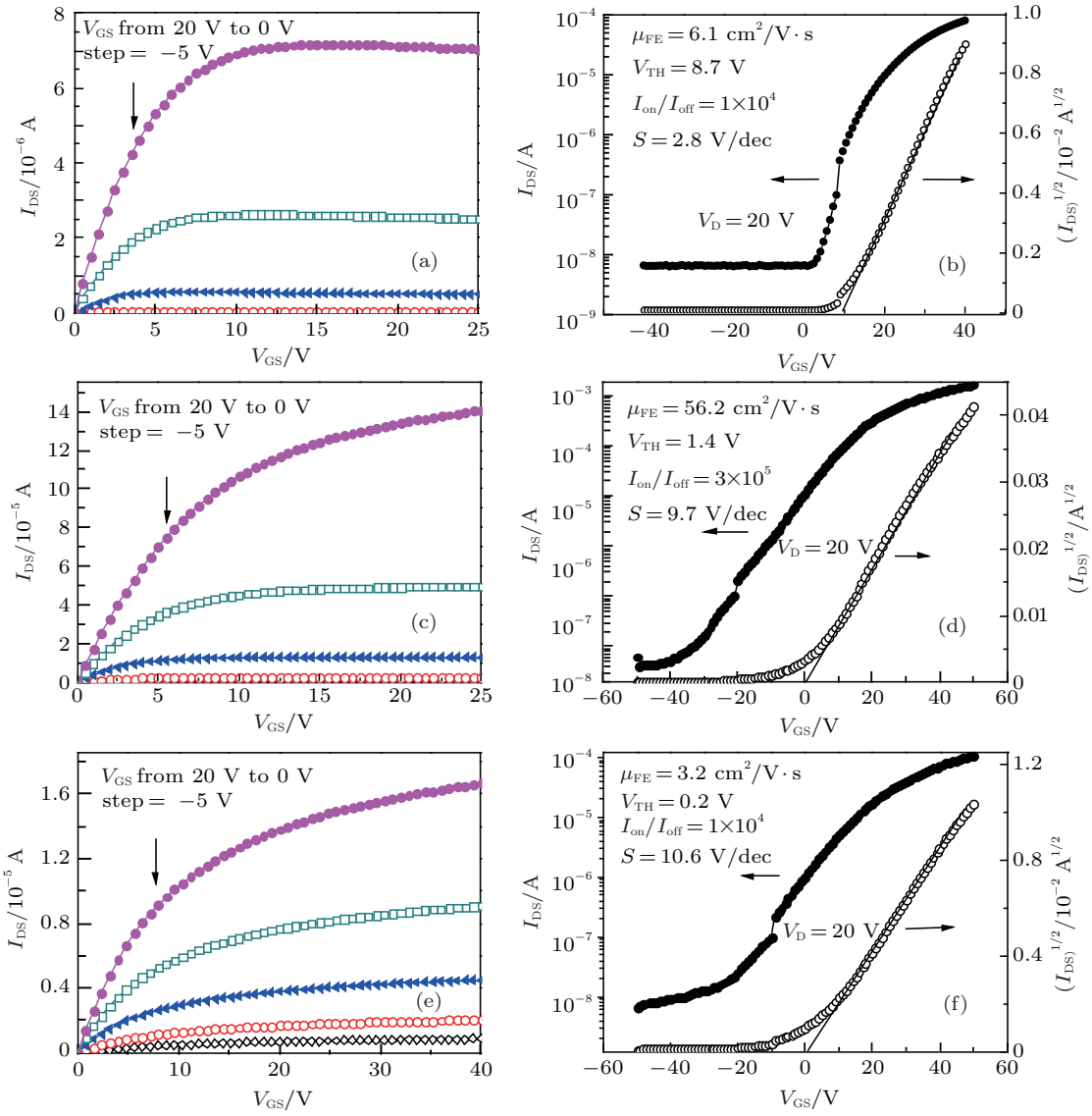


Fig. 4. (color online) Output characteristics of ZnSnO TFTs annealed at (a) 150 °C, (c) 200 °C, (e) 250 °C and transfer characteristics annealed at (b) 150 °C, (d) 200 °C, (f) 250 °C.

Figures 4(a), 4(c), and 4(e) show the output characteristics for the ZnSnO TFTs annealed at temperatures of 150 °C, 200 °C, and 250 °C, respectively. The gate voltage V_{GS} is varied from 0 V to 20 V in steps of 5 V. The output characteristics reveal that the devices each exhibit a nice pinch-off and good hard saturation. Maximum values of source/drain saturation current I_{DS} are obtained to be 140 μA on the sample annealed at temperature of 200 °C. Figures 4(b), 4(d), and 4(f) show the corresponding transfer characteristics $\log(I_{DS}) \sim V_{GS}$ and $\sqrt{I_{DS}} \sim V_{GS}$ for the ZnSnO TFTs annealed at different temperatures. We perform positive and negative voltage sweeps and observe small hystereses in transfer curves.[24] The saturation field effect mobility μ_{SAT} and the threshold voltage V_{TH} can be calculated from the transfer curve according to the formula,[25]

$$I_{DS} = \frac{W}{2L}\mu_{SAT}C_{SiO_2}(V_{GS} - V_{TH})^2, \quad V_{DS} > V_{GS} - V_{TH}, \quad (1)$$

where I_{DS} is the drain–source current, V_{GS} is the gate voltage, V_{DS} is the drain voltage, and W and L are the width and length of the channel. The thickness value of SiO_2 film is 100 nm, the dielectric constant of SiO_2 is 3.9, and the capacitance per unit area of the gate insulator (C_{SiO_2}) is 7.8 nF/cm^2. The parameters of ZnSnO TFTs are shown in Table 1. It is seen that the device characteristics are sensitive to the annealing temperature. The saturation field-effect mobility of the TFT annealed at 150 °C is 6.1 cm^2·V^{-1}·s^{-1}. After annealing at 200 °C, μ_{SAT} reaches a maximum value of 56.2 cm^2·V^{-1}·s^{-1}. The increase in mobility with the rise of annealing temperature from 150 °C to 200 °C presumably is attributed to the local atomic rearrangement and the improved bonding in the semiconductor layer.[26] The internal stress in the films may be relaxed and the densities of dislocation and point defects probably decrease in this annealing temperature range. The band structure below the conduction bottom may be modified, and a smaller fraction of the electrons from the source electrode, injected into the channel, could be trapped in the bulk trap centers. As the temperature further rises to 250 °C, the

evaporation of oxygen atoms in the ZnSnO thin film accelerates and the concentration of oxygen vacancies that act as ionized impurity centers may remarkably increase. Therefore, the decrease in μ_{SAT} is observed.[27] The threshold voltage values are 8.7 V, 1.4 V, and 0.2 V for the sample annealed at the temperatures of 150 °C, 200 °C, and 250 °C, respectively. The increase in the concentration of oxygen vacancies with the rise of annealing temperature contributes to the large negative shift in the threshold voltage, which is reported in Ref. [28]. Barquina *et al.*[29] also presented similar results for IZO TFTs, which show a large negative shift from $V_{TH} \cong 0.5$ V for the unannealed sample to $V_{TH} \cong -13$ V for the sample after 125-°C annealing.

Table 1. Electrical characteristics of the ZnSnO TFTs annealed at different temperatures.

Temperature /°C	μ_{SAT} /cm^2·V^{-1}·s^{-1}	I_{on}/I_{off}	V_{TH} /V	S /(V/dec)	N_{SS}^{max} /cm^{-2}
150	6.1	1×10^4	8.7	2.8	2.2×10^{12}
200	56.2	3×10^5	1.4	9.7	7.9×10^{12}
250	3.2	1×10^4	0.2	10.6	8.5×10^{12}

From the transfer characteristics, we also determine the gate voltage swing, S, through the following relation[25]

$$S = \frac{dV_{GS}}{d(\log I_{DS})}. \tag{2}$$

We further derive the maximum density of surface states at the semiconductor/dielectric interface as[25]

$$N_{SS}^{max} = \left(\frac{S\log(e)}{kT/q} - 1\right)\frac{C_{SiO_2}}{q}, \tag{3}$$

where k is Boltzmann's constant, T is the temperature, q is the electron charge, $\log(e)$ is the constant, and C_{SiO_2} is the gate insulator capacitance.

From Eqs. (2) and (3), the S values are evaluated to be 2.8, 9.7, and 10.6 V/decade, and N_{SS}^{max} are 2.2×10^{12}, 7.9×10^{12}, and 8.5×10^{12} cm^{-2} at the annealing temperatures of 150 °C, 200 °C, and 250 °C, respectively. The ZnSnO TFT annealed at 150 °C has the smallest S, which indicates the best gate control of device and the lowest trap density in the ZnSnO/SiO_2 interface.

In order to study the stabilities of ZnSnO TFTs, we measured the transfer characteristics of the TFTs at different drain voltages. Figure 5 shows the typical transfer characteristics for the ZnSnO TFTs annealed at 150 °C at the drain voltages ranging from 8 V to 22 V. We can see that the on-state currents of transfer characteristic curves change from 3.3×10^{-5} A to 6.78×10^{-5} A and the off-state currents change from 6.7×10^{-9} A to 7.1×10^{-9} A, which indicates that the ZnSnO TFTs display good stabilities.

To investigate the electrical properties of the ZnSnO-TFTs, an a-Si analytical model is used.[30] The transfer characteristics of TFTs are divided into four regions: an off region,

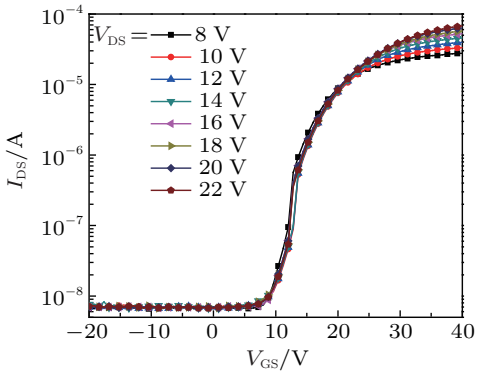


Fig. 5. (color online) Transfer characteristics of a ZnSnO TFT at different drain voltages annealed at 150 °C.

a reverse sub-threshold region, a forward sub-threshold, and an on region.[31] In the off region, the ZnSnO channel layer is fully depleted by the V_{GS}, and the wide band gap of the ZnSnO film makes the off current small. Taking into account the Poole–Frenkel effect in this region,[32] the current can be expressed by

$$I_{DS} = W\Delta L_D J_{OF}\exp\left(\frac{|V_{GS}|}{V_{FP}} + r_p V_{DS}\right), \tag{4}$$

where ΔL_D is the drain overlap length, J_{OF} is the effective current density when the electric field is zero, V_{FP} and r_p are the fitting parameters of the Poole–Frenkel emission. Considering the interface states, deep local states, and the amorphous material properties, we can describe the currents in the forward and reverse sub-threshold regions with the following expression:[33]

$$I_{DS}^{subf} = \frac{W}{L}I_{subo}\exp\left(\frac{V_{GS}}{S_f + \gamma V_{DS}} + r_a V_{DS}\right), \tag{5}$$

$$I_{DS}^{subr} = \frac{W}{L}I_{subo}\exp\left(\frac{V_{GS} - V_{TR}}{S_r} + r_n V_{DS}\right), \tag{6}$$

where γ is the fitting parameter that accounts for the lateral component of the electric field, S_f and S_r denote the forward and reverse sub-threshold slope, respectively. r_a and r_n are fitting parameters which are affected by V_{DS}.[34,35]

By considering the carrier saturation drift velocity effect, we obtain a model in the on region. The on region can be divided into linear region and saturation region and the currents yield:

$$I_{DS}^{lin} = \frac{W}{L}\mu_n C_{fm}\left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right], \tag{7}$$

$$I_{DS}^{sat} = \frac{W}{L}\mu_n C_{fm}\left[\sqrt{(V_{GS} - V_{TH})^2 + \left(\frac{v_{max}L}{\mu_n}\right)} - \left(\frac{v_{max}L}{\mu_n}\right)\right]\frac{v_{max}L}{\mu_n}, \tag{8}$$

where C_{fm} is the capacitance per unit area of the dielectric layer and v_{max} is the maximum velocity of the electrons in the

ZnSnO channel. Table 2 presents the extracted parameters of the analytical models in different regions for the TFT. Figure 6 shows the simulated and measured transfer characteristics for V_{GS}, ranging from −20 V to 40 V at $V_{DS} = 10$ V for a ZnSnO TFT annealed at 150 °C. We can see that the simulated transfer characteristics are in good consistence with the measured data.

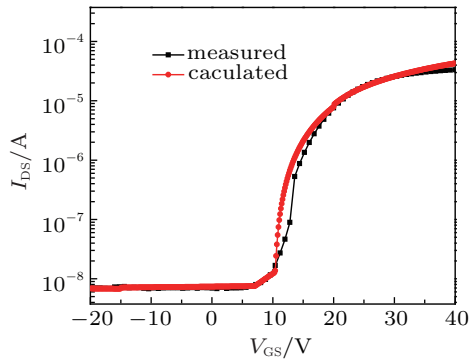


Fig. 6. (color online) Measured and calculated transfer characteristics of the ZnSnO TFT at $V_{DS} = 10$ V annealed at 150 °C.

Table 2. Parameters of the analytical model for the ZnSnO TFT.

	Parameter	Value	Unit
Linear region	W/L	200/50	–
	μ_n	5.5	$cm^2/(V{\cdot}s)$
	C_{fm}	7.7778×10^{-9}	F/cm^2
	V_{TH}	10	V
Saturation region	v_{max}	1.8×10^6	cm/s
Forward sub-threshold region	S_f	0.843	V
	γ	0.524	–
	r_a	−0.7878	V^{-1}
	I_{sub0}	1.548635×10^6	A
Reverse sub-threshold region	S_r	400.885	V
	r_n	1.068	V^{-1}
	I_{rsub0}	4.078098×10^{-14}	A
	V_{TR}	−15	V
Off-state region	V_{FP}	−534.76	V
	r_p	−0.025685	V^{-1}
	$W\Delta L_D J_{OF}$	8.5215×10^{-9}	A

4. Conclusion

We fabricate transparent oxide TFTs each using ZnSnO as an active layer and SiO_2 as a gate insulator. Annealing at 200 °C leads to good electrical performance with a maximum mobility and on/off ratio of 56.2 $cm^2/(V{\cdot}s)$ and 3×10^5, respectively. The devices also show good stabilities in performance. Room temperature deposition and the low temperature annealing process are significant advantages of the fabrication of the transparent electronic devices. The transfer characteristics are simulated using an analytical model and good agreement between measured and calculated transfer characteristics is demonstrated.

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