Bipolar tri-state resistive switching characteristics in Ti/CeO_x/Pt memory device

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Highly repeatable multilevel bipolar resistive switching in Ti/CeO_x/Pt nonvolatile memory device has been demonstrated. X-ray diffraction studies of CeO_2 films reveal the formation of weak polycrystalline structure. The observed good memory performance, including stable cycling endurance and long data retention times ($> 10^4$ s) with an acceptable resistance ratio ($\sim 10^2$), enables the device for its applications in future non-volatile resistive random access memories (RRAMs). Based on the unique distribution characteristics of oxygen vacancies in CeO_x films, the possible mechanism of multilevel resistive switching in CeO_x RRAM devices has been discussed. The conduction mechanism in low resistance state is found to be Ohmic due to conductive filamentary paths, while that in the high resistance state was identified as Ohmic for low applied voltages and a space-charge-limited conduction dominated by Schottky emission at high applied voltages.

Keywords: multilevel resistive switching, Schottky emission, cerium oxide, oxygen vacancy

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1. Introduction

Nonvolatile memory for multilevel storage has been extensively exploited in portable electronic products.[1–4] However, traditional nonvolatile floating gate memory devices have confronted some physical limits as they are continuously scaled down.[5–7] Resistive random access memory (RRAM) is being considered as one of the potential candidates for development of the next generation nonvolatile memory because of its advantages such as low energy consumption, high density, simple device structure, and intrinsic fast switching speed.[8–10] RRAM devices are based on conductor–dielectric–conductor sandwich structures which can reversibly be switched between two distinct resistance states by applying appropriate voltage.[11,12] In contrast to the conventional memory switching between the two resistance states (HRS and LRS), another kind of switching is also possible where device resistance switches between three or more levels, known as multilevel resistive switching (RS). Multilevel RS enhances storage capability which eventually leads to higher packing density of memory.[13] Many researchers have studied multilevel set/reset and tri-state RRAM devices based on rare earth/transition metal oxides.[14–17] Multilevel resistive states are usually achieved either by controlling the current compliance during the SET process or by limiting the amplitude of the voltage pulse during the RESET process. However, in our device (present study), tri-level resistance states were achieved via controlling the set and reset voltages. That is why physical origin of multilevel resistive switching is different in dissimilar devices. The multilevel bipolar switching in Cu/TaO_x/Pt device has been reported by Yang *et al.*[17] which was suggested due to the coupling effect between existing resistive switching mechanisms. On the other hand, a research group at Peking University has explained the multilevel bipolar resistance switching mechanism in Al/CeO_x/Pt device[15,16] in terms of formation and rupture of conducting filaments composed of oxygen vacancies. Therefore, a deep understanding of characteristics and mechanism of multilevel set/reset resistive switching in oxide-based memory structures is still a challenge to be addressed for potential nonvolatile RRAM applications.

In this study, multilevel bipolar RS characteristics in the nonstoichiometric CeO_x-based RRAM device with different top electrode as reported earlier[15,16] are being demonstrated. Bipolar resistive switching behavior in our Ti/CeO_x/Pt memory device retains stable resistance ratio of approximately $\sim 10^2$ with switching response for more than 3×10^2 cycles. It is expected that the top electrode reacts with the CeO_2 layer and forms an interfacial TiO_x layer. This oxygen-rich top interface area might play a key role in the formation and rupture of conductive filaments during multilevel resistive switching.

2. Experimental procedure

In this work, Ti/CeO_2/Pt-based MIM sandwich structures were fabricated. Ceria (CeO_2) films of 30 nm were deposited

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on Pt/Ti/SiO_2/Si substrates at room temperature using radio frequency (rf) magnetron sputtering of a ceramic CeO_2 target. Ceria film was prepared at a fixed rf power of 100 W and with argon:oxygen (6:12) flow rate of 20 sccm. The working pressure during deposition was kept at 10 mTorr (1 Torr = 1.33322×10^2 Pa). To complete the metal–insulator–metal structure, a 50-nm thick Ti top electrode was deposited by electron beam evaporation at ambient temperature with a diameter of 150 μm patterned through a metallic shadow mask. Pt film (20 nm) was used to avoid the oxidation of Ti electrode and to prevent it from scratching by the probe during electrical characterization. Electrical characteristics of the fabricated CeO_2-based resistive memory devices were measured at room temperature by Agilent B1500A semiconductor parameter analyzer. During electrical characterization, the bias voltages were applied to the Ti top electrode (TE) while the Pt bottom electrode (BE) was grounded. Crystal structure of the CeO_2 thin films was characterized by X-ray diffraction (XRD) in the 2θ range of 20°–80°.

3. Results and discussion

Figure 1 shows typical 3°-glancing angle XRD spectrum of CeO_2-based RRAM device fabricated on Pt/Ti/SiO_2/Si substrate. It depicts some broad peaks indicating that CeO_2 film possesses weak polycrystalline structure having only (111), (200), and (220) reflections corresponding to the diffraction angles 28.5°, 33.08°, and 47.5° respectively, yielding "fluorite cubic structure of CeO_2" (JCPDS #: 34-0394). The broadening of preferred orientation (111) reflection may be caused by the significant reduction in grain size[18] as well as very small thickness of CeO_2 film (30 nm). In addition, a few weak reflections are also visible in this spectrum which can be assigned to (100), (111) planes of TiO (JCPDS #: 82-0803). This fact might lead to the formation of a thin TiO_x interfacial layer. Such a kind of layer has been observed

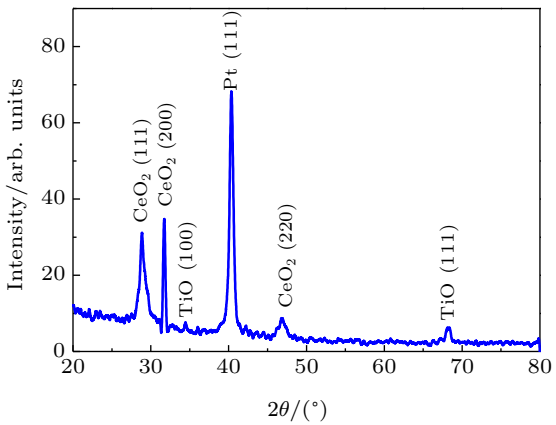


Fig. 1. (color online) XRD pattern of the fabricated Ti/CeO_x/Pt memory device at room temperature.

by Zhao *et al.*[19] in Ti/Dy_2 O_3/Pt device (also confirmed by TEM analysis), because Ti possesses strong oxygen affinity so oxygen ions from adjacent oxide layers tend to migrate to Ti/CeO_2 interface yielding a weak polycrystalline TiO_x interlayer.

Figure 2 illustrates the current–voltage (I–V) characteristics of the Ti/CeO_x/Pt memory device which exhibits tri-stable resistive switching behavior. Initially, a forming process is required for triggering the fresh CeO_2-based device to demonstrate the reversible resistive switching behavior, as shown in the inset of Fig. 2. It is believed that in this initial step, a positive voltage ($\sim$ 12 V) applied to the top electrode strongly attracts oxygen ions and causes the formation of oxygen vacancies in the bulk of CeO_2 layer. These positively charged oxygen vacancies align along the direction of current flow under the influence of the initial voltage sweep, create conducting filamentary path(s) between the two electrodes causing a sudden rise of current analogous to soft breakdown. This process, known as "electroforming" occurs at 9.85 V under the compliance current of 10 mA. After the forming process, a negative voltage sweep (0 V to −3 V) switches the device from low resistance state (LRS) to intermediate resistance state (IRS) at about −1.9 V, and then to high resistance state (HRS) at $\sim$ −2.5 V. In the proceeding positive bias sweep (0 V to +6 V), an abrupt rise in current occurs again at a specific voltage of 5.1 V (set voltage), indicating the switching of resistance from HRS to LRS. Obviously, our Ti/CeO_x/Pt device requires the same switching polarity in each set or reset cycle; as a positive bias induces the low resistance set state (LRS) and negative bias is responsible for the intermediate resistance state and hence the high resistance reset state (HRS). This tri-stable resistance switching behavior is reversible and controllable. Figure 3 shows multilevel set and reset resistive switching in a more convenient way. By sweeping the bias from 0 V to +6 V, a two-step set process is observed (Fig. 3(a)): "set-1" switches the device from HRS to IRS at voltage of 1.9 V, ($V_{\text{set-1}}$), while "set-2" further switches the device from intermediate resistance state to low resistance state at 3.2 V ($V_{\text{set-2}}$). A current compliance of 10 mA was adopted to protect the device from hard dielectric breakdown. In order to switch the device back to HRS, biasing voltage with reverse polarity is necessary. The reset process in Fig. 3(b) is also divided into two steps; "reset-1" switches the device from LRS to IRS at −1.3 V ($V_{\text{reset-1}}$), and "reset-2" from IRS to HRS at −3.5 V ($V_{\text{reset-2}}$). These results propose that the as-deposited CeO_2 devices have some meta-stable IRSs. To obtain multi-bit resistive random access memory (RRAM) device, these multilevel SET and RESET processes may be useful.[3,20]

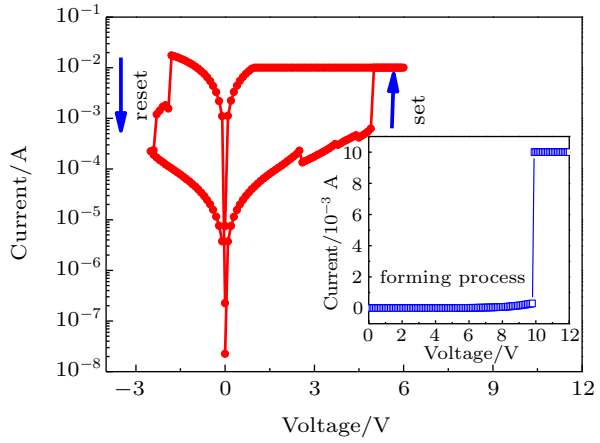


Fig. 2. (color online) Typical bipolar tri-state resistive switching *I*–*V* characteristics of Ti/CeO$_x$/Pt device (Inset illustrates initial forming process).

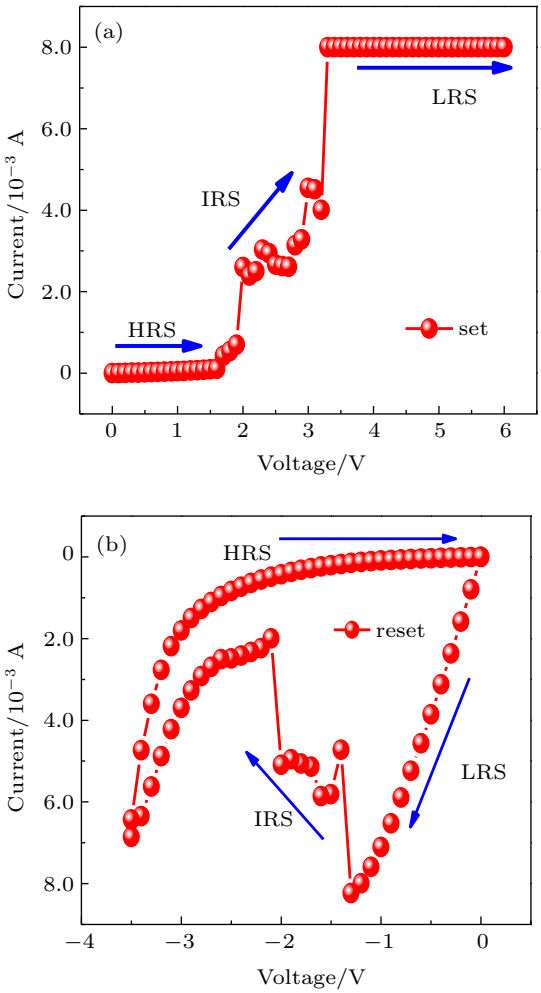


Fig. 3. (color online) Multilevel (a) set and (b) reset process in the Ti/CeO$_x$/Pt RRAM device.

The endurance properties of our Ti/CeO$_x$/Pt memory device are shown in Fig. 4(a). The HRS and LRS were both extracted at 0.3 V. It is worth mentioning that both HRS and LRS are stable over successive 3×10^2 switching cycles at room temperature. The ratio of resistances between the two memory states is approximately 10^2. To further demonstrate the stability of resistive switching properties, data retention was determined by measuring the current level of our device in the ON- and OFF-states over a long period of time ($> 10^4$ s) at room temperature. The results shown in Fig. 4(b) clearly illustrate that both the LRS and HRS are stable for about 3.5×10^3 s with well-resolved ON/OFF ratio of ~ 100 with a slight degradation in HRS during last 500 s. This slight deterioration in retention behavior might be due to local damage of the active layer.

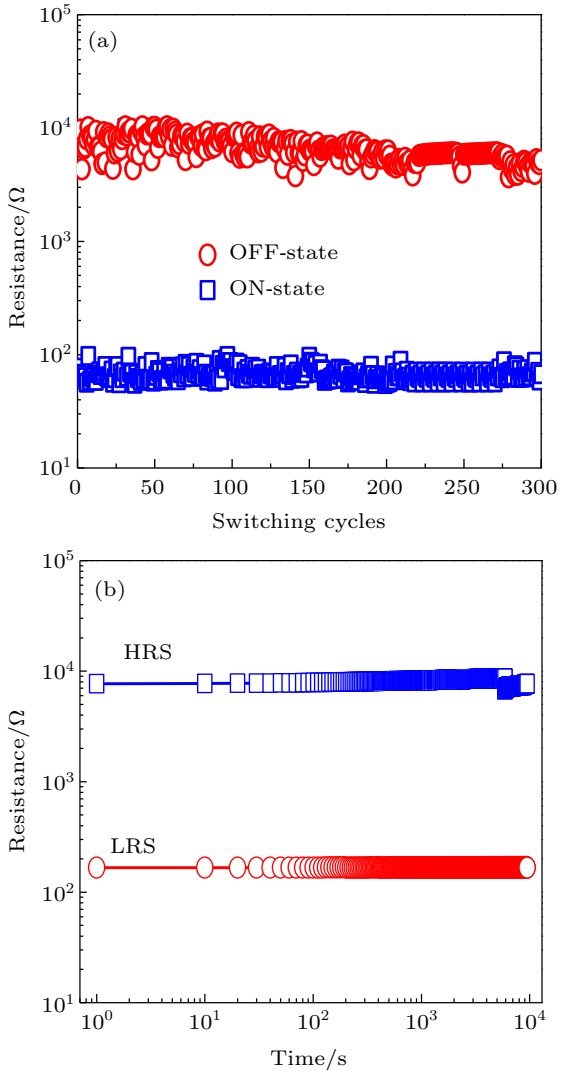


Fig. 4. (color online) Reliability of the proposed CeO$_x$-based RRAM: (a) The endurance characteristics for up to 300 cycles measured at $V_{\text{read}} = 0.3$ V for Ti/CeO$_x$/Pt device, (b) retention characteristics of the Ti/CeO$_x$/Pt device.

Figure 5(a) shows the statistical distributions of resistance in HRS, IRS, and LRS in dc sweeping modes. The distribution range of HRS, IRS, and LRS of our devices are from 49.7 Ω to 86.2 Ω, 1.3×10^3 Ω to 7.8×10^3 Ω, and 5.2×10^3 Ω to 1.9×10^4 Ω respectively. It is quite evident that the fluctuations in the HRS, IRS, and LRS are very small. Figure 5(b) shows typical cycle-to-cycle variation of the switching parameters of Ti/CeO$_x$/Pt device. The statistical data is taken over first 100 dc endurance cycles. Cumulative probability plot

for the set/reset voltages shows relatively uniform distribution with small Weibull slope as most values for the set voltage (V_{set}) range between 1.92 V and 3.62 V while for reset voltage (V_{reset}) they are mostly concentrated between −1.0 V and −1.90 V. The V_{set} and V_{reset} distributions demonstrate relatively stable turn-on and turn-off processes.

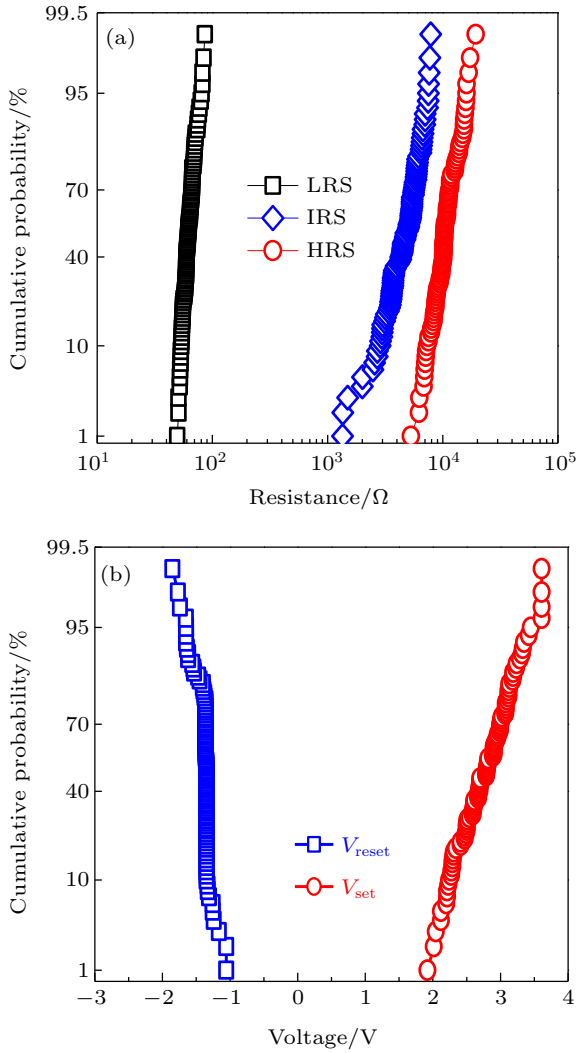


Fig. 5. (color online) (a) Statistical distributions of the resistances in HRS, IRS, and LRS measured during the voltage sweep operation up to 300 cycles in Ti/CeO_2/Pt device, (b) statistical voltage distributions (V_{set} and V_{reset}) operated by bipolar resistive switching operations for the Ti/CeO_x/Pt device.

To elucidate the resistive switching behavior of our Ti/CeO_x/Pt device, electrical conduction properties in both the HRS and LRS were analyzed systematically. Plots of log$I$–log$V$ in the positive bias region are shown in Fig. 6(a). Conduction in the LRS is Ohmic because the I–V curve is linear with a slope of ∼ 1, which is typically due to the creation of conductive filaments in CeO_x layer. However, at the HRS, the I–V characteristics are much more complicated and can be divided into three parts; within the low voltage range < 0.9 V (region-I) slope of log$I$–log$V$ plot is 1.07 which indicates Ohmic conduction due to thermally generated free electrons.[21] This may also be due to filamentary conduction

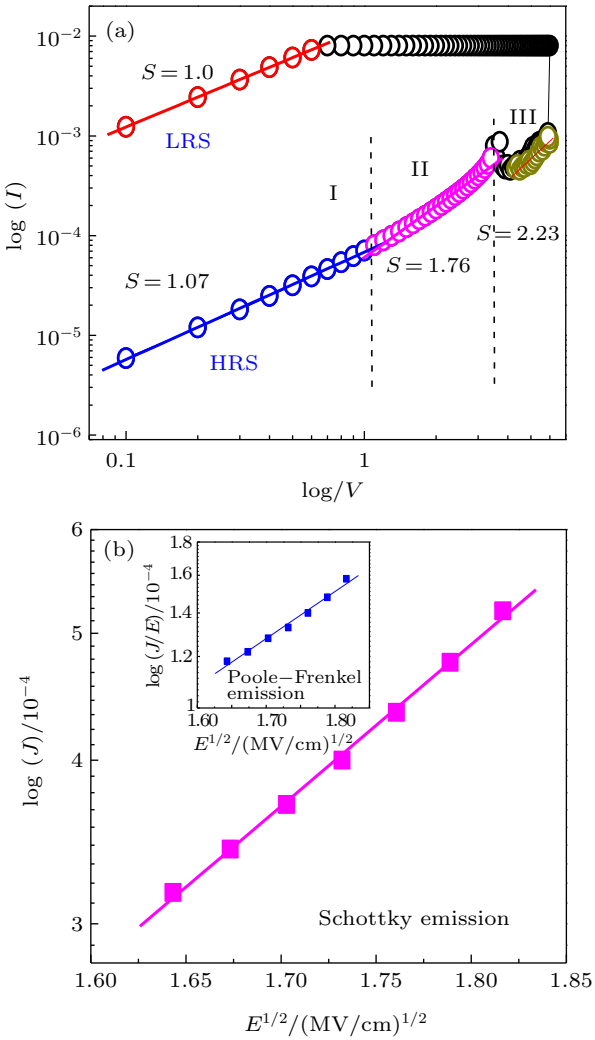


Fig. 6. (color online) (a) The double logarithmic I–V plots of both HRS and LRS for the Ti/CeO_x/Pt device. (b) Schottky emission linear fit curve at high voltage region in the HRS (Inset does not follow the Poole–Frenkel emission at high voltage region in the HRS).

of the accumulated oxygen vacancies into cerium oxide layer.[22] Moreover, Ohmic conduction is expected due to partial filling of traps during weak injection of charge carriers[23] from the bottom electrode Pt. On the other hand, in region-II, slope of log$I$–log$V$ plot is 1.76 which might lead to trap-filling region because of increasing the injected electrons with applied bias which are captured by the traps (oxygen vacancies etc.) in the CeO_x layer. As traps in the CeO_x are all occupied by injected carriers, current enters into region-III. In addition, at the same time the Ti/CeO_x interface keeps on extracting oxygen ions, thereby increasing the domain of oxygen vacancies (traps) in the bulk of CeO_x. This may lead to the intermediate state, where either current decreases or remains almost constant. But in region-III, on further increasing the applied bias, more electrons will be injected from the Pt electrode because the bulk CeO_x layer is incapable of supplying the excess electrons, as a result the space charge begins to form the injecting electrode interface. Thus in the high voltage region-III (> 2 V), the conduction mechanism may be attributed to trap-controlled space-charge-limited current

(SCLC).[24] Moreover, in region-III (with a slope of 2.23), the better linearity of log (J) versus $E^{1/2}$ plot as compared to that of log (J/E) versus $E^{1/2}$ plot and the mechanism discussed above indicate that the conduction mechanism is more consistent with Schottky emission as compared to Poole–Frenkel mechanism.[25]

Based on the above analyses, the multilevel set and reset bipolar resistive switching in Ti/CeO_x/Pt device is schematically illustrated in Fig. 7. Multilevel set and reset characteristics can be well explained based on the nonstoichiometric distribution characteristics of oxygen vacancies in Ti/CeO_x/Pt device. CeO_2 is a material with multiple oxidation states (+3 and +4). The weak polycrystalline nature of ceria films may create variations in the lattice strain which could initiate interplay between the two oxidation states resulting in the formation of oxygen vacancies as a charge compensation. In fact the formation energy at oxide surface is relatively low, so the concentration of oxygen vacancies at the surface can be expected to be higher than that in the bulk of the sandwiched oxide.[26] Moreover, as Ti is capable to reduce CeO_2 so probability of a relatively richer density of oxygen vacancies near the Ti/CeO_x interface is rather enhanced. While being nobel metal, the bottom electrode (Pt) is incapable of creating an appreciable amount of oxygen vacancies near the Pt/CeO_x interface. The resulting non-uniform density of oxygen vacancies in the oxide layer leads to bipolar resistive switching in Ti/CeO_x/Pt device. Furthermore, the formation of TiO_x layer seems to play a significant role in the distribution and movement of oxygen vacancies as well as in the conductive filament formation/rupture. As fresh RRAM device needs the electroforming process before showing any reversible resistance switching. During forming process, the positive voltage stress applied at the top electrode pushes the positively charged oxygen vacancies from the TiO/CeO_x interface into the vacancy deficient CeO_x bulk to form separated line-pattern conductive filaments. This happens because oxygen vacancies have ability to distribute themselves in line-pattern between electrodes rather than an interconnected network of filaments and are separated from one another due to impulsive interactions.[15,27,28] In the subsequent reset process, the negative bias applied to top electrode pulls oxygen vacancies back to the TiO/CeO_x interface from the bulk and oxygen ions towards the bulk, thus rupturing the filament(s) as illustrated in Fig. 7. The filamentary model explains the multilevel resistive switching mechanism as well. Because of the asymmetric distribution of oxygen vacancies in the active oxide layer, a filament after its formation in the set step is not likely to increase in scale. That is why the resistance of the device with only one filament may be intermediate until some additional filaments are formed at other locations when stronger biasing voltage is applied. The formation of multiple, and mutually separated, percolation paths between the two electrodes switches the device from the intermediate resistance state to low resistance state. It is noteworthy that if filamentary conduction paths were mutually connected (interconnected network of filaments), there would be practically no difference in resistance levels of the LRS and the IRS.

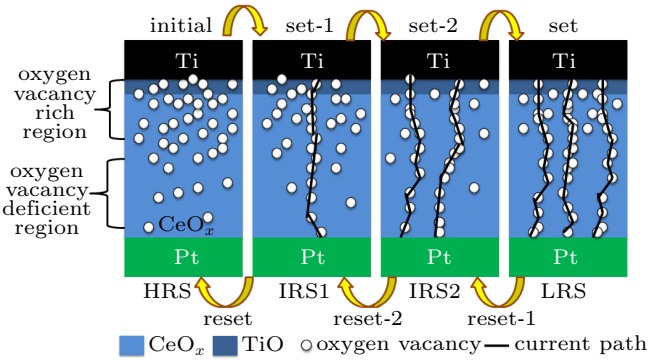


Fig. 7. (color online) Illustration of the proposed physical model to explain bipolar switching mechanism in the CeO_x-based RRAM device for the multilevel set and reset processes.

4. Conclusion

Nonstoichiometric CeO_x-based memory device successfully demonstrated multilevel set/reset bipolar resistive switching behavior. X-ray diffraction pattern confirmed that nature of the CeO_2 films is weak polycrystalline as well as the formation of a thin TiO layer. The observed multilevel stable intrinsic resistance states of CeO_x could be attributed to formation of separated line-pattern oxygen vacancy filaments in the CeO_x film. The conduction mechanism in the LRS is of Ohmic type, whereas in HRS it can be explained by Ohmic and trap-controlled space-charge-limited conduction dominated by Schottky emission. The reliability of resistive switching characteristics and data retention (10^4 s) were also verified at room temperature. The multilevel resistive switching in Ti/CeO_x/Pt devices may be considered for multi-bit memory storage applications. The highly stable switching behavior in Ti/CeO_x/Pt device has a great potential for nonvolatile memory applications.

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