Afterpulsing characteristics of InGaAs/InP single photon avalanche diodes*

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InGaAs/InP single photon avalanche diodes (SPADs) are more and more available in many research fields. They are affected by afterpulsing which leads to a poor single photon detection probability. We present an InGaAs/InP avalanche photodiode with an active quenching circuit on an application specific integrated circuit (ASIC). It can quench the avalanche rapidly and then reduce the afterpulse rate. Also this quenching circuit can operate in both free-running and gated modes. Furthermore, a new technique is introduced to characterize the influence of the higher order of afterpulses, which uses a program running on a field programmable gate array (FPGA) integrated circuit.

Keywords: single photon detection, active quenching, afterpulse, quantum key distribution

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1. Introduction

Since the mid-1990's, single photon detection has been increasing importance at telecom wavelengths in many research fields, such as quantum key distribution,[1] optical fiber characterization,[2] optical time domain reflectometry,[3,4] non-invasive testing of VLSI circuits,[5] and single-molecule detection.[6] Generally, there are several candidates for free-running single photon detectors (SPDs) in the telecom wavelength range. Among all these candidates, transition edge sensors (TES)[7] and superconducting nanowire single-photon detectors (SNSPDs)[8,9] are the best free-running SPDs. Although the TESs have virtually no dark counts, they are very slow in response speed. The SNSPDs show the best overall performance which can provide low dark count rates (DCR$<$ 100 Hz) as well as good timing jitter ($<$ 65 ps). However, they remain impractical for most applications because of requirements for cryogenic cooling ($<$ 4.2 K). For this reason, SPAD is currently the best option for practical applications because of its high performance, reliability, compactness, and low cost. The SPAD has a relatively high photon detection efficiency ($\sim$30%),[10] meanwhile, the dark count rate ranges from $\sim$1 kHz to a few tens of kHz. Also the timing jitter of the detector is very low ($<$ 100 ps). Compared with the SNSPD, SPAD can easily achieve a typical operation temperature range ($-$210 K–260 K) by using the Peltier cooling. However, the SPAD suffers the afterpulsing badly and has a high noise level.[11]

Commonly, in order to reduce the afterpulse effect and the dark count rate, InGaAs/InP SPAD needs to be operated in the gated mode.[12–14] In this mode, the diode is applied with a bias voltage beyond its breakdown voltage for a short time window where photons can only be detected. However, this is incompatible with free-running operation,[15] which requires active or passive quenching[16] when photons arrive in a random fashion such as asynchronous and continuous wave (CW) photon counting. While the passively quenched SPAD introduces a significant parasitic capacitance and has a lower photon detection efficiency, and impairs the photon-timing resolution. It has been suggested that an active quenching must be used in the asynchronous mode.[17]

In this paper, we present an InGaAs/InP single photon avalanche diode with an active quenching circuit on ASIC. It can operate in both gated and free-running modes. With this active quenching method, we can minimize the parasitic capacitance and rapidly quench the avalanche. Then we introduce an innovative technique, which uses a program running on FPGA, to measure the afterpulsing distribution as a function of time. With this method, we can set the parameters in the software controlling the FPGA so that the afterpulsing behavior can be characterized accurately, quickly, and automatically. Moreover, it is possible for us to analyze the importance of the higher orders of afterpulses with the help of FPGA.

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2. Setup and the presentation of the ASIC

When SPADs are operated in a free-running mode, active quenching circuit can be used. In the active quenching regime, there is a remote circuit which can sense the rise of the avalanche pulse and react back on the SPAD and thus reduce the voltage below breakdown so that the avalanche can be quenched quickly. Then the operating voltage is reset in a short and well defined time called hold-off time. Ideally, in order to reduce the influence of afterpulses, the time during this feedback loop should be reduced as much as possible. With a short hold-off time, the number of trapped carriers is limited due to the fact that the current flowing through the diode is stopped quickly, thereby reducing the afterpulse rate. InGaAs/InP SAPD is generally cooled with a multistage Peltier element. Considering the power consumption, the quenching circuit composed of discrete components cannot be placed in the box where the APD is cooled. Because of this, the quenching time increases and then influences the performance of the detector. Furthermore, the APD must be connected to the circuit by cables. The impedance mismatch can make signal reflections occur.[18] So when the detector is switched on, the efficiency of single photon detection and the timing resolution can be changed because of the nonuniformity of the applied voltage during being gated.

With the ASIC, the electronic circuit can be placed close to the APD so that we can minimize the parasitic capacitance. The circuit is developed to operate in either a gated or free-running mode and the principle of its operation is illustrated in Fig. 1.

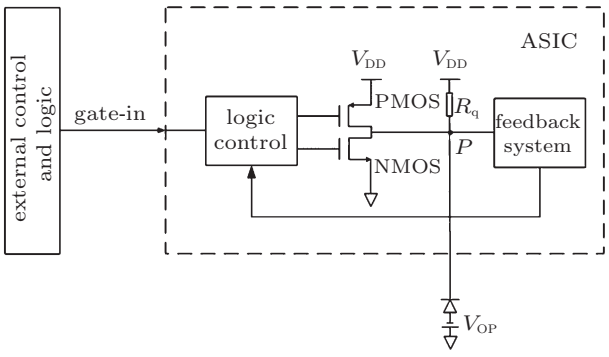


Fig. 1. Simplified diagram of the electronic control and active quenching circuit and its connection to the avalanche photodiode.

From Fig. 1 we can see that there are three key components: the external control, logic control, and a feedback system. Signals from the gate-in are converted into two pulses by level shifter in the logic control. Two correlated pulses generated by level shifter output pulse can control p-metal-oxide semiconductor (PMOS) and n-type MOS (NMOS) switches. In order to let the two switches do not operate at the same time, a short delay should be provided between the two pulses. At first, the PMOS switch is closed with a short duration charge pulse so that the APD cathode (P) is charged up to V (V_{DD}). After that, the PMOS switch is opened again. In the gated mode, the APD must be operated in the Geiger mode, i.e., the APD must be biased beyond its breakdown voltage V_{bd}. Then we can figure out that the voltage difference between the APD cathode and anode is $V_{bv} = V_{DD} + |V_{OP}|$ which exceeds its breakdown voltage V_{bd}. On the other hand, the NMOS switch remains open until the end of the gate when no avalanche is triggered, or until the active quenching after a triggered avalanche by a photon. If an avalanche is triggered during being gated, the current flow across the APD increases quickly. As a result, the voltage drop over the resistor R_q increases. The voltage drop at quenching point P is $V_{ex} = V_{DD} + |V_{OP}| - V_{bd}$, which equals the excess bias voltage. In the feedback system, there is a comparator and a following circuit that rapidly senses the voltage drop at P and immediately sends an active quenching feedback signal to the internal control logic. The NMOS switch is then closed and results in dropping the voltage at P down to zero. Therefore, an active quenching of the avalanche is completed. In the free-running mode, the gate in signal is no longer needed and the power supply voltage V_{DD} is applied to the cathode of the APD until an avalanche is triggered. More technical description about the ASIC operation can be found in Ref. [19].

3. Afterpulse characterization with an FPGA

Commonly, the well-known technique for measuring the afterpulse characterizations is double-window technique[20] which provides the decay curve of minority carriers trapped in the deep levels. However, higher orders of afterpulses induced by the trapped carriers which are generated by the former afterpulse cannot be characterized with the double-window technique. This phenomenon can make a difference from the afterpulsing behavior and then change the performance of the detector. We implement a process governed by an FPGA for free-running actively quenched APDs to characterize this higher orders phenomenon.

Figure 2 shows the logical behavior of the FPGA in the measurement of afterpulses. In order to ignore the effects of dark counts and the trapped carriers originating from a previous avalanche, the FPGA needs to wait until there are no avalanches detected for a fixed time (10 μs corresponding to 500 waiting cycles is used).

A pulse generator with a clock frequency of 50 MHz is used to trigger the FPGA. The time-bin, i.e., the temporal in-

terval used to discretize the data in a histogram, is a multiple of the inverse clock frequency. Therefore, the choice of the width of the time-bin is included in the selection of the triggering frequency. In this paper, the time-bin is 20 ns due to the triggering frequency of 50 MHz. If a wide acquisition range of the histogram is needed for an experiment, the resolution should be reduced accordingly.

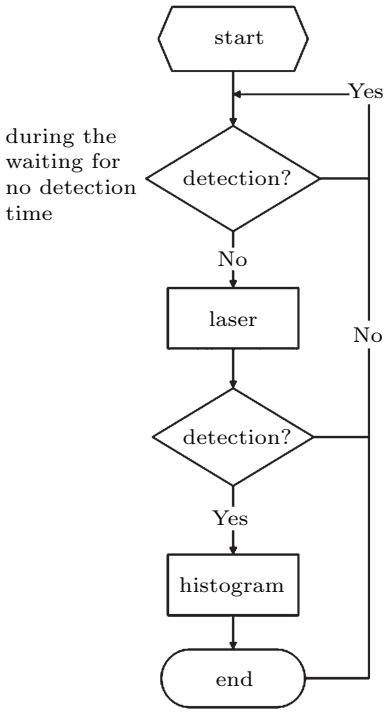


Fig. 2. Logical behavior of the FPGA in the measure of afterpulses.

At the beginning, the FPGA waits for several time-bins (10 μs) to put the APD in a well-defined state. If there are no detections during the time-bins, then the FPGA sends a pulse to trigger the laser. Instead, if there is a detection, the algorithm is restarted. When the photons in the laser pulse are sent into the APD, there is a probability of whether triggering an avalanche or not. Therefore, after sending the laser pulse, the FPGA waits for an appropriate delay and then checks whether the avalanche induced by the laser pulse has been detected. In this case, if there is a detection, the FPGA starts to wait for one or more detections which are induced by afterpulses or dark counts. Then the detections performed during the following 250 time-bins are registered into a 250-bin-histogram. In this way, the higher order phenomena can be characterized by recording all the afterpulses occurring after the laser detection. Otherwise, the algorithm of the logic behavior of the FPGA is restarted. The result of this measure is shown by a histogram of the afterpulse probability versus time. We should know that between two different laser pulses there are at least two delays in this measure. One is the delay for the FPGA to wait until no avalanche and the other is the length of the histogram. In order to remove the problems with afterpulsing induced by the former laser pulse, the total delay should be long enough so that the current carriers due to the previous avalanches, can be released adequately. In this case, the sum of all the delays of 60 μs, which involves a time of 10 μs needed to wait for no detection and a histogram of 50 μs, is chosen.

Figure 3 shows the measurement set-up. Both of the pulse generator and the FPGA can generate signals. After being triggered by the pulse generator, the FPGA sends a synchronized pulse to the AND-gate in which it passes through, with the pulse sent by the pulse generator. Then a 1550-nm laser diode triggered by the signals out of the AND-gate sends a laser pulse to a variable attenuator in order to have, on average, one photon per pulse. A 50/50 fiber beam splitter (BS) is used to split the laser pulses in order to monitor the laser power in real time by the power meter. After that, whether the diode impinged by the photons in the laser pulse could trigger an avalanche can be discriminated by the discriminator.

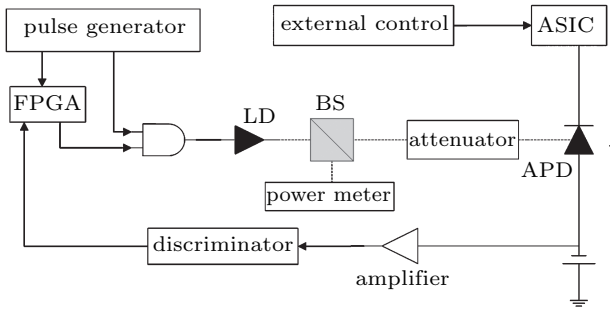


Fig. 3. Experimental set-up used to measure the afterpulses with the FPGA triggered by a pulse generator.

With this measurement, we can determine when the laser pulse is sent to the APD using the FPGA. Besides, after the first detection the FPGA whose settings are set by the users can wait for all the afterpulses for quite a long time in order to include the higher order pulses. In consideration of the veracity of the detector efficiency, the higher order afterpulses, which can increase the detections improperly, should be taken into account.

FPGA can be used to provide different biases and different values of dead time $\tau_{\rm d}$ in order to investigate the total afterpulse probabilities. After a 60-μs delay, the afterpulses originating from earlier avalanches can be reduced to a very low level which can be neglected. The total afterpulse probability can be calculated as follows:

$$P_{\rm total} = \sum_i \left(\frac{C_i}{C_{\rm d}} - r_{\rm dc}\tau \right). \quad (1)$$

Here, C_i and $C_{\rm d}$ are the numbers of avalanches occurring in the time-bin i and induced by laser pulse, respectively, $r_{\rm dc}$ and

τ are the measured dark count rate and the width of time-bin, C_i/C_d is the ratio between avalanches induced by all the other factors besides the photon, and $r_{dc}\tau$ is the ratio of dark count. Therefore, $C_i/C_d - r_{dc}\tau$ is the afterpulse probability, P_i, in the time-bin i. Figure 4 shows the histogram of the total afterpulse probability P_{total} versus dead time τ_d.

In Fig. 4, we see that the P_{total} reaches 1000% with a dead time of 2 μs, which means there are 10 afterpulses after a triggered avalanche on average at 20% of detection efficiency. Also the P_{total} is below 1% no matter whether the detection efficiency is 15% or 20% with a dead time of 20 μs.

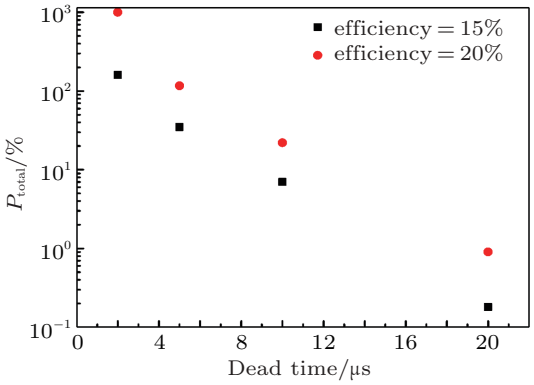


Fig. 4. (color online) Total afterpulse probability versus dead time.

In order to characterize the efficiency, a continuous distributed feedback diode laser source is used without FPGA. The counts corresponding to all detections are registered with the varying bias voltage on the APD. An optical shutter can be used to remove the laser signal in order to measure the dark counts. However, the dark count rate r_{dc} is influenced by τ_d because of afterpulsing. Then we should correct the measured r_{dc} for the total afterpulse probability P_{total} and for the dead time τ_d. The measured output count rate is corrected using the well-known formula:

$$N_{corrected} = N_{measured}/(1 - N_{measured} \times \tau_d). \quad (2)$$

So $r_{dc}/(1 - r_{dc}\tau_d)$ is the measured r_{dc} corrected for dead time, and $r'_{dc}(1 + P_{total})$ is the dark count rate involving the afterpulsing, where r'_{dc} is the inherent dark count rate induced by thermal generation of carriers or tunneling. Therefore, the inherent dark count rate can be derived from the following expression:

$$r'_{dc} = \frac{r_{dc}}{(1 + P_{total})(1 - r_{dc}\tau_d)}. \quad (3)$$

We can determine the quantum efficiency and effective efficiency in the free-running scheme. The quantum efficiency can be determined from the following expression:

$$\eta_{qe} = \frac{1}{n}\left[\frac{S}{(1 - S\tau_d)(1 + P_{total})} - r'_{dc}\right], \quad (4)$$

where the quantum efficiency is corrected for the dead time, τ_d, and for the total afterpulse probability P_{total}; S represents the signal detected when n photons (per second) are sent to the detector, with $S/(1 - S\tau_d)(1 + P_{total})$ denoting the number of clicks originating from the detector without afterpulsing and r'_{dc} being the inherent dark count rate. Thus $S/(1 - S\tau_d)(1 + P_{total}) - r'_{dc}$ is the detected click number due to photons. The effective efficiency can be defined as follows:

$$\eta_{eff} = \frac{S - N}{n}. \quad (5)$$

Here the noise is given by N which includes the inherent dark count rate and the afterpulses. The effective efficiency is saturated at a low applied bias compared with the quantum efficiency. Figure 5 shows that when the quantum efficiency increases to more than 25%, the saturation of effective efficiency is dependent on dead time.

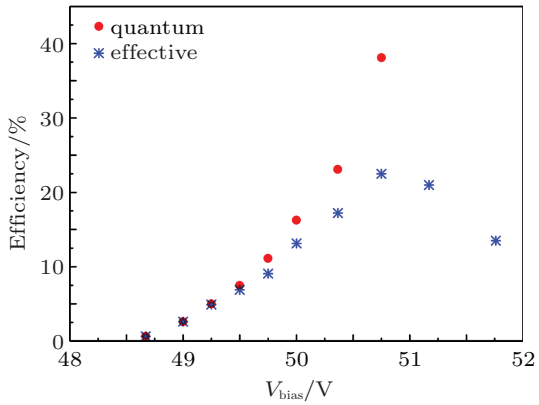


Fig. 5. (color online) Efficiency characteristics versus APD bias voltage.

4. Conclusion

In this paper, we present an active quenching ASIC used for free-running single photon detector based on InGaAs/InP. This quenching method can quench the InGaAs/InP SPADs rapidly so that the influence of the afterpulsing in the free-running mode can be significantly reduced. With the help of the FPGA, the single photon detector can start to work from a well-known initial condition which allows us to analyze the characterizations of the higher orders of afterpulses. The users can choose settings for the software to drive the FPGA, which makes this module fast and simple.

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