Experimental clarification of orientation dependence of germanium PMOSFETs with Al_2O_3/GeO_x/Ge gate stack*

Yun Quan-Xin(云全新), Li Ming(黎 明)†, An Xia(安 霞), Lin Meng(林 猛), Liu Peng-Qiang(刘朋强), Li Zhi-Qiang(李志强), Zhang Bing-Xin(张冰馨), Xia Yu-Xuan(夏宇轩), Zhang Hao(张 浩), Zhang Xing(张 兴), Huang Ru(黄 如), and Wang Yang-Yuan(王阳元)

Key Laboratory of Microelectronic Devices and Circuits (MOE), Institute of Microelectronics, Peking University, Beijing 100871, *China*

(Received 30 March 2014; revised manuscript received 21 April 2014; published online 17 September 2014)

An extensive and complete experimental investigation with a full layout design of the channel direction was carried out for the first time to clarify the orientation dependence of germanium p-channel metal–oxide–semiconductor field-effect transistors (PMOSFETs). By comparison of gate trans-conductance, drive current, and hole mobility, we found that the performance trend with the substrate orientation for Ge PMOSFET is (110)>(111) ∼ (100), and the best channel direction is (110)/[110]. Moreover, the (110) device performance was found to be easily degraded as the channel direction got off from the [110] orientation, while (100) and (111) devices exhibited less channel orientation dependence. This experimental result shows good matching with the simulation reports to give a credible and significant guidance for Ge PMOSFET design.

Keywords: germanium, metal–oxide–semiconductor field-effect transistor, orientation

PACS: 85.30.Tv, 85.30.De, 61.72.uf, 85.40.–e **DOI:** 10.1088/1674-1056/23/11/118506

1. Introduction

The germanium p-channel metal–oxide–semiconductor field-effect transistor (PMOSFET) has been regarded as a potential candidate for the next-generation MOSFET due to its high hole mobility, which is about four times higher than silicon.[1–4] Recently, PMOS devices with good performances have been demonstrated[1–4] based on an effective solution of interface passivation, which is one of the key issues to realize high-performance Ge MOSFETs.[5–9] As is well known, for semiconductor devices, the substrate orientation and the channel orientation are very important to determine the band structure of the material and thus the transport performance of the MOSFET, as well as the structure design of the CMOS.[10] Krishnamohan *et al.*[11] predicted theoretically with numerical simulations that for unstrained Ge PMOSFETs, the best combination of substrate and channel orientations was (110)/[110], and the performance trend with the substrate orientation was (110)>(111)∼(100). However, several existing experimental reports about the orientation effect by different research groups showed some unconformity with the simulation results and even conflicted among themselves,[12–14] mainly focusing on the performance trend with the substrate orientation, especially on the comparison between (100) and (110) substrates. For example, in Refs. [12] and [13], (110) Ge PMOSFET showed the highest hole mobility, while in Ref. [14], the best substrate choice for Ge PMOSFET was (100), though they had the same GeO_x passivation layer achieved by different methods. The unconformity was attributed to the difference of substrate doping,[14] while it should also be related to the difference of their passivation methods and gate stacks.

Thus, in this paper, by using Ge substrates with the same doping level, the same GeO_x interface passivation layer, and the same gate stacks realized by the same process, as well as plenty of substrate/channel orientation combinations, we devise an experimental investigation, trying to clarify the effects of substrate and channel orientations on Ge PMOSFETs. By a statistical comparison of the gate trans-conductance (g_m), drive currents, and hole mobilities of the devices, the performance trend with substrate and channel orientations and the optimum orientation combination for Ge PMOSFETs, are given.

2. Device fabrication

The (100), (110), and (111) oriented n-Ge wafers with doping of 1×10^{15} cm^{-3} were used to fabricate PMOSFETs. The primary flat orientation was [110] for all wafers. The interface passivation layer was GeO_x for all devices, achieved by rapid thermal oxidation (RTO) at 400 °C in O_2. The general process flow is shown in Fig. 1(a). After the active region definition and pre-cleaning, the Ge wafers were loaded into a rapid-thermal-process (RTP) chamber to perform the RTO passivation, followed by 5 nm Al_2O_3 deposition by atomic

*Project supported by the National Basic Research Program of China (Grant No. 2011CBA00601), the National Science and Technology Major Project of the Ministry of Science and Technology of China (Grant No. 2009ZX02035-001), and the National Natural Science Foundation of China (Grant Nos. 60625403, 60806033, and 60925015).

†Corresponding author. E-mail: liming.ime@pku.edu.cn

© 2014 Chinese Physical Society and IOP Publishing Ltd

layer deposition (ALD) at 200 °C. Then, the Al/Pt/TiN metal gate stack was sputtered and patterned. After cleaning, the wafers were annealed at 375 °C in N_2 for 15 min. Then, the ion implantation was carried out to form the source/drain junction, followed by activation annealing at 450 °C in N_2. Finally, Al/Ti contacts were formed for the source/drain and the substrate electrodes, followed by metallization annealing. To avoid the short-channel effects, especially the effects of the source/drain series resistance, the channel length L_g was 10 μm for all devices.

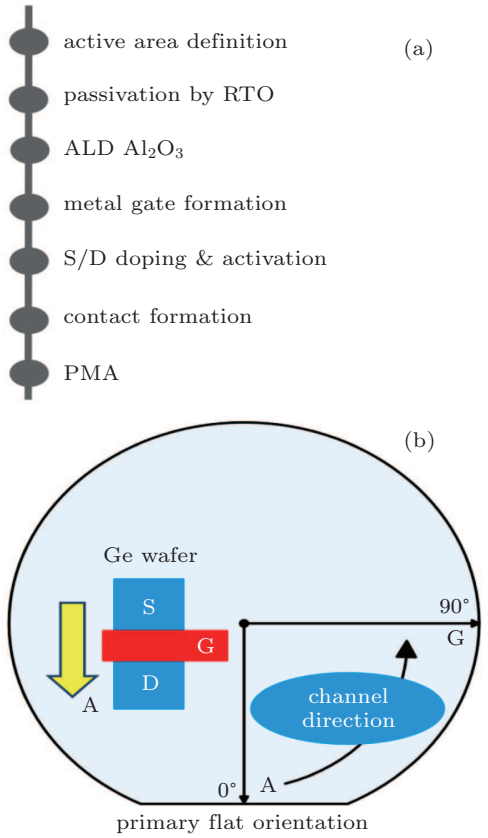


Fig. 1. (color online) (a) The general process flow for fabricating Ge PMOSFETs with an Al_2O_3/GeO_x gate stack, and (b) the schematic of the layout design for orientation investigation. A full design of the channel direction with different off-angles from the primary flat orientation is made.

3. Layout design

To investigate the orientation effects on Ge PMOSFETs, a set of channel orientations were designed in layout, as shown in Fig. 1(b) and Table 1. Seven types of devices labeled A–G, which have different off-angles from the primary flat orientation of the wafer, are listed in Table 1. This design covers all typical channel orientations on all three types of wafers, which is a full channel design for this investigation.

Table 1. Off-angle list in layout.

Device	A	B	C	D	E	F	G
Off angle/(°)	0	30	35.7	45	54.3	60	90

4. Results and discussion

PMOS capacitance–voltage (CV) curves were firstly measured to acquire the effective oxide thickness (EOT) results on different oriented substrates, as shown in Fig. 2. The EOT was extracted from the low frequency capacitance. The extracted results show similar EOTs from 4.8 nm to 5.1 nm, with less than 10% difference for different substrate orientations.

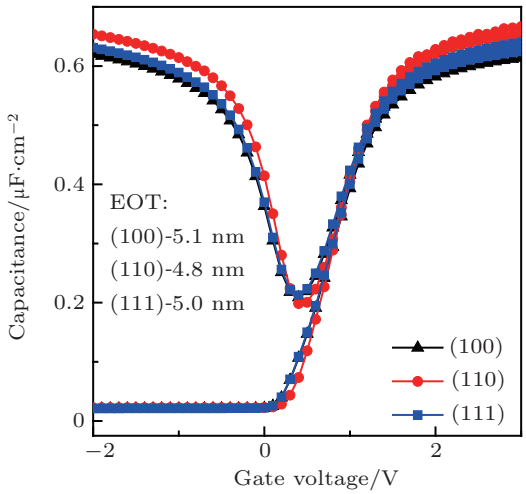


Fig. 2. (color online) PMOS CV curves and EOT results for different substrate orientations.

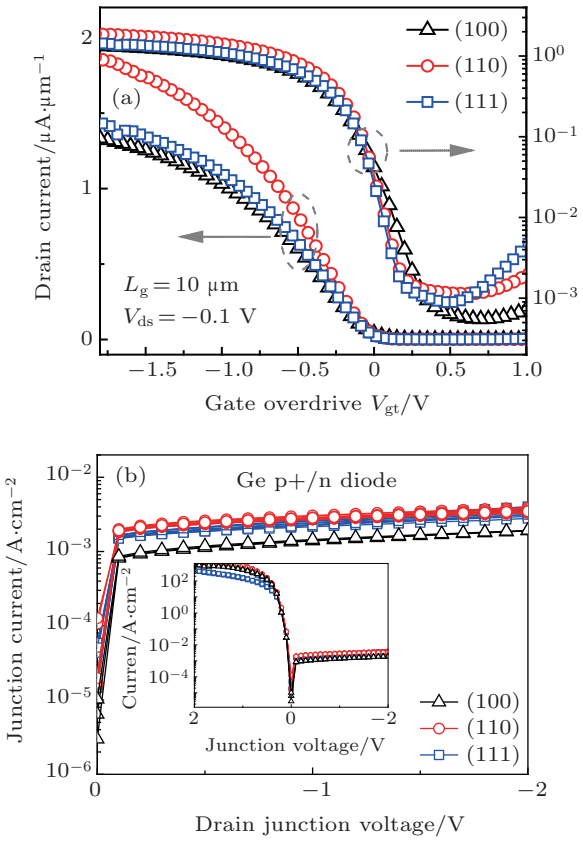


Fig. 3. (color online) (a) Transfer characteristics of devices along the [110] direction, and (b) the drain junction leakage as a function of the substrate orientation. The junction leakage currents are at a similar level, while the (110) device exhibits much better drive performance than (100) and (111) devices.

Figure 3 shows the transfer characteristics and the drain junction leakage currents on different oriented wafers. The (110) device exhibits a distinct enhancement compared to (100) and (111) devices in the drain current, as shown in Fig. 3(a). Little difference is observed in the junction leakage among different wafers, as shown in Fig. 3(b). The junction leakage is believed to be dominated by the BTBT current,[11,15] which is mainly affected by the band gap. Thus, this little orientation dependence in the junction leakage should be attributed to the band-gap differences between different sub valleys in Ge.[11,15]

To evaluate the performance trend with the orientation, the linear g_m, hole mobilities, and saturation drive currents of all samples were characterized and statistically compared, as shown in Figs. 4–6.

The peak g_m has a distinct dependence on the substrate orientation, as shown in Fig. 4, and the (110) substrate shows the highest g_m regardless of the channel angles. An obvious channel orientation dependence is also observed on the (110) substrate. We find that the g_m of Ge PMOSFET decreases greatly as the off-angle increases from 0° ([110]) to 90° ([100]) on the (110) substrate. The (110)/[110] aligned device shows at least 28% higher g_m than the (110)/[100] aligned device. However, different from the case on the (110) substrate, nearly no channel orientation dependence is observed on (100) and (111) substrates. Despite that the (111) substrate shows a little higher g_m than the (100) substrate, the results on both (111) and (100) substrates are very close. The best g_m result on the (110) substrate is at least 40% and 30% higher than that on (100) and (111) substrates, respectively, regardless of the channel orientation. Thus, the g_m trend with the substrate orientation is (110)>(111)∼(100), and the best g_m result is from the device aligned in the (110)/[110] orientation.

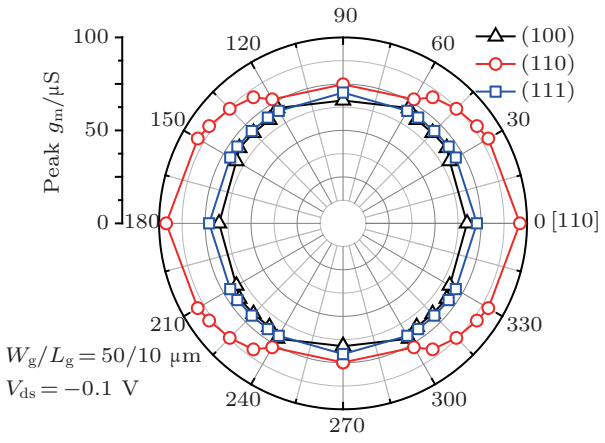


Fig. 4. (color online) The average peak g_m as a function of substrate and channel orientations, extracted from ten devices for each data point at $V_{ds} = -0.1$ V.

Besides, an obvious difference appears in the saturation drive current among different substrates, as shown in Fig. 5. Much similar to the g_m case, the drive current trend with the substrate orientation is also (110)>(111)∼(100), and the best channel orientation is (110)/[110]. The PMOSFET aligned in the (110)/[110] direction shows at least 50% and 40% enhancements in the drive current compared to that on (100) and (111) substrates, respectively, regardless of the channel orientation.

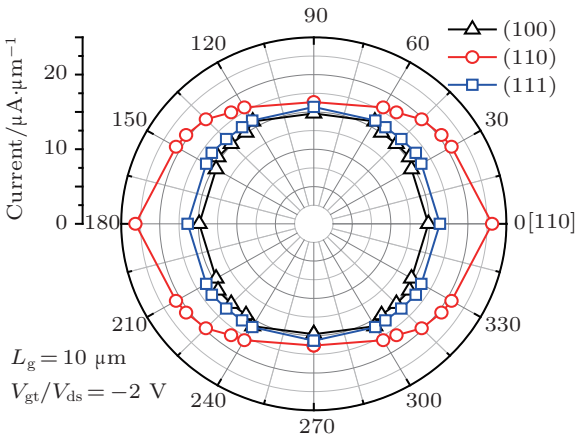


Fig. 5. (color online) The average drive current as a function of substrate and channel orientations, extracted from ten devices for each data point at $V_{gt} = V_{ds} = -2$ V.

The linear g_m and the saturation drive current can be described by the following formulas:

$$g_m = \frac{WC_{ox}V_{ds}}{L}\mu, \tag{1}$$

$$I_{Dsat} = \frac{WC_{ox}V_{gt}^2}{2L}\mu. \tag{2}$$

Since the EOTs on different substrates are very close to each other, as shown in Fig. 2, the difference of g_m and drive current among different substrates and channels should mainly originate from the hole mobility difference. The peak hole mobility is then extracted, as shown in Fig. 6, showing the consistent trend with g_m and the drive current.

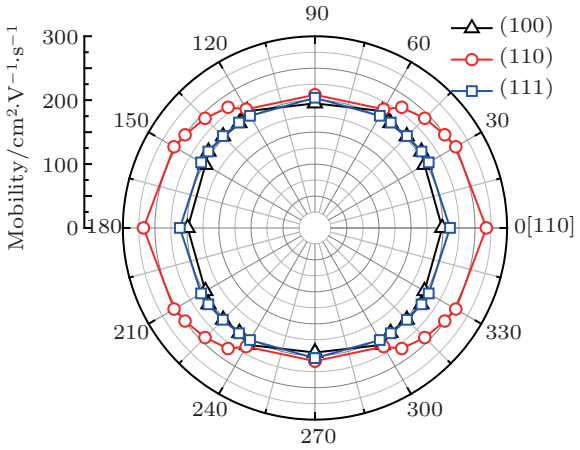


Fig. 6. (color online) The peak hole mobility as a function of substrate and channel orientations, extracted from g_m.

Overall, from the linear g_m, saturation drive current, and hole mobility results, the performance trend with the substrate

orientation for Ge PMOSFET is (110)>(111)∼(100), and the best channel choice is (110)/[110]. This performance trend is indeed consistent with the mobility trend obtained by the simulation under an unstrained condition,[11] which is calculated based on the valence band structure of Ge. Thus, the consistency of this experimental result with the simulation result makes it more credible for guiding the Ge PMOSFET design. Besides, we believe that, other reasons such as the interface quality, the density of states of the valence band, and the electrical field dependence of the hole mobility, may also contribute to the performance difference between different substrates, which need a further symmetric investigation to clarify the physical mechanism.

5. Conclusion

The orientation dependence of Ge PMOSFETs was experimentally clarified by an investigation using the same GeO_x interface passivation layer, the same gate stack, substrates with the same doping, and a full set of channel orientation layout designs. The statistical results of g_m, drive current, and hole mobility demonstrated that the performance trend with the substrate orientation for Ge PMOSFETs is (110)>(111)∼(100), and the best channel choice is (110)/[110]. Moreover, the (110) device exhibited a sensitive channel orientation dependence, while (100) and (111) devices had nearly no dependence on the channel orientation under the unstrained condition.

Acknowledgment

The authors would like to thank the Nanofabrication Facility of the Suzhou Institute of Nano-tech and Nano-bionics (SINANO) for the process support.

References

[1] Zhang L L, Gunji M, Thombare S and McIntyre P C 2013 *IEEE Electron Device Lett.* **34** 732
[2] Wu N, Zhang Q, Zhu C, Chan D S H, Du A, Balasubramanian N, Li M F, Chin A, Sin J K O and Kwong D L 2004 *IEEE Electron Device Lett.* **25** 631
[3] Kuzum D, Pethe A J, Krishnamohan T and Saraswat K C 2009 *IEEE Trans. Electron Devices* **56** 648
[4] Zhang R, Taoka N, Huang P C, Takenaka M and Takagi S 2011 *Technical Digest of the International Electron Devices Meeting*, December 5–7, 2011 Washington, USA, p. 642
[5] Lee C H, Nishimura T, Saido N, Nagashio K, Kita K and Toriumi A 2009 *Technical Digest of the International Electron Devices Meeting*, December 7–9, 2009 Baltimore, USA, p. 457
[6] Chen W B and Chin A 2010 *IEEE Electron Device Lett.* **31** 80
[7] Lin M, Li M, An X, Yun Q X, Li M, Li Z Q, Liu P Q, Zhang X and Huang R 2013 *Semicond. Sci. Technol.* **28** 085010
[8] Sun J B, Yang Z W, Geng Y, Lu H L, Wu W R, Ye X D, Zhang W, Shi Y and Zhao Y 2013 *Chin. Phys. B* **22** 067701
[9] Xue B Q, Wang S K, Han L, Chang H D, Sun B, Zhao W and Liu H G 2013 *Chin. Phys. B* **22** 107302
[10] Takagi S, Irisawa T, Tezuka T, Numata T, Nakaharai S, Hirashita N, Moriyama Y, Usuda K, Toyoda E, Dissanayake S, Shichijo M, Nakane R, Sugahara S, Takenaka M and Sugiyama N 2008 *IEEE Trans. Electron Devices* **55** 21
[11] Krishnamohan T, Kim D, Dinh T V, Pham A T, Meinerzhagen B, Jungemann C and Saraswat K C 2008 *Technical Digest of the International Electron Devices Meeting*, December 15–17, 2008 San Francisco, USA, p. 899
[12] Zhang R, Huang P, Lin J, Takenaka M and Takagi S 2012 *Technical Digest of the International Electron Devices Meeting*, December 10–13, 2012 San Francisco, USA, p. 371
[13] Zhang R, Iwasaki T, Taoka N, Takenaka M and Takagi S 2011 *Symposium on VLSI Technology,* June 14–16, 2011 Kyoto, Japan, p. 56
[14] Lee C H, Nishimura T, Tabata T, Wang S K, Nagashio K, Kita K and Toriumi A 2010 *Technical Digest of the International Electron Devices Meeting*, December 6–8, 2010 San Francisco, USA, p. 416
[15] Kim D, Krishnamohan T, Nishi Y and Saraswat K C 2006 *International Conference on Simulation of Semiconductor Processes and Devices*, September 6–8, 2006 Monterey, USA, p. 389