A two-dimensional analytical model for channel potential and threshold voltage of short channel dual material gate lightly doped drain MOSFET

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An analytical model for the channel potential and the threshold voltage of the short channel dual-material-gate lightly doped drain (DMG-LDD) metal–oxide–semiconductor field-effect transistor (MOSFET) is presented using the parabolic approximation method. The proposed model takes into account the effects of the LDD region length, the LDD region doping, the lengths of the gate materials and their respective work functions, along with all the major geometrical parameters of the MOSFET. The impact of the LDD region length, the LDD region doping, and the channel length on the channel potential is studied in detail. Furthermore, the threshold voltage of the device is calculated using the minimum middle channel potential, and the result obtained is compared with the DMG MOSFET threshold voltage to show the improvement in the threshold voltage roll-off. It is shown that the DMG-LDD MOSFET structure alleviates the problem of short channel effects (SCEs) and the drain induced barrier lowering (DIBL) more efficiently. The proposed model is verified by comparing the theoretical results with the simulated data obtained by using the commercially available ATLAS^{TM} 2D device simulator.

Keywords: dual-material-gate MOSFET, lightly doped drain, short channel effect, threshold voltage

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1. Introduction

The complementary metal oxide semiconductor (CMOS) technology has proven to be the most important driving force behind the evolution of almost all kinds of technologies in the last five decades.[1,2] With the integration limit reaching towards the gigascale range,[3,4] the conventional CMOS scaling has now approached the fundamental limits of operations, which include the leakage in channel and gate, diminished bulk effect, transport in silicon, and increased power dissipation.[5,6] If further scaling of CMOS has to take place, then there should be some means by which these limits of downscaled CMOS operations can be overcome. Furthermore, the technological trends and the possible technological options for future CMOS devices require possible solutions in the form of new device structures, new materials, and new technologies for conquering the physical and technology constraints of the downscaled device.[5] In lieu of this, various types of engineered structures for metal–oxide–semiconductor field-effect transistors (MOSFETs) have been developed by the researchers to improve the performance of the conventional structure.[7–18]

The main types of engineering that can be done to enhance the performance of MOSFET are gate engineering and channel engineering.[7] It has been shown in the literature that using a dual-material-gate structure minimizes the hot electron effect and lends to more control of the gate, which effectively reduces the short channel effects (SCEs).[8–12] In the dual-material-gate MOSFET structure, two different metal gates with different work functions are combined together causing a step in the surface potential profile that screens the effect of the drain on the channel. Further, the peak electric field at the drain end is reduced, which ensures that the average electric field under the gate is increased. This leads to an increased lifetime of the device, minimization of the ability of the localized charge to raise the drain resistance, and more control of the gate over the conductance of the channel so as to increase the gate transport efficiency. Long *et al.*[8] firstly proposed the dual-material-gate FET structure in 1997, and demonstrated that the use of dual materials as the gate solves the problem of the SCEs and leads to better carrier transportation efficiency. Kumar *et al.*[9] presented a two-dimensional (2D) analytical model for the surface potential and the threshold voltage of a short channel dual-material-gate (DMG) MOSFET and showed that the SCEs are suppressed to a good extent because of the step in the surface potential profile. The radio-frequency (RF) application of the DMG MOSFETs was reported by Dao-Ming *et al.*[10] in 2006. Later, Reddy *et al.*[11] proposed a dual-material DG MOSFET and showed that the SCEs are improved by using the new device structure, even for the channel lengths far below 50 nm. Recently, Tiwari *et al.*[12] proposed a channel potential and threshold voltage model for the triple material gate DG MOSFET and demonstrated improved hot carrier effects compared to the DMG DG MOSFET. Another important category of unconventional

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MOSFET structure is the one having some kind of channel engineering. For channel lengths below 100 nm, MOSFETs exhibit considerable leakage currents; to overcome this effect, different channel engineering techniques have been used. In the past few years, the local high doping in the channel region near the source/drain junctions, known as halo or pocket implants,[13–18] has become the most prominent lateral channel engineering technique. In a number of literatures,[13–18] single halo MOSFET structures have been introduced for bulk as well as for silicon-on-insulator (SOI) MOSFETs to adjust the threshold voltage and to improve the device SCEs. Recently, Fei *at al.*[19] presented a threshold voltage model for high-k gate dielectric MOSFETs with fully overlapped lightly doped drain (LDD) structures. They showed that the MOSFET having the LDD structure shows better immunity to the SCEs. However, to the best of my knowledge, no work has been reported so far for the 2D analytical model of the channel potential and the threshold voltage of the MOSFET having dual material gates and double halo implants.

In the present paper, the channel potential and the threshold voltage in the dual-material-gate lightly doped drain MOSFET (DMG-LDD MOSFET) are modeled. The analytical model is obtained by solving 2D Poisson's equation in the channel region. The parabolic approximation technique is utilized to solve the Poisson's equation in the channel region in conjunction with suitable boundary conditions. The boundary conditions are properly modified in order to incorporate the effects of the dual material gates and the lightly doped drain regions. The effects of various device parameters on the channel potential are discussed. The threshold voltage of the DMG-LDD MOSFET is modeled using the minimum middle channel potential of the MOSFET. Further, the threshold voltage of the DMG-LDD MOSFET is compared with that of the DMG MOSFET structure to establish the fact that the DMG-LDD MOSFET structure shows better immunity to the SCEs. Furthermore, the DMG-LDD structure is simulated using suitable models available in the library of the ATLAS$^{\text{TM}}$ device simulator.[20] The analytical results obtained from the model are compared to the numerical simulation data obtained by the ATLAS$^{\text{TM}}$ software to establish the validity of the proposed model.

2. Device details

A schematic structure of the DMG-LDD MOSFET used for our analysis and simulation is shown in Fig. 1, where L ($L = L_1 + L_2$), L_{n}, X_{j}, and t_{ox} are the gate length, the length of the LDD region, the junction depth of the LDD region, and the thickness of the gate oxide, respectively. The x and y axes of the schematic structure are considered to be along the channel length and the channel thickness, respectively. The gate electrode of the DMG-LDD structure is made up of two different gate materials with work functions ϕ_{M1} and ϕ_{M2} deposited over lengths L_1 and L_2, respectively. The gate material placed at the source end has a higher work function than the gate material placed at the drain end (i.e., $\phi_{\text{M1}} > \phi_{\text{M2}}$). The gate material having the larger work function is called the control gate, whereas that having the smaller work function is called the screen gate.[12] In the present work, tungsten disilicide (WSi_2) is taken as the material for the control gate and $Hf_{0.27}Ta_{0.58}N_{0.15}$ is used in the screen gate. The gate terminal of the DMG-LDD device is made by tying together control and screen gates to feed the device with the same gate to source voltage (V_{GS}). The p-type substrate is uniformly doped with a doping concentration of $N_{\text{a}} = 1 \times 10^{18}$ cm^{-3} and has pocket implantations at both source and drain sides with a peak pocket doping concentration of $N_{\text{p}} = 1 \times 10^{19}$ cm^{-3}. The source and the drain regions are assumed to be heavily doped with a doping concentration of $N_{\text{S/D}} = 1 \times 10^{21}$ cm^{-3}. The average doping concentration in the LDD region can be approximated as $N_{\text{av}} = n_{\text{t}}/X_{\text{j}}$, where n_{t} is the total doping concentration of the LDD region and is obtained by the following equation:[21]

$$n_{\text{t}} = \int_0^{\infty} N_{\text{p}} \exp\left[-\frac{1}{2}\left(\frac{x - x_{\text{p}}}{D_x}\right)^2\right] \mathrm{d}x, \tag{1}$$

where N_{p} is the peak concentration, x_{p} is the peak position, generally zero depicting that the peak concentration is in the surface of the substrate, and D_x is[19]

$$D_x = \sqrt{\frac{x_{\text{j}} - x_{\text{p}}}{-2\ln\left(N_{\text{j}}/N_{\text{p}}\right)}}. \tag{2}$$

In Eq. (2), x_{j} is the position of the p–n junction and equals the junction depth, and N_{j} is the doping concentration at the junction.

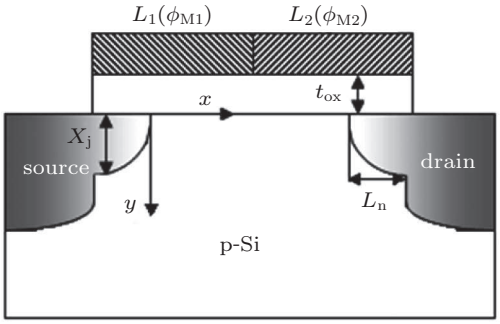


Fig. 1. Schematic diagram of DMG-LDD MOSFET, where L ($L = L_1 + L_2$), L_{n}, X_{j}, and t_{ox} are the gate length, the length of the LDD region, the junction depth of the LDD region, and the thickness of the gate oxide, respectively.

3. Analytical modeling

The channel region of the short channel DMG-LDD MOSFET device is divided into two regions for the purpose of analytical modeling. Let $\varphi_n(x,y)$ with $n = 1$ and 2 be the channel potentials in channel region I under gate length L_1

and chanel region II under gate length L_2, respectively. The 2D channel potential $\varphi_n(x,y)$ can be obtained in the channel region by solving the 2D Poisson's equation

$$\frac{\partial^2\varphi_n(x,y)}{\partial x^2}+\frac{\partial^2\varphi_n(x,y)}{\partial y^2}=\frac{qN_a}{\varepsilon_{si}},\quad n=1,2, \tag{3}$$

where ε_{si} is the permittivity of silicon, and q is the charge of an electron.

The boundary conditions used to solve the Poisson's equation can be given as follows.[11]

Boundary condition 1 The potential function should be continuous in the entire channel region, so the following boundary condition should be fulfilled at the interface of the two regions:

$$\varphi_1(L_1,0)=\varphi_2(L_1,0). \tag{4}$$

Boundary condition 2

$$\left.\frac{\mathrm{d}\varphi_n(x,y)}{\mathrm{d}y}\right|_{y=0}=\frac{\varepsilon_{ox}}{\varepsilon_{si}}\left(\frac{\varphi_{Sn}(x)-V_{GS}+V_{fbn}}{t_{ox}}\right), \tag{5}$$

where ε_{ox} is the permittivity of the silicon dioxide, $\varphi_{Sn}(x)$ is the surface potential related to the n-th region, and V_{fbn} is the flat band voltage related to the n-th region

$$V_{fbn}=\varphi_{mn}-\left[\chi_{si}+\frac{E_g}{2q}+\frac{kT}{q}V_T\ln\left(\frac{N_a}{n_i}\right)\right],$$

where φ_{mn} is the gate material work function of the n-th region, χ_{si} is the electron affinity of silicon, E_g is the bandgap of silicon, n_i is the intrinsic carrier concentration of silicon, k is the Boltzmann constant, and T is the temperature.

Boundary condition 3 The electric fluxes should also be continuous at the interface of the two regions. Thus, we have

$$\left.\frac{\mathrm{d}\varphi_1(x,y)}{\mathrm{d}x}\right|_{x=L_1}=\left.\frac{\mathrm{d}\varphi_2(x,y)}{\mathrm{d}x}\right|_{x=L_1}, \tag{6}$$

$$\left.\frac{\mathrm{d}\varphi_1(x,y)}{\mathrm{d}y}\right|_{y=t_{si}}=\left.\frac{\mathrm{d}\varphi_2(x,y)}{\mathrm{d}y}\right|_{y=t_{si}}=0. \tag{7}$$

Boundary condition 4 The potentials at the source–channel and the drain–channel interfaces can be written as[11]

$$\varphi_1(0,0)=\varphi_{S1}(0)=V_{bi}, \tag{8}$$

$$\varphi_2(L_1+L_2,0)=\varphi_{S2}(L_1+L_2)=V_{bi}+V_{DS,eff}, \tag{9}$$

where V_{bi} is the built-in potential of the DMG-LDD MOSFET and represents the potential of the n^- substrate junction instead of the n^+ substrate junction for the normal MOSFET

$$V_{bi}=\frac{kT}{q}n\left(\frac{N_a\overline{N_{av}}}{n_i^2}\right). \tag{10}$$

The $V_{DS.eff}$ is the effective drain to source voltage in the DMG-LDD MOSFET since the voltage drop in the LDD region may not be neglected at a higher drain to source voltage V_{DS}. It can be given as[21]

$$V_{DS,eff}=\frac{V_{DS}(L_1+L_2)}{(L_1+L_2)+\alpha L_n},$$

where α is a fitting parameter whose value ranges between 0 and 1.

The solution of Eq. (3) for $n=1$ and 2 can be written as[22]

$$\varphi_n(x,y)=a_{n0}(x)+a_{n1}(x)y+a_{n2}(x)y^2,\quad n=1,2, \tag{11}$$

where a_{n0}, a_{n1}, and a_{n2} are arbitrary functions of x which can be obtained by using suitable boundary conditions given in Eqs. (4)–(9). Now, substituting $y=0$ in Eq. (11), we obtain

$$a_{n0}(x)=\varphi_{Sn}(x), \tag{12}$$

where $\varphi_{Sn}(x)$ is the surface potential at the Si–SiO_2 interface. By putting Eq. (12) into Eq. (11), equation (11) becomes

$$\varphi_n(x,y)=\varphi_{Sn}(x)+a_{n1}(x)y+a_{n2}(x)y^2. \tag{13}$$

Then using boundary conditions of Eqs. (5) and Eq. (7), we obtain

$$a_{n1}(x)=\frac{\varepsilon_{ox}}{\varepsilon_{si}}\left(\frac{\varphi_{Sn}(x)-V_{GS}+V_{fbn}}{t_{ox}}\right), \tag{14}$$

$$a_{n2}(x)=-\frac{\varepsilon_{ox}}{t_{si}\varepsilon_{si}}\left(\frac{\varphi_{Sk}(x)-V_{GS}+V_{fbn}}{t_{ox}}\right). \tag{15}$$

Further substituting a_{n1} and a_{n2} in Eq. (13) and putting $y=t_{Si}/2$, we have

$$\begin{aligned}\varphi_{Sn}=&\left[4\varepsilon_{si}t_{ox}\varphi_{cn}(x)+\varepsilon_{ox}t_{si}(V_{GS}-V_{fbn})\right]\\&\times(4\varepsilon_{si}t_{ox}+\varepsilon_{ox}t_{si})^{-1}.\end{aligned} \tag{16}$$

Now, since the characteristic length λ associated with the channel potential of silicon is stringent in determining the SCEs of the DMG-LDD MOSFET, it is essential to obtain λ. Solving the Poisson's equation at the middle of the channel gives a convincingly good value for characteristic length λ, so equation (3) is solved at the middle of the silicon channel as

$$\frac{\mathrm{d}^2\varphi_{cn}(x)}{\mathrm{d}x^2}=\frac{1}{\lambda^2}\left[\varphi_{cn}(x)+\frac{\lambda^2qN_a-\varepsilon_{si}(V_{GS}-V_{fbn})}{\varepsilon_{si}}\right], \tag{17}$$

where $\varphi_{cn}(x)$ is the middle channel potential in the n-th region and

$$\lambda=\sqrt{\frac{t_{si}^2(4\varepsilon_{si}t_{ox}+\varepsilon_{ox}t_{si})}{2\varepsilon_{ox}t_{si}}}.$$

Now, a generalized solution for Eq. (17) can be written as

$$\varphi_{cn}(x)=A_n\exp(\eta x)+B_n\exp(-\eta x)-\frac{\beta_n}{\alpha}, \tag{18}$$

where $\eta=1/\lambda=\sqrt{\alpha}$ and

$$\beta_n=\frac{\lambda^2qN_a-\varepsilon_{si}(V_{GS}-V_{fbk})}{\lambda^2\varepsilon_{si}}.$$

The constants A_n and B_n correspond to A_1, A_2 and B_1, B_2 for channel regions I and II, respectively. These coefficients can be obtained by solving Eq. (18) in conjunction with the boundary conditions given in Eqs. (4)–(9)

$$A_1 = V_{\rm bi} + \frac{\beta_1}{\alpha} - B_1, \tag{19}$$

$$\begin{aligned} B_1 = {} & \frac{1}{\exp(-\eta(L_1+L_2)) - \exp(\eta(L_1+L_2))} \\ & \times \Bigg[V_{\rm bi}(1-\exp(\eta(L_1+L_2))) \\ & + V_{\rm DS,eff} + \frac{\beta_1}{2\alpha}\left[\frac{\exp(\eta(L_1+L_2))}{\exp(\eta L_1)} + \frac{\exp(-\eta(L_1+L_2))}{\exp(-\eta L_1)} \right. \\ & \left. - 2\exp(\eta(L_1+L_2))\right] - \frac{\beta_2}{2\alpha}\left[\frac{\exp(\eta(L_1+L_2))}{\exp(\eta L_1)} \right. \\ & \left. + \frac{\exp(-\eta(L_1+L_2))}{\exp(-\eta L_1)} - 2\right]\Bigg], \end{aligned} \tag{20}$$

$$\begin{aligned} A_2 = {} & \left[V_{\rm bi} + V_{\rm DS,eff} + \frac{\beta_2}{\alpha} - B_2\exp(-\eta(L_1+L_2)\right] \\ & \times \frac{1}{\exp(\eta(L_1+L_2))}, \end{aligned} \tag{21}$$

$$\begin{aligned} B_2 = {} & \frac{1}{\exp(-\eta(L_1+L_2)) - \exp(\eta(L_1+L_2))} \\ & \times \Bigg[V_{\rm bi}(1-\exp(\eta(L_1+L_2))) \\ & + V_{\rm DS,eff} - \frac{\beta_1\exp(\eta(L_1+L_2))}{\alpha} \\ & \times \left[1 - \frac{1}{2\exp(\eta L_1)} - \frac{1}{2\exp(-\eta L_1)}\right] \\ & - \frac{\beta_2\exp(\eta(L_1+L_2))}{2\alpha}\left[\frac{1}{\exp(\eta L_1)} + \frac{1}{\exp(-\eta L_1)} \right. \\ & \left. - \frac{2}{\exp(\eta(L_1+L_2))}\right]\Bigg]. \end{aligned} \tag{22}$$

Now, by using Eqs. (13), (16), (18), and (19)–(22), the 2D channel potentials in regions I and II can be given as

$$\begin{aligned} \varphi_n(x,y) = {} & 4(4\varepsilon_{\rm si}t_{\rm ox} + \varepsilon_{\rm ox}t_{\rm si})^{-1}\Bigg[A_n\exp(\eta x) + B_n\exp(-\eta x) \\ & - \frac{\beta_n}{\alpha} + \frac{\varepsilon_{\rm ox}t_{\rm si}}{4\varepsilon_{\rm si}t_{\rm ox}}(V_{\rm GS} - V_{{\rm fb}n})\Bigg] \\ & \times \left(\frac{\varepsilon_{\rm si}t_{\rm si}t_{\rm ox} + \varepsilon_{\rm ox}t_{\rm si}y - \varepsilon_{\rm ox}y^2}{t_{\rm si}}\right) \\ & - \frac{\varepsilon_{\rm ox}t_{\rm si}(V_{\rm GS} - V_{{\rm fb}n})}{\varepsilon_{\rm si}t_{\rm si}t_{\rm ox}}\left[y - y^2t_{\rm si}^{-1}\right]. \end{aligned} \tag{23}$$

Under the threshold condition, the channel under the control gate will not conduct until the channel under the screen gate is turned on; it implies that to establish the conducting channel between the source and the drain, all the gates should be turned on. In other words, it can be stated that the threshold voltage of the device can be monitored by the control gate. Now, if $\varphi_{\rm c1,min} = \varphi_{\rm c1}(x)\big|_{x=x_{0,\rm min}}$ represents the minimum middle channel potential, then the distance $x = x_{0,\rm min}$ can be obtained by putting

$$\frac{{\rm d}\varphi_{\rm c1}(x_{0,\rm min})}{{\rm d}x} = 0. \tag{24}$$

From the above condition, $x_{0,\rm min}$ can be obtained as

$$x_{0,\rm min} = \frac{1}{2\eta}\ln\frac{B_1}{A_1}. \tag{25}$$

By using Eqs. (18) and (25), $\phi_{\rm c1,min}$ can be obtained as

$$\varphi_{\rm c1,min} = 2(A_1B_1)^{1/2} - qN_{\rm a}\lambda^2\varepsilon_{\rm si}^{-1} + V_{\rm GS} - V_{\rm fb1}. \tag{26}$$

The threshold voltage of the DMG-LDD MOSFET is the gate voltage at which $\varphi_{\rm c1,min} = 2\varphi_{\rm f}$, where $\varphi_{\rm f} = (kT/q)\ln(N_{\rm a}/n_{\rm i})$. Upon solving with the aforementioned condition, we obtain the expression for the threshold voltage

$$V_{\rm T} = \frac{2kT}{q}\ln\frac{N_{\rm a}}{n_{\rm i}} + qN_{\rm a}\lambda^2\varepsilon_{\rm si}^{-1} - 2(A_1B_1)^{1/2} + V_{\rm fb1}. \tag{27}$$

4. Results and discussion

In this section, some theoretical results obtained by the proposed model are validated by comparing them with the numerical simulation results obtained by using the ATLAS$^{\rm TM}$ device simulator. The drift–diffusion model is used in place of the energy balance model because it can predict the I–V characteristics of the short-channel MOS devices more realistically than the EB model.[23] The Caughey–Thomas high-field mobility model is implemented in the ATLAS$^{\rm TM}$ with a suitable modification in the saturation velocity of the electron.[20,24] The modified saturation velocity is well matched for device lengths $L \geq 10$ nm.[24]

The work function of the control gate material is $\phi_{\rm M1} = 4.8$ eV and that of the screen gate material is $\phi_{\rm M2} = 4.6$ eV. Further, the ratio of lengths of region I and II is taken as $L_1 : L_2 :: 1 : 1$ for all the computations. The proposed model is applicable for non-LDD DMG MOSFET structures after a few modifications, hence to obtain the results for the non-LDD structures, the doping concentration of the LDD region is replaced by the doping concentration of the n^+ region and the pocket length is kept at zero. Further, the built-in potential in the model is calculated for the n^+-substrate junction and $V_{\rm DS,eff}$ is replaced by $V_{\rm DS}$.

The channel potential variation of the DMG-LDD MOSFET as a function of channel length L is shown in Fig. 2 for different gate–source voltages $V_{\rm GS}$. It can be observed from the figure that the potential profile consists of two steps and the minimum channel potential lies under the control gate. Moreover, as $V_{\rm GS}$ increases, the peak of the potential minimum shifts in the upward direction without any change in its boundary values owing to the fact that the charge under the gate electrode increases with increasing gate bias. Figure 3

demonstrates the variation in the channel potential along the channel length for different drain to source voltages V_{DS}. It can be clearly seen from the figure that due to the step profile, there is no significant increase in the potential under the control gate and it is essentially screened from V_{DS}. It is noteworthy from Fig. 3 that the drain induced barrier lowering (DIBL) effect is considerably reduced for the given structure since the drain voltage shows very little influence on the drain current after saturation, thereby reducing the drain conductance. Figure 4 shows the variation of the channel potential along the channel length for different peak pocket doping concentrations N_p. It can be observed from the figure that the potential increases as N_p increases. It is due to the fact that there is an effective increase in the carrier concentration along the channel when N_p increases. The variation of the channel potential along the channel length is shown in Fig. 5 for different pocket lengths L_n. It can be seen from the figure that the channel potential increases with decreasing L_n. It is due to the fact that when L_n decreases, the effective doping concentration also decreases. The influence of the DIBL on the sub-threshold behavior of the device can be monitored by the minimum surface potential; therefore, to demonstrate the effect, the minimum surface potential is plotted in Fig. 6 as a function of the channel length and V_{DS} for the DMG-LDD MOSFET and the DMG MOSFET. It is seen from the figure that due to the presence of the dual material gates, there is no significant change in the potential under gate M_1, even when the drain bias is increased (also evident from Fig. 3). Note that the DIBL effect has been observed to be even less for the DMG-LDD MOSFET in comparison to that for the DMG MOSFET. Figure 7 shows the threshold voltage against the variation in the channel length for the DMG-LDD MOSFET and the DMG MOSFET. It can be observed from the figure that the threshold voltage roll-off is considerably improved for the DMG-LDD MOSFET compared to the DMG MOSFET, implying that the DMG-LDD MOSFET shows better SCEs.

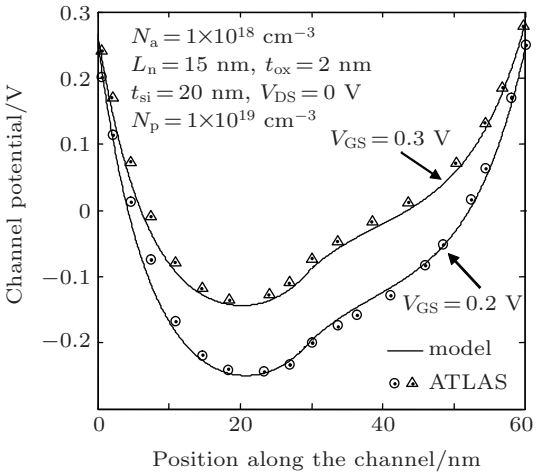


Fig. 2. Variation of the channel potential along the channel length for different gate to source voltages V_{GS}.

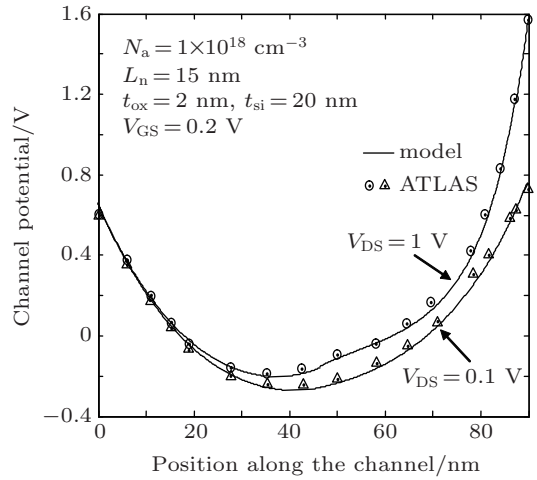


Fig. 3. Variation of the channel potential along the channel length for different gate to source voltages V_{DS}.

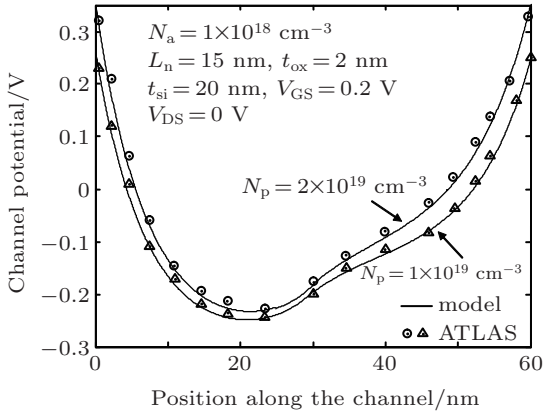


Fig. 4. Variation of the channel potential along the channel length for different LDD region doping N_p.

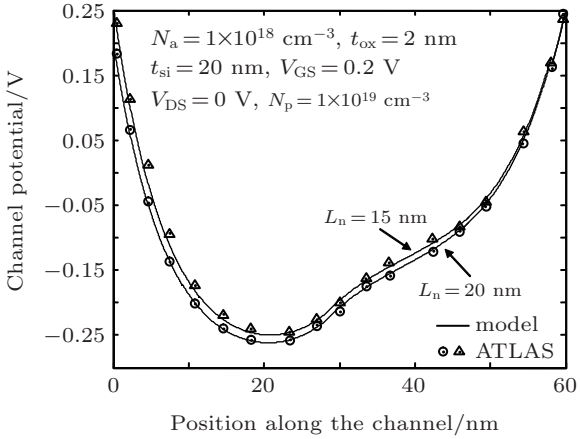


Fig. 5. Variation of the channel potential along the channel length for different LDD region lengths L_n.

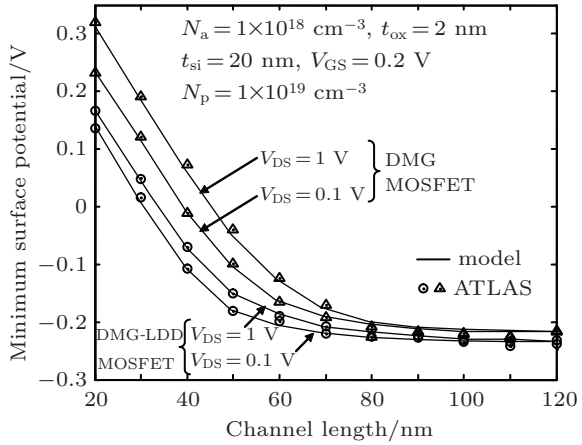


Fig. 6. Variation of the minimum surface potential as a function of the channel length and V_{DS} for DMG-LDD MOSFET and DMG MOSFET.

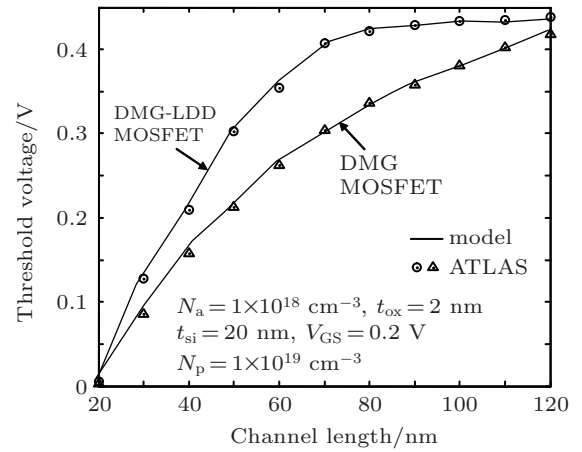


Fig. 7. Variation of threshold voltage V_T for different gate lengths for DMG-LDD MOSFET and DMG MOSFET.

5. Conclusion

In this paper, the 2D channel potential has been modeled for the DMG-LDD MOSFET following the parabolic approximation method. The effects of the bias voltages and the pocket profile parameters on the channel potential have also been studied extensively. Furthermore, the threshold voltage of the DMG-LDD MOSFET has also been derived using the minimum middle channel potential, and was compared to the threshold voltage of the DMG MOSFET. The better immunity to the SCEs has been observed in the DMG-LDD MOSFET as compared to the DMG MOSFET. The good overall match of the new model with the simulation results obtained using the ATLAS^{TM} 2D device simulator illustrate the applicability of the analytical model.

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