Impact of nitrogen plasma passivation on the interface of germanium MOS capacitor*

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Nitrogen plasma passivation (NPP) on (111) germanium (Ge) was studied in terms of the interface trap density, roughness, and interfacial layer thickness using plasma-enhanced chemical vapor deposition (PECVD). The results show that NPP not only reduces the interface states, but also improves the surface roughness of Ge, which is beneficial for suppressing the channel scattering at both low and high field regions of Ge MOSFETs. However, the interfacial layer thickness is also increased by the NPP treatment, which will impact the equivalent oxide thickness (EOT) scaling and thus degrade the device performance gain from the improvement of the surface morphology and the interface passivation. To obtain better device performance of Ge MOSFETs, suppressing the interfacial layer regrowth as well as a trade-off with reducing the interface states and roughness should be considered carefully when using the NPP process.

Keywords: germanium, roughness, interface trap density, interfacial layer thickness

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1. Introduction

Germanium (Ge) has been regarded as a good alternative to silicon (Si) due to its high carrier mobility.[1–3] However, to take full advantage of the high-mobility Ge channel, several obstacles should be overcome first, among which the most important one is the high interface trap density (D_{it}) between Ge and the gate stack. Until now, some interface passivation methods have been proposed, such as GeO_x,[4] GeO_xN_y,[5] and GeN_x.[6,7] Among them, the oxygen-based passivation, such as GeO_x, has been proved to be thermally instable, while the nitrogen-based passivation has better thermal stability.[5–8] It is then regarded as a promising passivation method for the Ge MOSFET application. In addition, with downscaling of MOSFETs, the electrical field becomes higher, which makes the surface roughness scattering effect more severe, causing a carrier mobility degradation.[9] Therefore, the surface roughness issue during passivation should also be evaluated and investigated besides the surface passivation and thermal stability. However, there are few results about it at this time. Moreover, the interfacial layer (IL) regrowth during the passivation process should also be carefully accounted for to avoid the sacrifice of the equivalent oxide thickness (EOT).

In this paper, nitrogen plasma passivation (NPP) on Ge is extensively studied in terms of Ge MOS capacitors. The impact of NPP on the surface roughness, D_{it}, and the IL thickness is statistically characterized and discussed.

2. Experimental details

The (111) p-Ge wafers were used as the starting wafers. The NPP process was carried out in a thermal plasma-enhanced chemical vapor deposition (PECVD) chamber. After wet cleaning by dilute HCl, the wafers were loaded into the PECVD chamber with a substrate temperature of 350 °C. The NPP was implemented using pure N_2 with a pressure of 1000 mTorr. The radio-frequency (RF) power for plasma generation was 50 W. The plasma-treating times were 30 s, 1 min, and 2 min, respectively. A wafer without plasma treatment was set as the control sample. After the plasma treatment, the surface morphology was characterized by atomic force microscopy (AFM) in the trapping mode. Besides, to characterize the passivation performance of the NPP, MOS capacitors were also fabricated using the same surface treating method as above. After the NPP passivation, 5 nm Al_2O_3 was deposited as the gate dielectric by thermal atomic layer deposition (ALD) at 200 °C for all MOS capacitors. An Al/TiN gate was deposited by sputtering and patterned by lift-off. The Al/Ti metal was sputtered as the back electrode. After cleaning, post metallization annealing (PMA) was carried out at 375 °C in N_2 for 15 min. The MOS capacitors were characterized, and the EOT and D_{it} were extracted from the capacitance–voltage (CV) results.

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3. Results and discussion

The X-ray photoelectric spectroscopy (XPS) measurement was carried out to evaluate the chemical states of the Ge surface. The results of Ge-3d, N-1s, and O-1s core levels are shown in Fig. 1. The Ge-3d spectra can be divided into at least three component peaks: bulk Ge–Ge, Ge–N_4, and GeO_2, with binding energies of 29.4 eV, 31.5 eV, and 32.9 eV, respectively. The N-1s spectra can be divided into at least two component peaks: N-Ge_3 and N–Ge–O, with binding energies of 397.4 eV and 398.2 eV, respectively. The presence of the Ge–N bond indicates the realization of Ge surface nitridation. However, the oxide components are also observed, mainly resulting from the exposure to air before the XPS measurement.[10] The Ge-3d, N-1s, and O-1s spectra show that the proportion of the nitride components (Ge–N_4 and N–Ge_3) increases with increasing NPP treating time, while the relative intensity of the oxide components (GeO_2 and N–Ge–O) decreases with increasing NPP treating time. This result indicates that the oxide components are not introduced in the NPP process.

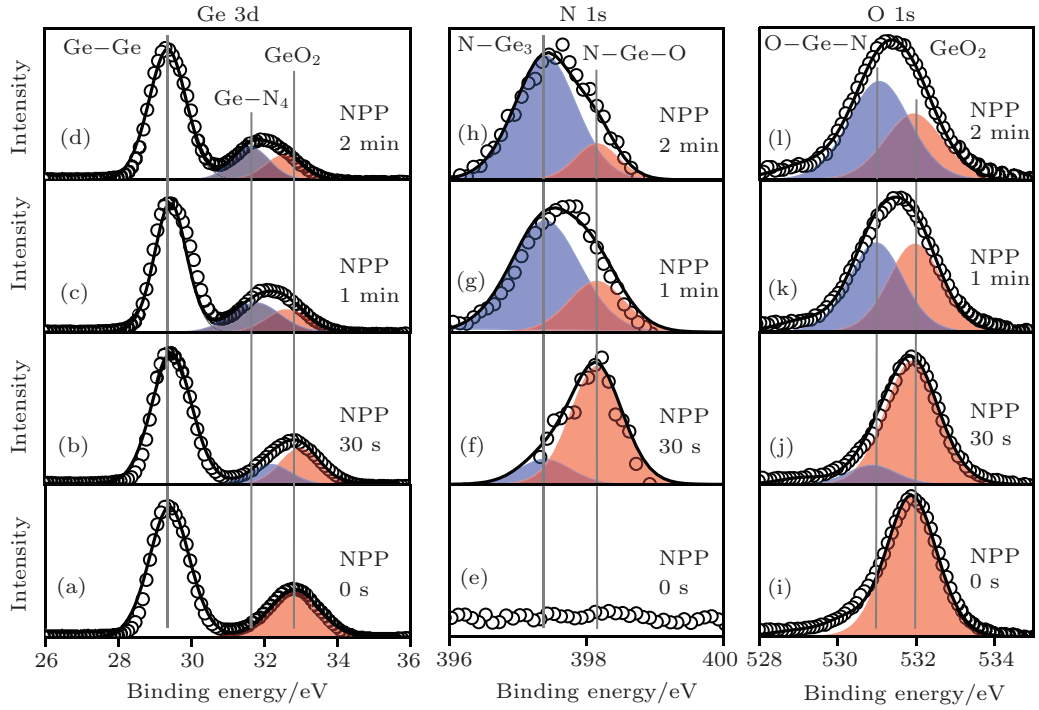


Fig. 1. (color online) XPS spectra of (a)–(d) Ge-3d, (e)–(h) N-1s, and (i)–(l) O-1s core levels, measured in samples with NPP treating time ranging from 0 to 2 min.

The surface roughness of the wafers with NPP was characterized by AFM just after the plasma treatment. The statistical results of the average surface roughness (R_a) are shown in Fig. 2. Compared to the control sample as cleaned, the surface roughness of the wafers with NPP is reduced obviously. As the NPP treating time increases, the surface roughness is further improved. The R_a is reduced about 20% from about 2.4 Å to 1.9 Å after 2 min NPP treatment. The improvement of the surface morphology may be attributed to the reduction of the surface diffusion barrier resulted from the formation of Ge–N clusters, similar to the case of Ge or Si annealed in hydrogen.[11,12] Similar to the Si–H and Ge–H cases, the attaching N to (111)-Ge can also reduce the surface diffusion barrier and roughness by increasing the local density of states (LDOS) at the Fermi level.[11–13]

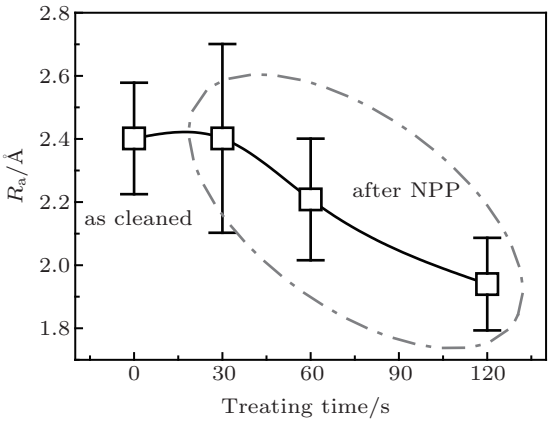


Fig. 2. (color online) Average surface roughness R_a as a function of the NPP treating time.

The MOS capacitance was measured by an Agilent B1500A, as shown in Fig. 3(a). The capacitance in the accumulation region is reduced after the NPP treatment due to

the regrowth of the interfacial layer, while the frequency dispersion is improved. To evaluate the passivation performance of the NPP, D_{it} was extracted using the high–low frequency (HF–LF) method at the minimum points of the low frequency CV curves (C_{lf_min}), as shown in Fig. 3(a). The HF–LF method is described by the following formula:

$$D_{it}=\frac{C_{ox}}{q}\left(\frac{C_{lf}/C_{ox}}{1-C_{lf}/C_{ox}}-\frac{C_{hf}/C_{ox}}{1-C_{hf}/C_{ox}}\right), \quad (1)$$

where C_{ox}, C_{lf}, and C_{hf} represent the oxide, the low-frequency, and the high-frequency capacitances, respectively, and q is the electron charge. Figure 3(b) shows the statistical results of D_{it} as a function of the NPP treating time. A minimum D_{it} of about 5×10^{11} cm^{-2}·eV^{-1} is comparable to the results of other research groups using the GeN_x passivation layer.[6] Compared to the control sample, the samples with NPP show a distinct reduction in D_{it}, indicating the enhancement of the passivation efficiency with the increase of the NPP treating time. This trend is consistent with that of surface roughness improvement. As the NPP treating time increases, the surface passivation uniformity is improved, thus resulting in the reduction of D_{it} and the improvement of the surface roughness. This is very beneficial to controlling the interface trap scattering and the surface roughness scattering in MOSFET at the same time.

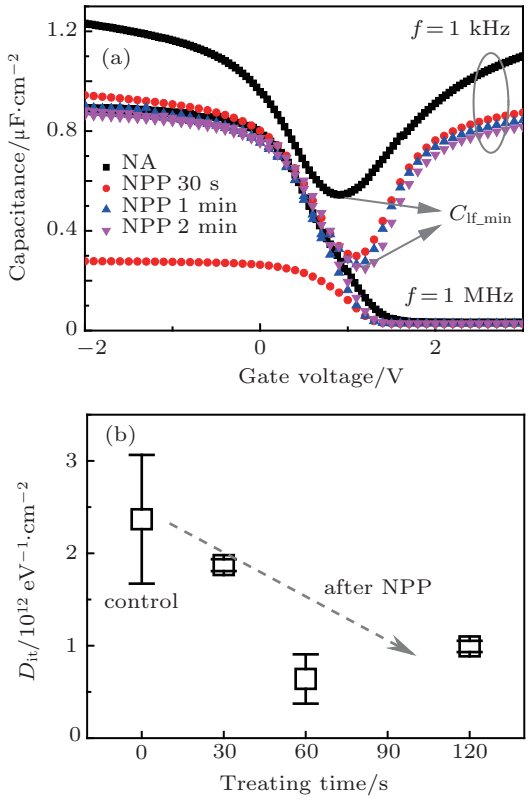


Fig. 3. (color online) (a) CV and (b) D_{it} each as a function of the NPP treating time.

However, as the NPP treating time increases, the EOT also increases, as shown in Fig. 4. Considering the same Al_2O_3 gate oxide for all samples, the increase of the EOT should be attributed to the regrowth of the IL. It is believed that during the passivation process, the nitrogen plasma can diffuse into the Ge substrate and react with Ge atoms to generate a GeN_x IL,[14–17] as illuminated in Fig. 5. The total EOT of the MOS capacitor can be simply described by the following formula:

$$\mathrm{EOT\,(total)=EOT\,(Al_2O_3)+EOT\,(IL)}, \quad (2)$$

where EOT(Al_2O_3) is the EOT of the Al_2O_3 gate oxide, and EOT(IL) represents the EOT increment caused by the IL (also shown in Fig. 4). Compared to the control sample, the EOT(IL) is more than 1 nm for the sample with 2 min NPP treatment. Similar to the case of silicon nitridation, a saturation trend of the GeN_x IL regrowth is observed due to the effect of the barrier against the nitrogen diffusion.[15,16] The increased IL thickness will become a severe problem for EOT scaling,[18] especially in the sub-1 nm EOT era. It will degrade the performance gain by surface morphology improvement and D_{it} reduction.

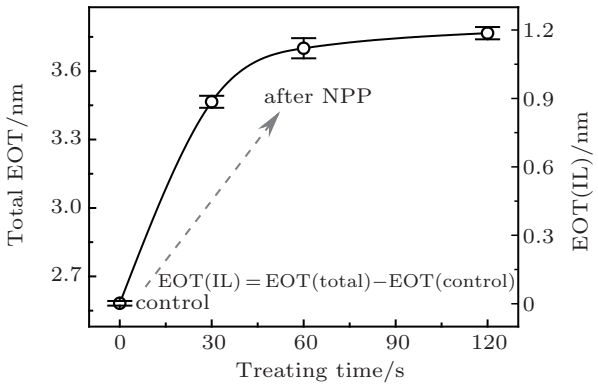


Fig. 4. EOT extracted from low-frequency CV results.

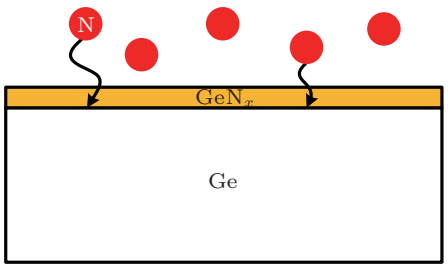


Fig. 5. (color online) Schematic diagram of regrowth of interfacial layer in NPP.

From the above discussion, it is found that a long time NPP treatment is needed to improve the roughness and D_{it}, however it also induces an extradinary increase in the IL thickness, thus being bad for the EOT scaling. To suppress the IL regrowth in the NPP, the process parameters including working pressure, process temperature, RF power, as well as the following PMA should be optimized carefully. For example, reducing the working pressure and the process temperature is believed to suppress the diffusion of N as well as the

IL regrowth. Moreover, a thinner high-k dielectric deposition will be required to recover the disadvantage of NPP induced IL growth. Thanks to the simultaneous improvement of the surface roughness and D_{it}, the NPP process will be a potential solution with great promise for the gate stack of high-performance Ge MOSFETs.

4. Conclusion

Nitrogen plasma passivation has been studied on (111) Ge by thermal PECVD. The results showed that the NPP can improve the surface morphology due to the surface diffusion barrier reduction benefiting from the formation of Ge–N clusters. A 20% reduction in roughness was obtained. Besides, the NPP could reduce the interface trap density, simultaneously, and a minimum D_{it} of about 5×10^{11} cm^{-2}·eV^{-1} was achieved. The improvement of roughness and D_{it} is beneficial for suppressing the surface roughness scattering and the interface-trap scattering in MOSFETs, thus improving the carrier transport. However, the interfacial layer regrowth (EOT(IL) larger than 1 nm) was also observed, which caused a decrease of the gate capacitance. To gain the advantage of NPP on roughness and D_{it} improvement, the NPP process should be optimized to suppress the interfacial layer regrowth. By recovering EOT increasing, the NPP will be a promising solution for future high performance Ge MOSFET gate stack application.

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References

[1] Takagi S, Irisawa T, Tezuka T, Numata T, Nakaharai T, Hirashita N, Moriyama Y, Usuda K, Toyoda E, Dissanayake S, Shichijo M, Nakane R, Sugahara S, Takenaka M and Sugiyama N 2008 *IEEE Trans. Electron. Devices* **55** 21

[2] Caymax M, Eneman1 G, Bellenger F, Merckling C, Delabie A, Wang G, Loo R, Simoen E, Mitard J, De Jaeger B, Hellings G, De Meyer K, Meuris M and Heyns M 2009 *Technical Digest of the International Electron Devices Meeting,* December 7–9, 2009 Baltimore, USA, p. 461

[3] Toriumi A, Lee C H, Wang S K, Tabata T, Yoshida M, Zhao D D, Nishimura T, Kita K and Nagashio K 2011 *Technical Digest of the International Electron Devices Meeting,* December 5–7, 2011 Washington, USA, p. 646

[4] Lee C H, Nishimura T, Nagashio K, Kita K and Toriumi A 2011 *IEEE Trans. Electron. Devices* **58** 1295

[5] Chui C O, Ito F and Saraswat K C 2006 *IEEE Trans. Electron. Devices* **53** 1501

[6] Fukuda Y, Okamoto H, Iwasaki T, Otani Y and Ono T 2011 *Appl. Phys. Lett.* **99** 132907

[7] Bhatt P, Chaudhuri K, Kothari S, Nainani A and Lodha S 2013 *Appl. Phys. Lett.* **103** 172107

[8] Wang S J, Chai J W, Pan J S and Huan A C H 2006 *Appl. Phys. Lett.* **89** 022105

[9] Zhang R, Lin J C, Yu X, Takenaka M and Takagi S 2013 *Microelectron. Eng.* **109** 97

[10] Hayakawa R, Yoshida M, Ide K, Yamashita Y, Yoshikawa H, Kobayashi K, Kunugi S, Uehara T and Fujimura N 2011 *J. Appl. Phys.* **110** 064103

[11] Nayfeh A, Chui C O, Saraswat K C and Yonehara T 2004 *Appl. Phys. Lett.* **85** 2815

[12] Sato N and Yonehara T 1994 *Appl. Phys. Lett.* **65** 1924

[13] Horch S, Lorensen H T, Helveg S, Lagsgaard E, Stensgaard I, Jacobsen K W, Norskov J K and Besenbacher F 1999 *Nature* **398** 134

[14] Schroder D K 2008 *Semiconductor Material and Device Characterization* (2nd edn.) (Dalian: Dalian University of Technology Press) p. 274 (in Chinese)

[15] Kubler L, Bischoff J L and Bolmont D 1988 *Phys. Rev. B* **38** 13113

[16] Maeda T, Yasuda T, Nishizawa M, Miyata N, Morita Y and Takagi S 2006 *J. Appl. Phys.* **100** 014101

[17] Wu C Y, King C W, Lee M K and Chen C T 1982 *J. Electrochem. Soc.* **129** 1559

[18] Zhang R, Iwasaki T, Taoka N, Takenaka M and Takagi S 2011 *Microelectron. Eng.* **88** 1533