Analysis of flatband voltage shift of metal/high-k/SiO_2/Si stack based on energy band alignment of entire gate stack*

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A theoretical model of flatband voltage (V_{FB}) of metal/high-k/SiO_2/Si stack is proposed based on band alignment of entire gate stack, i.e., the V_{FB} is obtained by simultaneously considering band alignments of metal/high-k, high-k/SiO_2 and SiO_2/Si interfaces, and their interactions. Then the V_{FB} of TiN/HfO_2/SiO_2/Si stack is experimentally obtained and theoretically investigated by this model. The theoretical calculations are in good agreement with the experimental results. Furthermore, both positive V_{FB} shift of TiN/HfO_2/SiO_2/Si stack and Fermi level pinning are successfully interpreted and attributed to the dielectric contact induced gap states at TiN/HfO_2 and HfO_2/SiO_2 interfaces.

Keywords: metal gate, high-k dielectric, band alignment, V_{fb} shift

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1. Introduction

The flatband voltage (V_{FB}) tuning is one of the most important issues of metal oxide semiconductor (MOS) device with high-k/metal gate stack. In the literature, the V_{FB} of MOS stack with metal/high-k/SiO_2/Si structure is given as[1–4]

$$V_{FB} = -\frac{Q_{SiO_2,Si}EOT}{\varepsilon_0\varepsilon_{SiO_2}} - \frac{Q_{high-k,SiO_2}d_{high-k}}{\varepsilon_0\varepsilon_{high-k}} - \frac{\rho_{bulk,high-k}d_{high-k}^2}{2\varepsilon_0\varepsilon_{high-k}} + \Delta V_{high-k,SiO_2} + \Delta V_{metal,high-k} + \phi_{ms}, \quad (1)$$

where EOT is the equivalent oxide thickness of the entire high-k/SiO_2 stack; ϕ_{ms} is the vacuum workfunction difference between metal gate and Si substrate; $Q_{SiO_2,Si}$ and Q_{high-k,SiO_2} are the areal charge densities (per unit area) at SiO_2/Si and high-k/SiO_2 interfaces, respectively; $\rho_{bulk,high-k}$ is the bulk charge density (per unit volume) in high-k dielectric. $\Delta V_{high-k,SiO_2}$ and $\Delta V_{metal,high-k}$ are the V_{FB} shift moments due to the possible dipole at high-k/SiO_2 interface and Fermi level pinning (FLP) at metal gate/high-k interface; ε_0, ε_{SiO_2}, and ε_{high-k} express the vacuum permittivity, the relative permittivities of SiO_2 and high-k dielectric, respectively; d_{high-k} is the physical thickness of high-k dielectric. Equation (1) for an MOS stack with metal/high-k/SiO_2/Si structure is derived from simple extension of V_{FB} expression for MOS stack with metal/SiO_2/Si structure. For an MOS stack with metal/SiO_2/Si structure, the V_{FB} can be given as[5]

$$V_{FB} = \phi_{ms} - \frac{Q_{SiO_2,Si}EOT}{\varepsilon_0\varepsilon_{SiO_2}}. \quad (2)$$

For the MOS stack with metal/high-k/SiO_2/Si structure, the contribution of interfacial charges at high-k/SiO_2 interface to the V_{FB} is a linear function of d_{high-k}, and can be given as[1–5]

$$V_{FB,Q_{high-k,SiO_2}} = -\frac{Q_{high-k,SiO_2}d_{high-k}}{\varepsilon_0\varepsilon_{high-k}}. \quad (3)$$

The contribution of bulk charges in high-k dielectric to the V_{FB} is a quadratic function of d_{high-k}, and can be given as[1–5]

$$V_{FB,\rho_{bulk,high-k}} = -\frac{\rho_{bulk,high-k}d_{high-k}^2}{2\varepsilon_0\varepsilon_{high-k}}. \quad (4)$$

In addition, the contributions of metal/high-k and high-k/SiO_2 interfaces to the V_{FB} are denoted as $\Delta V_{high-k,SiO_2}$ and $\Delta V_{metal,high-k}$. Then the V_{FB} of MOS stack with metal/high-k/SiO_2/Si structure in Eq. (1) is linear additivity of Eqs. (2)–(4), $\Delta V_{high-k,SiO_2}$ and $\Delta V_{metal,high-k}$. As a consequence, the effects of following parameters on the V_{FB} are independent of each other: difference between vacuum workfunctions of metal gate and Si substrate, $\Delta V_{metal,high-k}$, bulk charges in the high-k dielectric, interfacial charges at the high-k/SiO_2 interface, $\Delta V_{high-k,SiO_2}$, and interfacial charges at SiO_2/Si interface.

2. Weakness of traditional model

It should be noted that the derivation of Eq. (1) is based on the following assumptions.

(i) $\Delta V_{metal,high-k}$ is determined only by the metal/high-k interface, i.e., the band alignment of metal/high-k interface is determined by this interface itself.

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(ii) $\Delta V_{\text{high}-k,\text{SiO}_2}$ is determined only by high-k/SiO_2 interface, i.e., the band alignment of high-k/SiO_2 interface is determined by this interface itself.

(iii) Both $\Delta V_{\text{metal,high}-k}$ and $\Delta V_{\text{high}-k,\text{SiO}_2}$ are independent of the physical thickness of high-k dielectric, the interfacial charges at high-k/SiO_2 interface, the bulk charges in high-k dielectric, and the interfacial charges at SiO_2/Si interface. In addition, there is no interaction between the metal/high-k and high-k/SiO_2 interfaces.

Several instructive results have been reported to investigate the physical origin of the $\Delta V_{\text{high}-k,\text{SiO}_2}$ and $\Delta V_{\text{metal,high}-k}$.[6–13] These opinions discussed either metal/high-k interface or high-k/SiO_2 interface separately and independently, and the interaction between metal/high-k and high-k/SiO_2 interfaces was not considered. For the case of metal/high-k contact with high-k material semi-infinite, the band alignment of metal/high-k interface is determined only by this interface itself, so is the case for high-k/SiO_2 contact when high-k and SiO_2 are semi-infinite. The above assumptions are reasonable. But according to our previous work, this is not true for MOS samples with finite thickness.[14]

3. New model based on energy band alignment of entire gate stack

In this letter, a theoretical model is proposed to discuss the V_{FB} based on energy band alignment of the entire metal/high-k/SiO_2/Si stack, i.e., the band alignment of the whole stack is established after simultaneously considering band alignments of the metal/high-k, high-k/SiO_2 and SiO_2/Si interfaces and their interactions.

The V_{FB} of MOS device with metal/high-k/SiO_2/Si stack can be obtained after knowing the surface band bend of the Si substrate and the EOT of the entire gate stack. The surface band bend of Si substrate can be obtained by analyzing the band alignment of entire gate stack. The band alignment of the entire metal/high-k/SiO_2/Si stack is built after the band alignments of the respective metal/high-k, highi-k/SiO_2 and SiO_2/Si contacts and their interactions. High-k dielectric materials and SiO_2 can be thought as semiconductors with wide band gap. Thus, the band alignments of all these contacts are determined by the metal/semiconductor or semiconductor/semiconductor contacts interpreted by the model based on gap states.[13,15–19] Band alignment for the metal (semiconductor)/semiconductor (semiconductor) contact is established when the Fermi levels are consistent after charge transfer between the metal (semiconductor) and the semiconductor (semiconductor). These charges are located in the metal, the space charge region of the semiconductor, and the interfacial gap states of the semiconductor. These charges induce voltage drop on the contact and the relative shift of the Fermi level with respect to the bulk energy band so that the Fermi levels of the metal (semiconductor) and semiconductor (semiconductor) are identical. For the metal/high-k/SiO_2/Si structure, there are dielectric contact induced gap states (DCIGS) at the metal/high-k and high-k/SiO_2 interfaces due to the mismatch of materials.[8] The charges transfer among the metal, Si substrate, the DCIGS at the metal/high-k and high-k/SiO_2 interfaces, resulting in potential drop through the entire stack. Finally, the Fermi levels of the metal, high-k, SiO_2, and Si substrate are consistent.

The detailed energy band diagram of a metal/high-k/SiO_2/Si stack is schematically shown in Fig. 1. The various physical parameters are defined as follows: $\phi_{2,\text{L}}$, $\phi_{2,\text{R}}$, $\phi_{4,\text{L}}$, $\phi_{4,\text{R}}$, and ϕ_{S} are the barrier heights measured from the Fermi level to the conduction band minimum on the left and right sides of high-k, the left and right sides of SiO_2, and the Si substrate, respectively; $D_{2,\text{L}}$, $D_{2,\text{R}}$, and $D_{4,\text{L}}$ are the DCIGS densities on the left and right sides of high-k dielectric, and the left side of SiO_2, respectively; the DCIGS at the SiO_2/Si interface are not considered because of low state densities ($\sim 10^{11}$ cm^{-2}). $Q_{2,\text{L}}$, $Q_{2,\text{R}}$, and $Q_{4,\text{L}}$ are the DCIGS charges corresponding to the left and right sides of high-k, and the left side of SiO_2, respectively; Q_3 and Q_5 are the fixed charge densities at the high-k/SiO_2 interface and SiO_2/Si interface; ρ is the bulk charge density in the high-k dielectric; Q_{S} expresses the space charge density of Si substrate; ΔV_1, ΔV_2, ΔV_3, ΔV_4, and ΔV_5 are the potential drops on the gap between metal and high-k, the high-k, the gap between high-k and SiO_2, SiO_2, and the gap between SiO_2 and Si, respectively; ε_0, ε_1, ε_2, ε_3, ε_4, ε_5, and ε_{S} are the vacuum permittivity, the relative permittivities of the gap between metal and high-k, high-k, the gap between high-k and SiO_2, SiO_2, the gap between SiO_2 and Si, and Si substrate, respectively; d_1, d_2, d_3, d_4, and d_5 are the physical thicknesses of the gap between metal and high-k, high-k, the gap between high-k and SiO_2, SiO_2, and the gap between SiO_2 and Si, respectively; $\phi_{2,\text{CNL}}$ and $\phi_{4,\text{CNL}}$ are the differences between the charge neutrality level (CNL) and the valence band maximum for the high-k and SiO_2; $E_{2,\text{g}}$ and $\text{E}_{4,\text{g}}$ are band gaps of the high-k and SiO_2; χ_2, χ_4, and χ_{S} are the electron affinities of the high-k, SiO_2, and Si, respectively; ϕ_{m} is the vacuum work function of metal gate.

For the SiO_2/Si interface, there is the following relation by the inspection of the energy band diagram in Fig. 1.

$$\phi_{4,\text{R}} + \chi_4 = \Delta V_5 + \chi_{\text{S}} + \phi_{\text{S}}. \tag{5}$$

The potential drops ΔV_5 can be obtained by the application of the Gauss's law and the poisson equation to various charges in the whole gate stack

$$\Delta V_5 = \frac{ed_5}{\varepsilon_0 \varepsilon_5}(Q_5 + Q_{\text{S}}). \tag{6}$$

Herein e is the electron charge, and ΔV_5 is defined as positive when the sum of Q_5 and Q_{S} is positive, i.e., positive charges

localized on the right side of SiO_2/Si interface. Otherwise, ΔV_5 is negative, so are the definitions of ΔV_1, ΔV_2, ΔV_3, and ΔV_4. For the space charge density of Si substrate, Q_S can be expressed as[5]

$$Q_S = \pm\left(\frac{2\varepsilon_0\varepsilon_S kTP_0}{e^2}\right)^{1/2}\left\{\left[\exp\left(-\frac{e\Phi_S}{kT}\right)+\frac{e\Phi_S}{kT}-1\right] + \frac{N_0}{P_0}\left[\exp\left(\frac{e\Phi_S}{kT}\right)-\frac{e\Phi_S}{kT}-1\right]\right\}^{1/2}, \quad (7)$$

where k is the Boltzmann constant; T is the temperature in Kelvin; N_0 and P_0 are the equilibrium concentrations of the electrons and holes in the bulk of Si substrate. Φ_S is the surface potential of Si substrate, and is equal to

$$\Phi_S = kT\ln\left(\frac{P_0}{N_i}\right)+0.56-\phi_S, \quad (8)$$

where N_i is the intrinsic carrier concentration of the Si. The Φ_S is negative when the surface band is bent upward while positive when the surface band is bent downward. The Q_S is with the positive sign when Φ_S is negative and negative sign when Φ_S is positive.

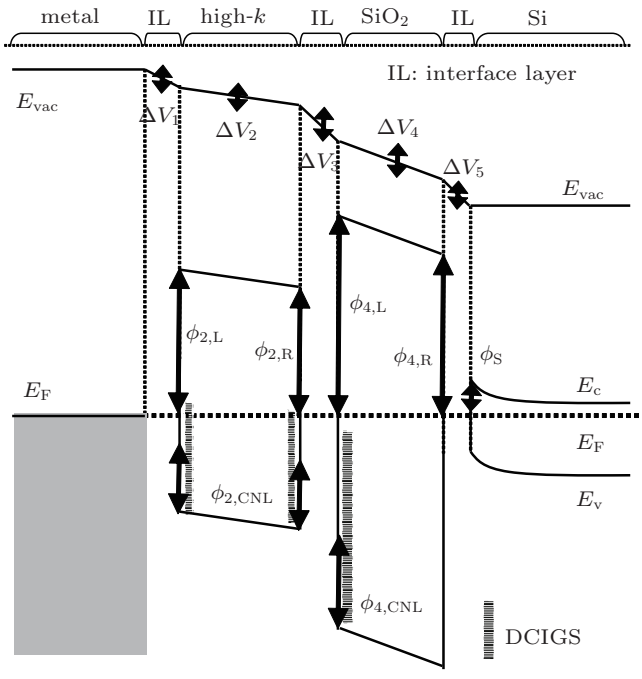


Fig. 1. Energy band diagram of metal/high-k/SiO_2/Si stack.

For the space region of SiO_2, the following equations can be obtained:

$$\phi_{4,L} = \Delta V_4 + \phi_{4,R}, \quad (9)$$

$$\Delta V_4 = \frac{ed_4}{\varepsilon_0\varepsilon_4}(Q_5+Q_S). \quad (10)$$

Similarly, for the high-k/SiO_2 interface, there are the following relations:

$$\phi_{2,R}+\chi_2 = \Delta V_3+\chi_4+\phi_{4,L}, \quad (11)$$

$$\Delta V_3 = \frac{ed_3}{\varepsilon_0\varepsilon_3}(Q_3+Q_{4,L}+Q_5+Q_S). \quad (12)$$

The DCIGS charge densities (cm^{-2}) $Q_{4,L}$ can be expressed as

$$Q_{4,L} = D_{4,L}(\phi_{4,L}+\phi_{4,CNL}-E_{4,g}). \quad (13)$$

For the space region of high-k dielectric, we can obtain

$$\phi_{2,L} = \Delta V_2+\phi_{2,R}, \quad (14)$$

$$\Delta V_2 = \frac{ed_2}{\varepsilon_0\varepsilon_2}\left(\frac{\rho d_2}{2}+Q_{2,R}+Q_3+Q_{4,L}+Q_5+Q_S\right), \quad (15)$$

$$Q_{2,R} = D_{2,R}(\phi_{2,R}+\phi_{2,CNL}-E_{2,g}). \quad (16)$$

For the metal/high-k interface,

$$\phi_m = \Delta V_1+\chi_2+\phi_{2,L}, \quad (17)$$

$$\Delta V_1 = \frac{ed_1}{\varepsilon_0\varepsilon_1}(Q_{2,L}+\rho d_2+Q_{2,R}+Q_3+Q_{4,L}+Q_5+Q_S), \quad (18)$$

$$Q_{2,L} = D_{2,L}(\phi_{2,L}+\phi_{2,CNL}-E_{2,g}). \quad (19)$$

Based on equations above, it can be concluded as follows: for a given stack with several known parameters (ε_1, ε_2, ε_3, ε_4, ε_5, and ε_S; d_1, d_2, d_3, d_4, and d_5; $\phi_{2,CNL}$ and $\phi_{4,CNL}$; Q_3 and Q_5; ρ; $D_{2,L}$, $D_{2,R}$, and $D_{4,L}$; $E_{2,g}$ and $E_{4,g}$; χ_2, χ_4, and χ_S; N_0 and P_0; ϕ_m), the energy band alignment of the entire metal/high-k/SiO_2/Si stack is determined, i.e., the parameters (ΔV_1, ΔV_2, ΔV_3, ΔV_4, and ΔV_5; $Q_{2,L}$, $Q_{2,R}$, $Q_{4,L}$, and Q_S; $\phi_{2,L}$, $\phi_{2,R}$, $\phi_{4,L}$, $\phi_{4,R}$, ϕ_S and Φ_S) can be finally obtained. Then the V_{FB} can be calculated as follows:

$$V_{FB} = -\Phi_S+\frac{eQ_S}{\varepsilon_0}\left(\frac{d_1}{\varepsilon_1}+\frac{d_2}{\varepsilon_2}+\frac{d_3}{\varepsilon_3}+\frac{d_4}{\varepsilon_4}+\frac{d_5}{\varepsilon_5}\right). \quad (20)$$

Thus, the V_{FB} of the metal/high-k/SiO_2/Si stack can be discussed from the physical viewpoint of the energy band alignment of the entire stack. It should be noted that this model is significantly different from the reported literatures. In this model, the V_{FB} of metal/high-k/SiO_2/Si stack is analyzed considering the interactions among the metal/high-k, high-k/SiO_2 and SiO_2/Si interfaces. The band alignments of metal/high-k, high-k/SiO_2 and SiO_2/Si interfaces are affected by each other, i.e., the band alignment of metal/high-k interface is determined by the entire stack but not only the metal/high-k interface, so are the cases for high-k/SiO_2 and SiO_2/Si interfaces.

4. Demonstration of new model

Then the proposed model is used to investigate the experimental V_{FB} of MOS capacitors with TiN/HfO_2/SiO_2/Si structures. All MOS capacitors were fabricated using conventional MOS process.[14] SiO_2 of $\sim$ 20.5 nm in thickness was grown firstly on diluted HF-last (100) n-type Si substrate (1.14×10^{15} cm^{-3}) by thermal oxidation. Then thick SiO_2 was wet etched to have a terraced SiO_2 structure. HfO_2 films

with fixed thicknesses (4.7 nm, 7.0 nm, 9.4 nm, 11.7 nm, or 14.0 nm) were deposited by physical vapor deposition (PVD) on the terraced SiO_2 structure. A 30-nm-thick TiN film and a 50-nm-thick W layer were deposited on the HfO_2 by PVD. In addition, metal gates such as Ta, W, and Ni were also deposited on 11.7-nm HfO_2/terraced SiO_2/Si stack. Capacitance–Voltage (C–V) characteristic was measured at a frequency of 1 MHz. EOT and V_{FB} were extracted from the C–V fitting with quantum effect correction by QMCV model. For an MOS capacitor with metal/high-k/terraced SiO_2/Si structure, the V_{FB}–EOT plot is linear. Herein a physical parameter named delta intercept is introduced, and it is defined to be the difference between the intercept of the V_{FB}–EOT plot for the MOS capacitors with metal/high-k/terraced SiO_2/Si structure and that with metal/terraced SiO_2/Si structure, i.e., MOS capacitors with and without high-k dielectric. Positive delta intercept means positive V_{FB} shift of metal/high-k/SiO_2/Si stack compared with metal/SiO_2/Si stack. Figure 2 shows the experimental results of the delta intercept versus HfO_2 thickness. The slopes of the experimental V_{FB}–EOT plots of TiN/HfO_2/terraced SiO_2/Si stack for different HfO_2 thicknesses are nearly identical (-0.011 to -0.025), which are not shown here. Also shown in Fig. 2 are the theoretical calculation results based on the proposed model. The values of parameters used in the calculation are described as follows: d_1, d_3, and d_5 are all assumed to be 0.3 nm.[15] $E_{2,g}$ and $E_{4,g}$ are 6.0 and 8.9 eV, respectively.[19] χ_2, χ_4, and χ_S are 2.5, 0.9, and 4.05 eV, respectively.[19] ε_1, ε_3, and ε_5 are defined based on the method proposed by Louie *et al.*[15] to be 4.5, 3.2, and 2.9, respectively. ε_4 and ε_S are 3.9 and 11.9, respectively. ε_2 is experimentally extracted to be 18. Based on the proposed model and fitting the experimental results, ϕ_m is calculated to be 4.78 eV for TiN metal gate. $D_{2,L}$ and $D_{2,R}$ are both 7.50×10^{12} $eV^{-1}\cdot cm^{-2}$, and $D_{4,L}$ is 1.65×10^{12} $eV^{-1}\cdot cm^{-2}$. The $\phi_{2,CNL}$ and $\phi_{4,CNL}$ are obtained to be 2.3 and 4 eV, respectively. Q_3, Q_5, and ρ are estimated to be -3×10^{12} cm^{-2}, 2.5×10^{11} cm^{-2} and 2×10^{19} cm^{-3}, respectively. It can be seen from Fig. 2 that the theoretical calculations are in good agreement with the experimental results.

Then the origin of positive V_{FB} shift for the MOS capacitor with TiN/HfO_2/SiO_2/Si structure shown in Fig. 2 is analyzed based on the proposed theoretical model. Figure 2 also shows the delta intercepts for three cases. The first case is considering the charges at the HfO_2/SiO_2 interface, the bulk charges in the HfO_2 and the DCIGS at the TiN/HfO_2 and HfO_2/SiO_2 interfaces. The theoretically calculated results are identical with the experimental data. The second case is only considering the charges at the HfO_2/SiO_2 interface and the bulk charges in the HfO_2 but not considering the DCIGS at the TiN/HfO_2 and HfO_2/SiO_2 interfaces. More negative V_{FB} shifts are induced. The last case is only considering the DCIGS at the TiN/HfO_2 and HfO_2/SiO_2 interfaces but not the charges at the HfO_2/SiO_2 interface and the bulk charges in the HfO_2. More positive V_{FB} shifts are obtained. Thus it can be concluded that the positive V_{FB} shift of the TiN/HfO_2/SiO_2/Si stack relative to the TiN/SiO_2/Si structure is due to the DCIGS at the TiN/HfO_2 and HfO_2/SiO_2 interfaces. It is noted that the delta intercept considering both the charges and the DCIGS is not simply linear additivity of the delta intercepts for the case only considering the charges and the case only considering the DCIGS as shown in Fig. 2.

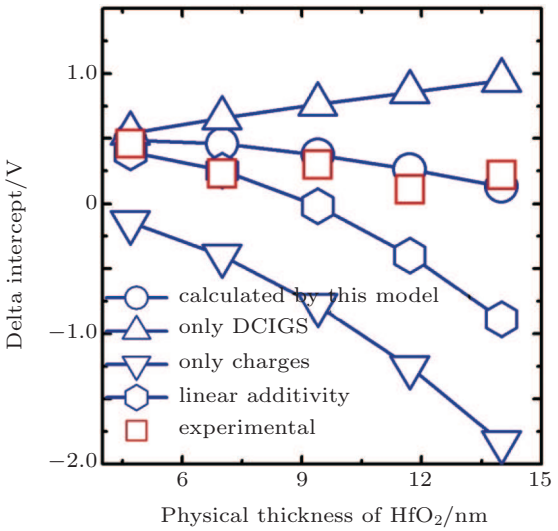


Fig. 2. (color online) Experimental result and theoretical calculation data of delta intercept for sample with TiN/HfO_2/terraced SiO_2/Si structure versus physical thickness of HfO_2.

In addition, the physical origin of the FLP phenomenon[9,21] is demonstrated by this model. When considering the charges at the HfO_2/SiO_2 interface, the bulk charges in the HfO_2 and the DCIGS at the TiN/HfO_2 and HfO_2/SiO_2 interfaces, using the values of the physical parameters above, the V_{FB} of the metal/HfO_2/SiO_2/Si stack is calculated for different metal and the same HfO_2 and SiO_2 as shown in Fig. 3. The slope of the V_{FB} verses the vacuum workfunction ϕ_m is 0.45 which is less than 1. These clarify that the FLP is present. For the case only considering the charges at the HfO_2/SiO_2 interface and in the HfO_2, the slope of the V_{FB} verses ϕ_m is 1 as shown in Fig. 3, which indicates that no FLP appears. For the case only considering the DCIGS at the metal/HfO_2 and HfO_2/SiO_2 interfaces, however, the slope is found to be 0.45. These furthermore clarify that the FLP is also attributed to the DCIGS at the metal/HfO_2 and HfO_2/SiO_2 interfaces. Then the intercept of V_{FB}–EOT plot of the metal/11.7 nm HfO_2/terraced SiO_2/Si stack is calculated for different metals is shown in Fig. 4. The slope of the intercept versus the vacuum workfunction is 0.457 which is less than unit. Furthermore, the experimental results are also shown in Fig. 4. Considering the experimental error, the theoretically calculated data based on

this model are in good agreement with the experimental results, which further confirms the feasibility of our model.

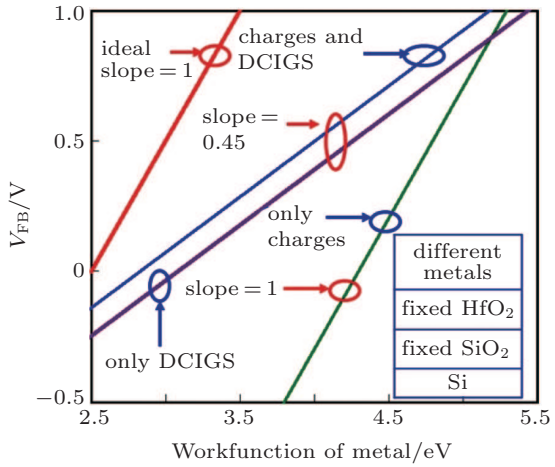


Fig. 3. (color online) Calculated V_{FB} of the metal/HfO_2/SiO_2/Si stack for different vacuum workfunctions of metals. The insert schematically shows the structure of the MOS capacitors.

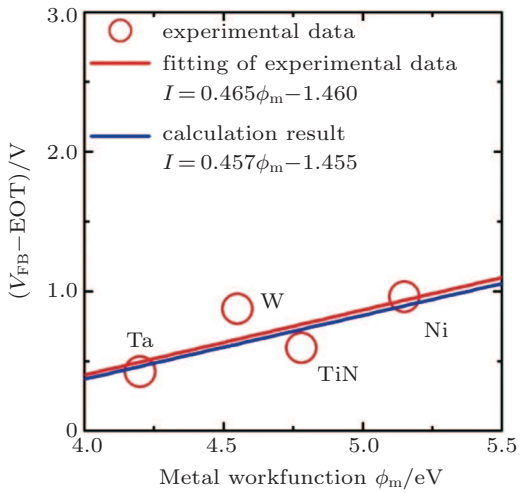


Fig. 4. (color online) Theoretically calculated and experimental intercept of V_{FB}–EOT plot of metal/HfO_2/terraced SiO_2/Si stack versus vacuum workfunction of metal gate. Also shown are the fitting formulas.

5. Conclusion

In conclusion, a theoretical model is proposed to demonstrate the V_{FB} of MOS stack with metal/high-k/SiO_2/Si stack based on the energy band alignment of the entire gate stack. The band alignments of the metal/high-k, high-k/SiO_2, and SiO_2/Si contacts are all simultaneously considered to establish the band alignment of the whole gate stack. The experimental positive V_{FB} shift of the TiN/HfO_2/SiO_2/Si stack and the FLP are successfully interpreted and attributed to the DCIGS at the TiN/HfO_2 and HfO_2/SiO_2 interfaces. The experimental data for the TiN/HfO_2/SiO_2/Si structure are well consistent with the theoretical calculation results based on this model, which further confirms the feasibility of the proposed model.

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