# Impact of substrate injected hot electrons on hot carrier degradation in a 180-nm NMOSFET*

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Although hot carriers induced degradation of NMOSFETs has been studied for decades, the role of hot electron in this process is still debated. In this paper, the additional substrate hot electrons have been intentionally injected into the oxide layer to analyze the role of hot electron in hot carrier degradation. The enhanced degradation and the decreased time exponent appear with the injected hot electrons increasing, the degradation increases from 21.80% to 62.00% and the time exponent decreases from 0.59 to 0.27 with $V_b$ decreasing from 0 V to −4 V, at the same time, the recovery also becomes remarkable and which strongly depends on the post stress gate bias $V_g$. Based on the experimental results, more unrecovered interface traps are created by the additional injected hot electron from the breaking Si–H bond, but the oxide trapped negative charges do not increase after a rapid recovery.

**Keywords:** substrate hot electron injection, hot carrier injection (HCI) degradation, interface trap, oxide trapped charge

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## 1. Introduction

Although hot carrier injection (HCI) degradation has been studied for decades, the role of hot electron was still under debate, several research groups proposed different physical mechanisms to explain the hot carrier degradation, however, the role of hot electron is very inconsistency in these theories.

One important viewpoint is that:[1] the hot electrons, not the hot holes, can directly determine the HCI degradation. However, many researchers proposed that: the hot electrons seem to be insignificant in HCI degradation. There are many evidences to support this theory, the experiments about the degradation of substrate hot electron injection and substrate hot hole injection show that the holes were orders of magnitude more efficient for trap creation,[2] and the HCI degradation peaked at hot hole injection regimes ($V_g \approx V_d/2$ for the older technology and $V_g \approx V_d$ for the advanced technology).[3,4] However, in our experiments, with the substrate injected hot electrons increasing ($V_g = V_d/2$, and $|V_b| > 0$ in our technology), the enhanced degradation, the decreased time exponent and the increased recovery appeared, so the additional injected hot electrons seem to be also important on HCI degradation, compared with that of hot hole, the role of hot electron in HCI degradation needs to be discussed in depth.

The HCI degradation is induced by the oxide trapped surplus charges and the created interface traps.[5–9] The interface traps can be created by breaking the Si–H bonds and the Si–O bonds (large number of the Si–O bonds at the interface).[10,11] The hot holes can break the Si–O bonds and the broken Si–O bonds cannot recover, the $n \approx 0.5$ time exponent of the degradation can be due to breaking the Si–O bonds.[12] Moreover, the broken Si–H bonds can also create the interface traps,[13] and the relatively smaller time exponent can be due to breaking the Si–H bonds,[13] Grasser *et al.* studies[14,15] further proposed that: the interface traps created by breaking the Si–H bonds are also the unrecoverable traps.

Whether or not the oxide trapped negative charges and the unrecoverable interface traps increase after additional hot electrons injecting need to be verified, and in this paper, we will discuss these two HCI degradation mechanisms of hot electron in 180-nm NMOSFETs.

## 2. Device and experimental details

The devices used in our studies are fabricated by a 0.18-μm standard bulk silicon CMOS process, the oxide thickness is 3.8 nm, the gate width is 10 μm. The degradation is measured periodically by using the *I*–*V* curves and the stress induced leakage current (SILC) is used to monitor the oxide traps by using the separated devices. The experiments perform at room temperature (25 °C) and Agilent-4156C Precision Semiconductor Parameter Analyzer is used for the tests.

In the experiments, we select the hot hole injection regimes ($V_g = 1.5$ V and $V_d = 3.0$ V are the hot hole injection regimes for our technology, the conclusion will be verified by our latter experimental results in Fig. 5 in which we can find the peak value of hole current is presented near this DC

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bias condition) to accelerate the degradation ($V_s = V_b = 0$ V for common channel HCI stress and $V_s = 0$ V but $V_b = -1$ V down to $-4$ V for the additional substrate hot electron injection stress). The recovery performs after 2000 s HCI stress and the post stress performs with $V_g = 0$ V and $-2$ V (other terminals are grounded), respectively. According to JEDEC standards,[16,17] we select the $I_{dlin}$ ($I_{dlin}$ is the dc drain current measured when the transistor is biased in the linear region, and the typical dc bias voltages for $I_{dlin}$ measurements are $V_d = 0.1$ V, $V_g = 1.8$ V, $V_b = V_s = 0$ V[16]) as the monitored parameter, and since parameter degradations typically exhibit a power-law behavior, the stress intervals increase by exponential time steps of 2 and the data analysis are fitted by the power-law behavior as recommended in JEDEC standards.[16,17]

## 3. Experimental results

Figure 1 shows the time evolution of $I_{dlin}$ (%) degradation at different $V_b$, the degradation follows a good power law of stress time, the amplitude of the degradation significantly increases and the time exponent clearly decreases with increasing $|V_b|$. The time exponent decreases from 0.59 to 0.27 (as shown in Fig. 1).

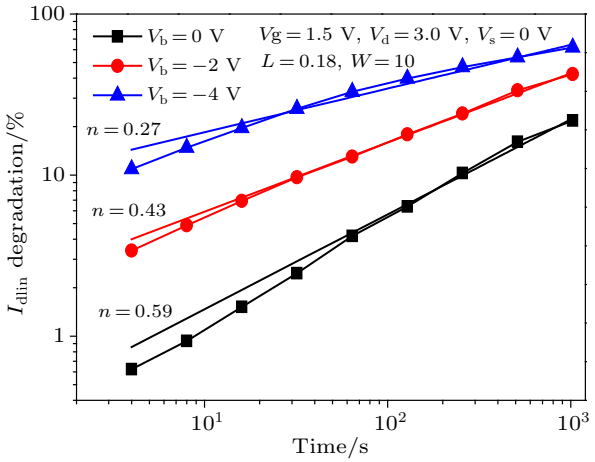



**Fig. 1.** (color online) Time evolution of $I_{dlin}$ (%) for HCI degradation at different $V_b$.

Figure 2 further shows the relationship between $I_{dlin}$ (%) degradation and $V_b$, the measurements perform at 100 s and 1000 s after the HCI stress. With the injected hot electrons increasing, the amplitude of the degradation extremely increases, and an interesting inflexion also appears near $|V_b| =$ 2 V region which is independence of the gate length ($L$). The experimental results also show that the degradation increases as $L$ decreases.

Figure 3 shows the fractional recovery of $I_{dlin}$ degradation at different $V_b$ and different post stress $V_g$, the recovery shows visibly increase as $|V_b|$ increases at $V_g = 0$ V, and the recovery significantly increases with $|V_g|$ increasing.

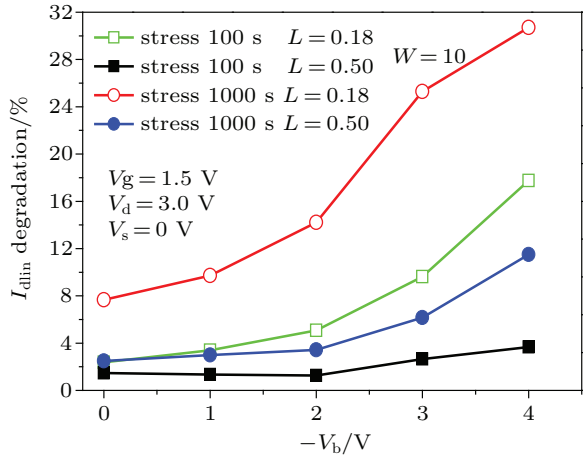



**Fig. 2.** (color online) Relationship between degradation of $I_{dlin}$ (%) and $V_b$ at different $L$.

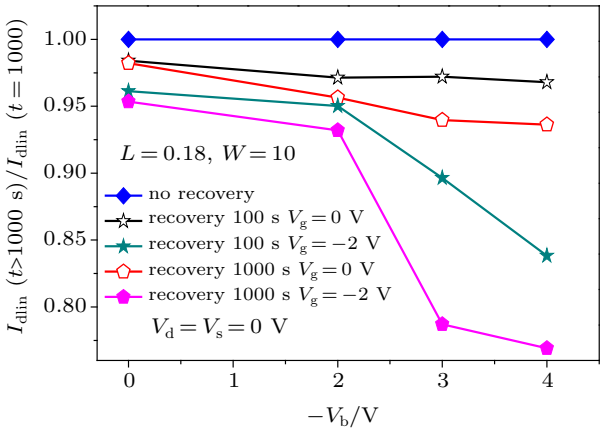



**Fig. 3.** (color online) Fractional recovery of $I_{dlin}$ after 1000 s stress and subsequent 100 s/1000 s post stress.

## 4. Discussion

The hot hole created defects depend on the population of the hot hole.[2,4,10,11] With $|V_b|$ increasing, the population of the electron in the inversion layer will decrease due to the body effects, the impact ionization will weaken, and the population of the hot hole coming from the impact ionization will decrease. The impact ionization induced substrate hole currents ($I_b$) are further monitored in additional experiments for two different samples. As shown in Fig. 4, $I_b$ decreases a little at $V_b = -2$ V but remarkably decreases at $V_b = -4$ V in both the two samples, the results indicate that: the impact ionization rate decreases with $|V_b|$ increasing, and the population of the hot hole coming from the impact ionization also decreases with $|V_b|$ increasing, the conclusion was also consistent with that in Mahapatra *et al.*' Monte Carlo simulations (Fig. 4 in Ref. [10]).

The gate currents ($I_g$) are also monitored in the same experiments for these two samples. However, as shown in Fig. 5, $I_g$ significantly increases with increasing $|V_b|$, this indicates that more and more electrons gain enough energy to overcome the interface barrier to pass through the gate oxide

with increasing $|V_b|$, so the population of the hot electron significantly increases, the conclusion was also consistent with that in Mahapatra *et al.*'s Monte Carlo simulations (Fig. 3 in Ref. [10]). All of these experimental results show that: the hot holes induced degradation are correspondingly decreases, the enhanced degradation must be induced by the additionally injected hot electrons.

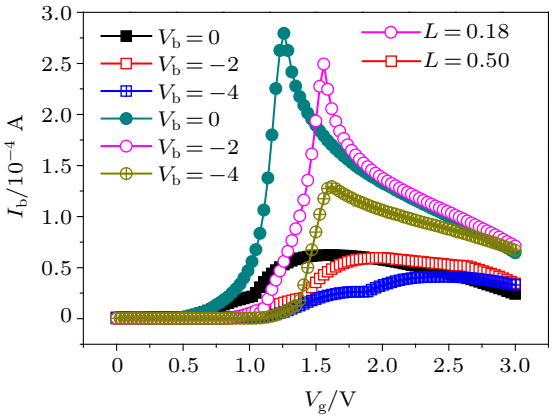



**Fig. 4.** (color online) Substrate impact ionization induced hole current at different $V_b$.

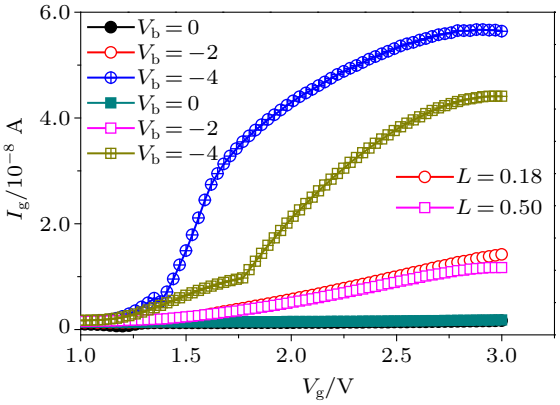



**Fig. 5.** (color online) Gate current at different $V_b$.

In order to further study the inside physical details of NMOSFET at different $|V_b|$ stress, three dimensional NMOSFET is constructed by Technology Computer Aided Design (TCAD) tool and the numerical simulations are performed. The geometric structure of NMOSFET comes from the layout used to fabricate the experimental sample, as shown in Fig. 6. Due to the good look-inside capability, three-dimensional TCAD simulation has been proven to be a useful mean for investigating the inside mechanism of device.[18–23] In the simulations, the degradation process is simulated by the lucky cot-carrier injection model, Fowler–Nordheim tunneling model is used for modelling the gate tunneling current, the impact ionization is simulated by the avalanche model, and hydrodynamic model is used for carrier transport.

The impact ionization rates along channel section and channel cut line (corresponding to different $|V_b|$) are shown

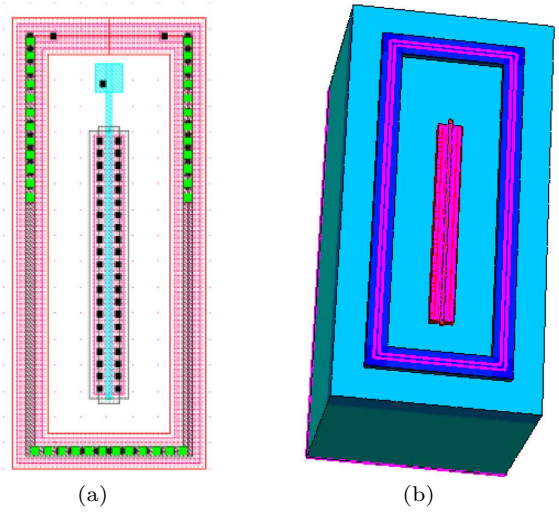



**Fig. 6.** (color online) Layout structure (a) and device model in TCAD (b).

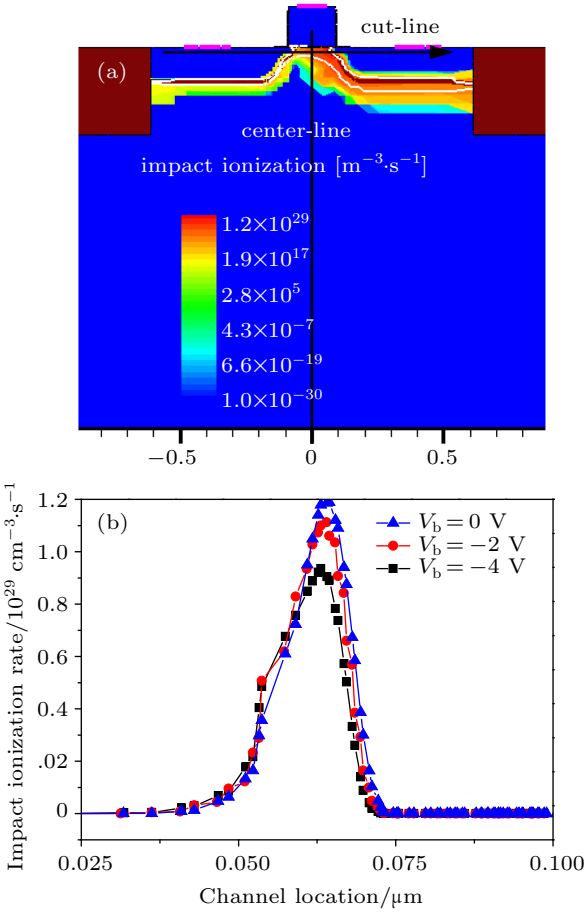



**Fig. 7.** (color online) Impact ionization rates along channel section (a) and channel cut line for different $V_b$ (b).

in Fig. 7, the simulation results show that the peak value of the impact ionization rate is presented at the depletion region (near the drain) and the rate decreases with increasing $|V_b|$, so the peak value of hole density is also presented at the depletion region and the population also decrease with $|V_b|$ increasing (as shown in Fig. 8(a)). However, as shown in Fig. 8(b), though the population of the electron in the channel region decreases

due to the body effects with $|V_b|$ increasing, the population of the electron is still two orders of magnitude more than that of the holes, so the hole is insignificant in the channel.

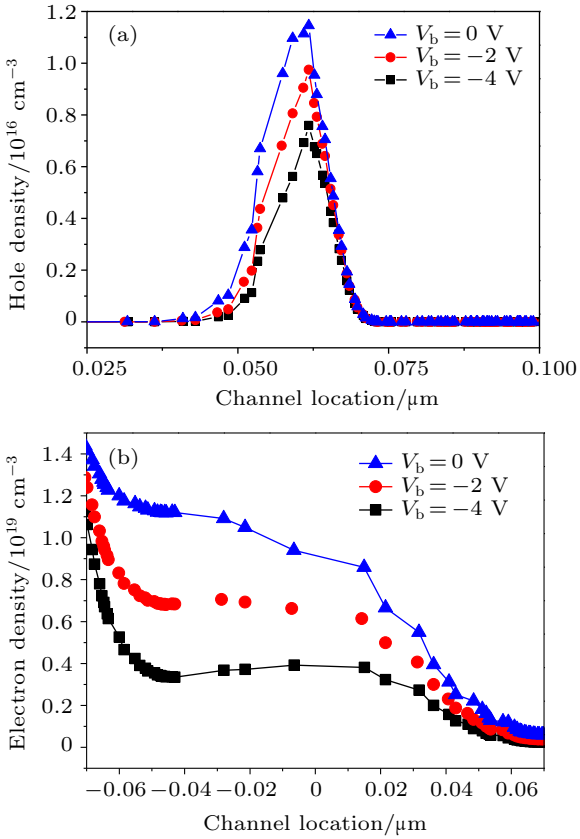



**Fig. 8.** (color online) Density of hole (a) and electron (b) for different $V_b$.

The velocities of the carries along the channel cut line are also shown in Fig. 9, when $|V_b|$ increases from 0 V to 4 V, the velocity of the electron increases. Especially, the velocity increases by more than four times near the source (the peak value of electrons density is near the source but the peak value of hole density is near the drain, as shown in Fig. 8). However, the velocity of the hole is almost unchanged near the drain and the velocity of electron is much larger than that of hole in this region. All of the simulation results show that the population and the velocity of the hole are more insignificant than that of the electron, so the results further indicated the enhanced degradation must be induced by the additionally injected hot electrons.

After hot electrons being additionally injected into the oxide layer, the interface traps may be created and the surplus negative charges may be trapped in the oxide layer. However, the enhanced degradation and the decreased time exponent seem to come from additional interface traps being created by the additional injected electrons,[24,25] because the additional injected hot electrons do not increase the oxide trapped negative charges after a rapid recovery. The SILC is usually used to monitor oxide traps,[2,4] the decrease of the SILC comes from the increase of the tunnel electrons been trapped. As shown in Fig. 10, when the stress is interrupted periodically to measure the SILC, the SILC shows an interesting time evolution (as shown in Fig. 10), which significantly decreases with $|V_b|$ increasing (strong dependence on $|V_b|$), but after a rapid recovery, the oxide trapped negative charges is almost independent on $|V_b|$, so the additional injected hot electrons do not increase the oxide trapped negative charges. Moreover, with the post gate bias stress decreasing to −2 V, the oxide trapped negative charges are reduced and the population is also almost independent of $|V_b|$ after a rapid recovery. With post gate bias stress decrease, the electrons trapped into the deep level oxide traps can gain enough energy to achieve activation energy to release from the traps, so the oxide trapped negative charges decrease and the recovery becomes remarkable. Finally, the enhanced degradation and the decreased time exponent should be coming from additional interface traps being created by the additional injected electrons.

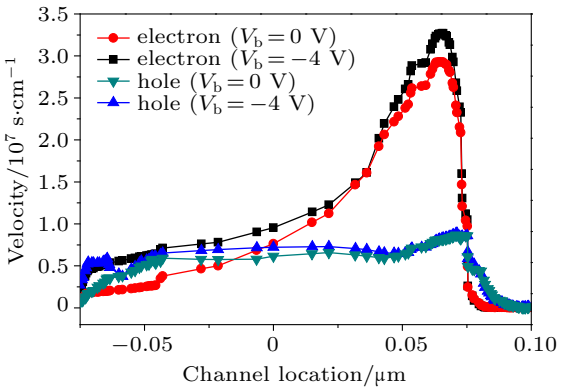



**Fig. 9.** (color online) Velocity of electron and hole for different $V_b$.

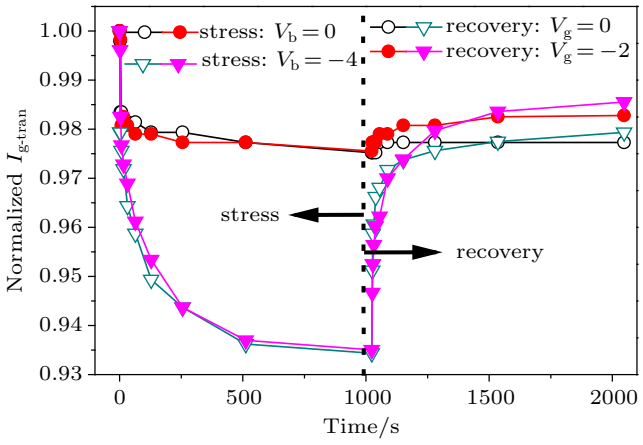



**Fig. 10.** (color online) Time evolution of $I_{g\text{-}tran}$ at different substrate bias.

Do the injected hot electrons really create the unrecoverable interface traps? Figure 11 shows the time evolution of the $I_{dlin}$ (normalized) at different substrate bias (unfortunately, the unintentional recovery induced by the measurement periods makes the recovery relatively smaller than the one in Fig. 3, but which does not affect the permanent degradation). After

a quick recovery at the post stress $V_g = 0$ V, the remained permanent degradation achieves saturation and is almost unchanged with anneal time increasing, but permanent degradation significantly increases with $|V_b|$ increasing, the experimental results show that the unrecoverable interface traps actually created with the additional hot electrons injection. After a quick recovery at the post stress $V_g = -2$ V, the remained permanent degradation also achieves saturation and is also almost unchanged with anneal time increasing, the electrons trapped into the deep level oxide traps can gain enough energy to achieve activation energy to release from the traps, so the recovery increases at the post stress $V_g = -2$ V. Thus, the enhanced degradation comes from additional interface traps being created by the additional injected electrons, and the interface trap comes from the breaking Si–H bond due to the decreased time exponent.[12,13]

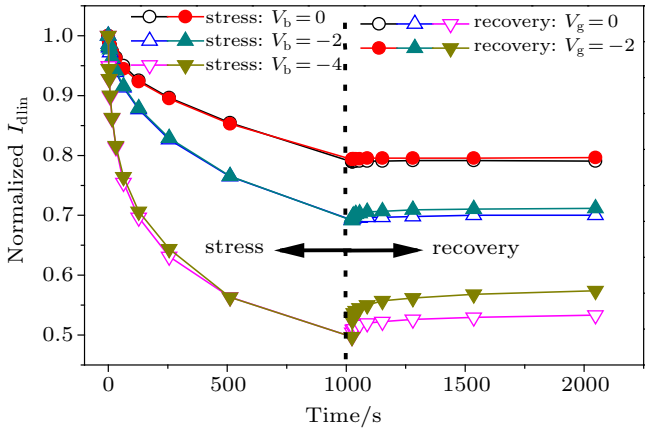



**Fig. 11.** (color online) Time evolution of $I_{dlin}$ at different substrate bias.

## 5. Conclusion

In this paper, the role of hot electron in the HCI degradation have been studied and discussed, the substrate hot electrons have been intentionally injected into the oxide layer to analyze the impact of hot electron on HCI degradation. The experimental results show that: the amplitude of the degradation increase but the time exponent decrease as the injected hot electron increases, and the recovery also becomes remarkable and which strongly depends on the post stress gate bias $V_g$. Based on the experimental results, more unrecovered interface traps are created by the additional injected hot electron from the breaking Si–H bond, but the oxide trapped negative charges do not increase after a rapid recovery.

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