Effect of gate length on the parameter degradation relations of PMOSFET under NBTI stress*

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The influence of PMOSFET gate length on the parameter degradation relations under negative bias temperature instability (NBTI) stress is studied. The threshold voltage degradation increases with reducing the gate length. By calculating the relations between the threshold voltage and the linear/saturation drain current, we obtain their correlation coefficients. Comparing the test result with the calculated linear/saturation current value, we obtain the ratio factors. The ratio factors decrease differently when the gate length diminishes. When the gate length reduces to some degree, the linear ratio factor decreases from greater than 1 to nearly 1, but the saturation factor decreases from greater than 1 to smaller than 1. This results from the influence of mobility and the velocity saturation effect. Moreover, due to the un-uniform distribution of potential damages along the channel, the descending slopes of the curve are different.

Keywords: negative bias temperature instability (NBTI), gate length, degradation

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1. Introduction

With the rapid development of very large scale integrated circuit technology, the size of the MOSFET is shrinking. As MOSFETs are scaled down, operating voltage does not reduce with the same scale. Thus, the channel electric field and the oxide electric field increase significantly, which leads to a more serious negative bias temperature instability (NBTI) effect. The NBTI becomes one of the factors that restrict the life of MOS devices.[1–6] People have extensively studied the NBTI degradation models through a variety of methods, including reaction–diffusion model, electrochemical reaction model, etc.[7–10] However, few researchers focus on the impact of the size of devices on the NBTI effect. Theoretically, the NBTI stress is a uniform gate stress, and device degradation depends only on relevant parameters of vertical structure.[11–13] However, the diminution of device size still has an important influence on the NBTI. The device degradation is closely related to its horizontal structure, which makes people believe that the horizontal structure must be taken as one of the important factors.[14–18] Therefore, in this paper, we focus on the effect of PMOSFET gate length on the relationship of parameter degradation under the NBTI stress, including threshold voltage, mobility, and drain current. It is obvious that they have a close correlation. The impact of the gate length on device degradation is mainly caused by the un-uniform distribution of potential damages along the channel.

2. Devices

The PMOSFETs used here are of the surface channel. They were manufactured by using a 90-nm process technology with lightly doped drain (LDD) structure and shallow trench isolation (STI) scheme. The devices used here have a gate width of 10 μm, ultra-thin gate oxide thickness of 1.4 nm, and different sizes of gate length. The temperature stress is 120 °C/150 °C, and the gate voltage stress V_g is −1.8 V/−2.0 V, with source, drain, and substrate grounded.

3. Experiments and analysis

3.1. Device degradation under NBTI stress

Figure 1 shows the relationship of device threshold voltage V_{th} shifts and NBTI stress time in the double logarithmic coordinate. We can find that the absolute values of the threshold voltage shift increase with the stress time. From the definition of the device threshold voltage, the negative drift of threshold voltage means the generation of positive charges, including the interface traps and the oxide traps during stress.[19]

The preliminary study[20–22] has shown that under the action of holes in the inversion layer, the Si–H bond energy is weakened at the Si/SiO_2 interface. It brings about breaking of Si–H bonds at high temperature, which forms the dangling bond of silicon, namely, interface trap, and H^+ that can migrate into the oxide layer. The H^+ and holes that have got into the gate oxide drift to the gate electrode under the gate electric

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field and they are easily captured by oxide traps. Meanwhile, H^+ nearby interface reacts with Si–H bond to produce H_2. H_2 diffuses to the gate electrode and promotes forward reaction. Resultant interface traps and positive charges in the oxide layer lead to a threshold voltage shift and the drive current decrease. From Fig. 2, both transfer characteristics and output characteristics of PMOS devices degrade obviously after NBTI stress. Therefore, MOS circuits will be seriously impacted, and that is why the NBTI effect attracts extensive attention.

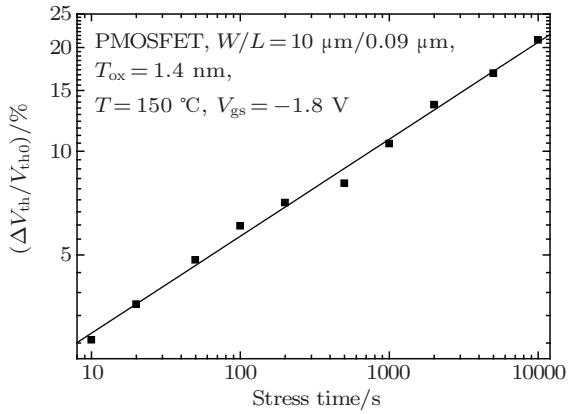


Fig. 1. Relationship between threshold voltage shift percentage V_{th}/V_{th0} and stress time.

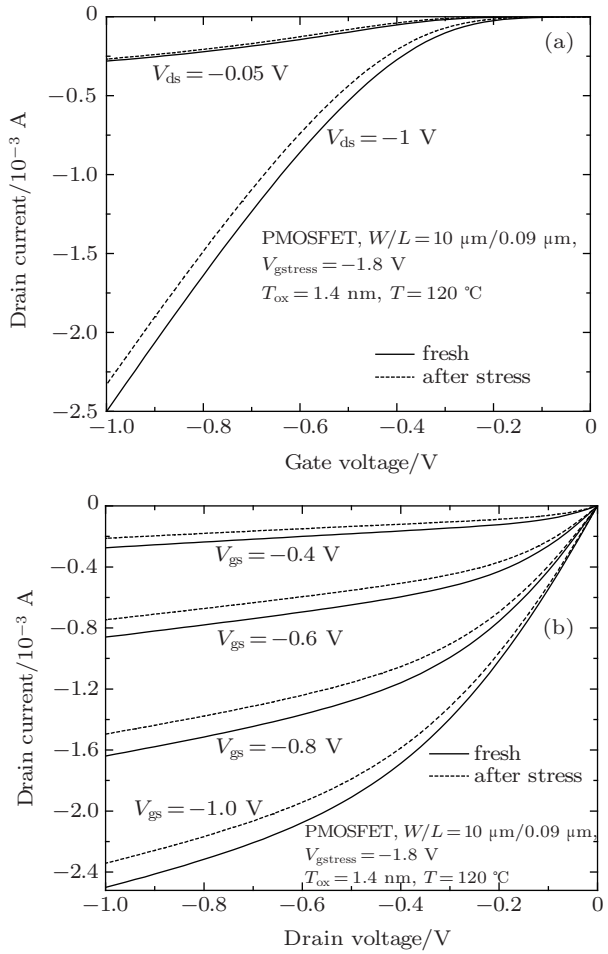


Fig. 2. Device characteristics before and after NBTI stress. (a) Transfer characteristics; (b) output characteristics.

3.2. Effects of gate length on NBTI threshold voltage degradation in PMOSFETs

Under NBTI stress condition, relationship between threshold voltage shifts of different channel lengths and different gate lengths is shown in Fig. 3. The gate lengths of PMOSFETs range from 1 μm to 0.09 μm. It is clearly shown that the gate length has an important effect on the NBTI degradation. We can see that the NBTI degradation obviously increases along with the shortening gate length. In double logarithmic coordinates, the NBTI degradation and gate length meet the linear relation in the form of

$$\Delta V_{th}\% = AL^{-B}, \tag{1}$$

where both A and B are constants.

The obvious relationship between the NBTI degradation and the gate length shows that un-uniform degradation damages along the channel appear in the NBTI stress process. According to the characteristics of NBTI stress, there is a kind of uniform stress along the channel, which means that there is no voltage drop along the channel. Hence, the un-uniform degradation damage is not related to the horizontal electric field, but related to an un-uniform distribution of potential damages along the channel. From the analysis of the experiment, we can know that this phenomenon is caused by the un-uniform distribution of potential damages in the gate–drain region, the gate–source region, and the middle of the channel. Damages at the edge of the channel are more serious than that in the middle. Thus, while the gate length L reduces, the percentage of the edge region will increase, which causes a strong edge effect.[23]

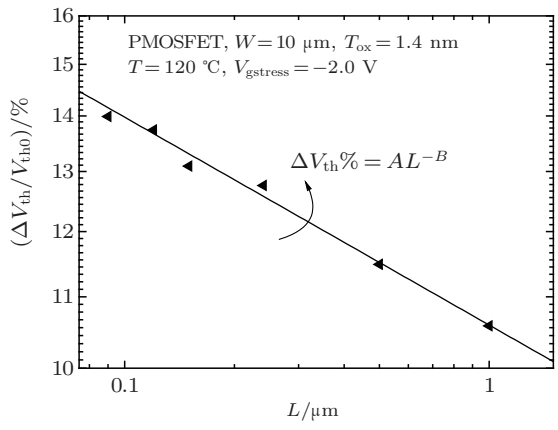


Fig. 3. Relationship between the threshold voltage shift and the gate length under NBTI stress.

3.3. Effect of gate length on degradation of NBTI parameters in PMOSFETs

3.3.1. Drain current shifts over stress time

Figures 4(a) and 4(b) show saturation drain current shifts over stress time respectively in the linear coordinate and double logarithmic coordinate. Figures 5(a) and 5(b) show the

same situation of linear drain current. Drain current degradation constantly gets increasingly serious as stress time increases. In addition, it is clear that the drain current degradation in the saturated zone is more serious than that in the linear zone. While the degradation of the threshold voltage is most obvious during the NBTI stress process, drain current degradation is affected by the threshold voltage shift greatly. With previous analysis, under high temperature and negative bias condition, Si–H bonds break to produce traps at the Si/SiO_2 interface and H-related species. H-related species will be captured by the traps of the oxide layer. At the same time, some holes can get into gate oxide and be trapped in a negative bias condition, which produces oxide layer positive charge. The two factors cause threshold voltage V_{th} to shift under NBTI stress. No doubt, it can influence drain current. We can conclude that the threshold voltage shifts influence the saturation and linear drain current degradation through their relations with threshold voltage.

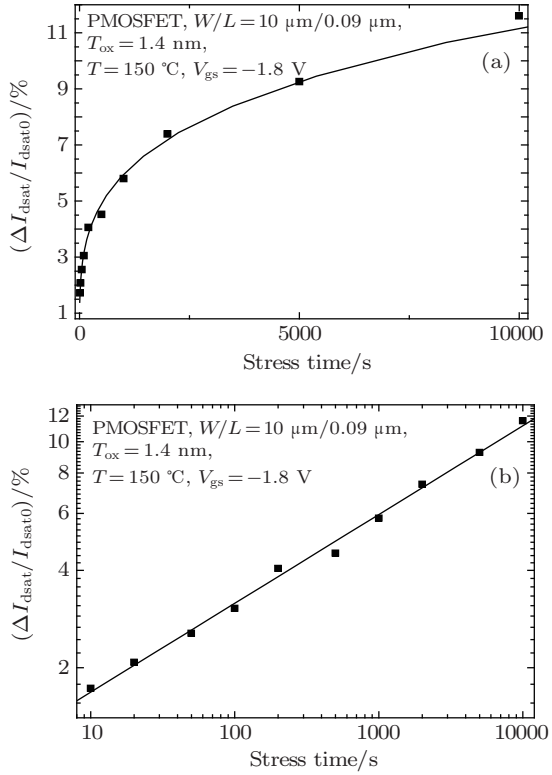


Fig. 4. Saturation drain current shift percentage. (a) Linear coordinate; (b) double logarithmic coordinate.

Saturation drain current is given by

$$I_{dsat}=\frac{Wu_nC_{ox}}{2L}(V_{gs}-V_{th})^2=\frac{\beta}{2}(V_{gs}-V_{th})^2. \tag{2}$$

The differential of threshold voltage is calculated by

$$\begin{aligned}\frac{dI_{dsat}}{dV_{th}} &= -\beta(V_{gs}-V_{th})=-\frac{\beta(V_{gs}-V_{th})^2/2}{1/2(V_{gs}-V_{th})}\\ &= -2\frac{I_{dsat}}{V_{gs}-V_{th}}.\end{aligned} \tag{3}$$

Adjusting the order, we obtain

$$\frac{dI_{dsat}}{I_{dsat}}=-2\frac{dV_{th}}{V_{gs}-V_{th}}. \tag{4}$$

The approximation of the above formula is

$$\frac{\Delta I_{dsat}}{I_{dsat}}=-2\frac{\Delta V_{th}}{V_{gs}-V_{th}}. \tag{5}$$

The coefficient between the threshold voltage and the saturation drain current is 2.

Then we can analyze the relationship between the linear drain current and the threshold voltage. The linear drain current formula reads

$$I_{dlin}=\frac{Wu_nC_{ox}}{L}(V_{gs}-V_{th})V_{ds}=\beta(V_{gs}-V_{th})V_{ds}. \tag{6}$$

The differential of threshold voltage is calculated by

$$\frac{dI_{dlin}}{dV_{th}}=-\beta V_{ds}=-\frac{\beta(V_{gs}-V_{th})V_{ds}}{(V_{gs}-V_{th})}=-\frac{I_{dlin}}{V_{gs}-V_{th}}. \tag{7}$$

Adjusting the order, we obtain

$$\frac{dI_{dlin}}{I_{dlin}}=-\frac{dV_{th}}{V_{gs}-V_{th}}. \tag{8}$$

The approximation of the above formula is

$$\frac{\Delta I_{dlin}}{I_{dlin}}=-\frac{\Delta V_{th}}{V_{gs}-V_{th}}. \tag{9}$$

The coefficient between the threshold voltage and the linear drain current is 1.

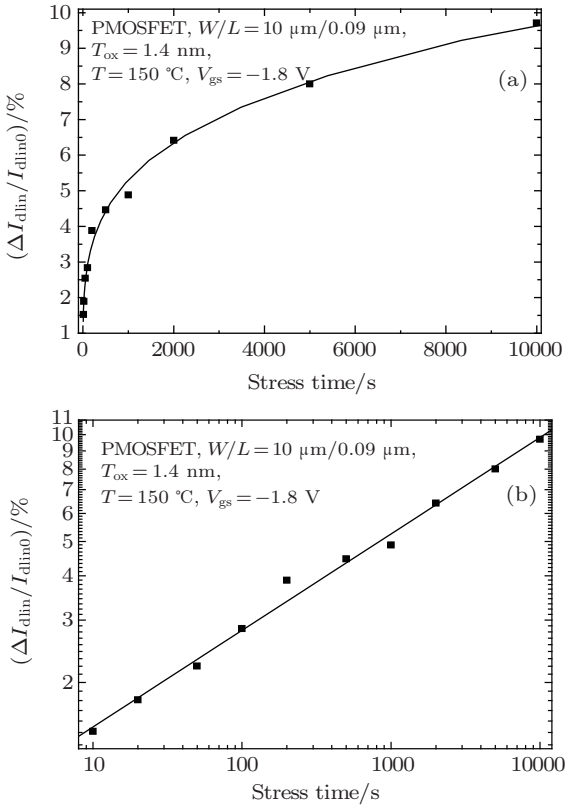


Fig. 5. Linear drain current shift percentage. (a) Linear coordinate; (b) double logarithmic coordinate.

From the above analysis, the impact factors of threshold voltage shifts are different to the two drain currents. The impact factor to saturation drain current degradation is 2 and that to linear drain current is 1. Different effects of the threshold voltage shifts on drain current degradations are the reason why their degradation amount is different. Except for the effect on the threshold voltage, the increase in interface traps and oxide charges can also enhance the scattering effect of carriers. It results in the drop of effective velocity of carriers. That is to say, the mobility declines. The mobility has a significant impact on drain currents, which is because the linear drain current is closely related to all the defects in the channel of the saturation drain current portion.

3.3.2. Effect of gate length on drain current shifts

We now obtain the relation between device parameter degradations during the NBTI stress process, where the relation between the threshold voltage degradation and the linear drain current degradation is

$$\frac{\Delta I_{\rm dlin}}{I_{\rm dlin}} = -\frac{\Delta V_{\rm th}}{V_{\rm gs} - V_{\rm th}}, \tag{10}$$

and the relation between the threshold voltage degradation and the saturation drain current degradation is

$$\frac{\Delta I_{\rm dsat}}{I_{\rm dsat}} = -2\frac{\Delta V_{\rm th}}{V_{\rm gs} - V_{\rm th}}. \tag{11}$$

Here, the drain current shifts with different gate lengths are solved by calculating Eqs. (10) and (11), and then compared with their test values.

Figure 6 shows the relation between the calculated values and the test values of linear drain current shifts with a gate length of 0.1 μm. From this figure, we can see that they are consistent with each other in this condition.

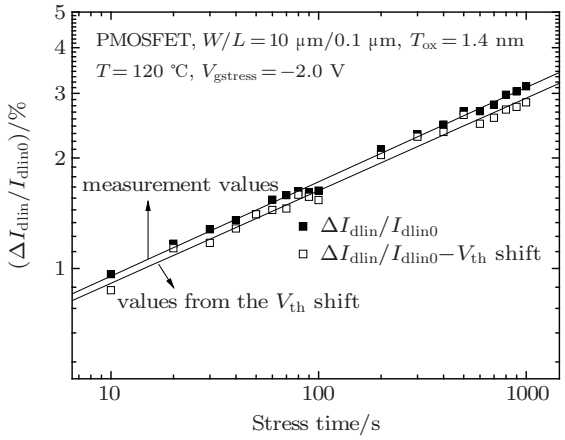


Fig. 6. Relationship between calculated/test values of linear drain current shifts with a gate length of 0.1 μm and time.

As device degradation is closely related to the gate length during the NBTI stress process, we extract the calculated linear drain current shift values with various gate lengths. The relationship between the ratio (R) of the test shift values to the calculated shift values and the gate length L is shown in Fig. 7. It is clear that R decreases gradually from a value greater than 1 to nearly 1 at the point where the gate length is approximately 0.1 μm. A ratio larger than 1 means that the test value of linear drain current shifts is larger than the calculated one. Except for the influence of threshold voltage, mobility can also affect the drain current. The part over 1 can be taken as the effects from mobility. The R decreases to nearly 1 along with decreasing gate length L, which illustrates that the influence of mobility is weakened and almost becomes very weak for ultra-short channel devices. That is because the shorter the channel is, the less the influencing mechanism, like lattice scattering. It results in that the linear drain current is almost controlled by the threshold voltage shift in ultra-short channel devices. Moreover, R has good linear relations with gate length L, which can lay the foundation for the extrapolation prediction method.

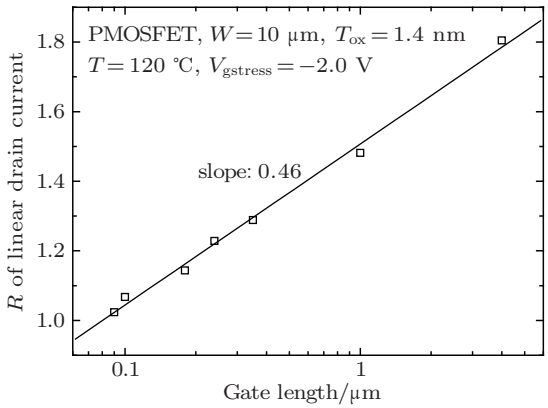


Fig. 7. Relationship of linear drain current shift test values to calculated values ratio and gate length.

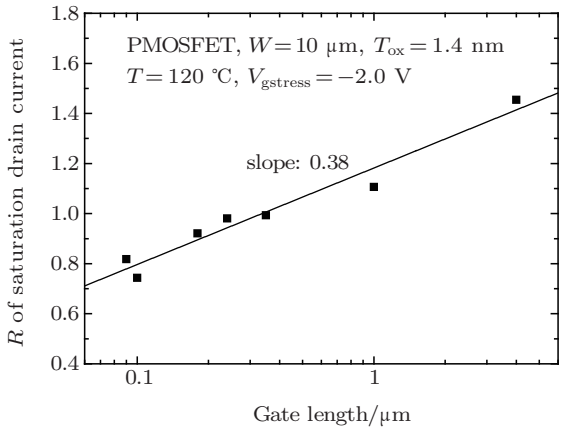


Fig. 8. Relationship of saturation drain current shift's test values to calculated values and gate length.

Meanwhile, we extract the saturation drain current shift calculated with threshold voltage for comparison with the test value, as shown in Fig. 8. It shows the relationship between the ratio R of the test shift values to calculated shift values and gate lengths L. From Fig. 8, we can also see that, along with L diminishing, R decreases gradually from the value larger than

1, and the value is near to 1 when the gate length is approximately 0.24 μm. R becomes less than 1 when gate length L further decreases. Decreasing R also illustrates that the influence of mobility gradually weakens. In the meantime, the descending slope 0.38 is smaller than that of linear drain current shift data 0.46.

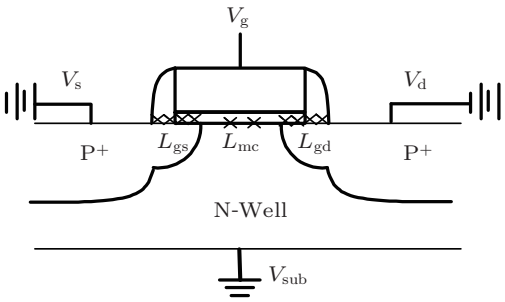


Fig. 9. Schematic diagram of the non-uniform distribution of damage in three parts.

From above analysis, damages at the edge of the channel are more serious than damage in the middle. Damages along device channel are shown in Fig. 9.[23] This can explain the smaller decreasing slope. Saturation drain current shields the more seriously damaged gate–drain overlapped area. With decreasing gate length L, what impacts the mobility of saturation drain current is the center area of the channel. Since the damage of the center area is less than that of the overlapped region, the mobility is less influenced. From the data of the linear drain current, we can know that the all channel area impacts the values while L is diminishing. As a result, descending slope of saturation drain current data is smaller than that of linear drain current.

The calculated value R does not finish at value 1, like linear drain current, but changes to be smaller than 1. It illustrates that we have to take other factors into account when it comes to short channel devices, besides mobility.

We start with the equation of the saturation drain current in the short channel device. Previous derivation of the formula was performed with the saturation drain current in a long channel device, which does not take the velocity saturation effect into account. While the gate length L reduces to a certain extent, the drift electric field within the channel becomes very high under high drain voltage and it is easy to reach the critical field E_c ($= 2\times10^4$ V/cm) where the carrier velocity saturation occurs. Then drain carrier velocity will be saturated, namely, the carrier velocity saturation effect. The saturation drain current at this moment is given by

$$I_{dsat} = \beta(E_cL)^2\left\{\left[\left(\frac{V_{gs}-V_{th}}{E_cL}\right)^2+1\right]^{1/2}-1\right\}. \tag{12}$$

The relationship between the saturation drain current shift and the threshold voltage shift is described as followes:

$$\frac{dI_{dsat}}{I_{dsat}} = -\frac{dV_{th}}{(V_{gs}-V_{th})+(E_cL)^2\left\{1-\left[\left(\frac{V_{gs}-V_{th}}{E_cL}\right)^2+1\right]^{1/2}\right\}\Big/(V_{gs}-V_{th})}, \tag{13}$$

$$\frac{\Delta I_{dsat}}{I_{dsat}} = -\frac{\Delta V_{th}}{(V_{gs}-V_{th})+(E_cL)^2\left\{1-\left[\left(\frac{V_{gs}-V_{th}}{E_cL}\right)^2+1\right]^{1/2}\right\}\Big/(V_{gs}-V_{th})}. \tag{14}$$

On account of $(E_cL)^2 \ll V_{gs}-V_{th}$, $(E_cL)^2/(V_{gs}-V_{th})$ can be negligible, and the above formula can be written as

$$\begin{aligned}\frac{\Delta I_{dsat}}{I_{dsat}} &= -\frac{\Delta V_{th}}{(V_{gs}-V_{th})+(E_cL)^2\left\{1-\left[\left(\frac{V_{gs}-V_{th}}{E_cL}\right)^2+1\right]^{1/2}\right\}\Big/(V_{gs}-V_{th})} \approx -\frac{\Delta V_{th}}{(V_{gs}-V_{th})+\frac{(E_cL)^2-E_cL(V_{gs}-V_{th})}{V_{gs}-V_{th}}}\\ &= -\frac{\Delta V_{th}}{(V_{gs}-V_{th})\left(1+\frac{(E_cL)^2/(V_{gs}-V_{th})-E_cL}{V_{gs}-V_{th}}\right)} \approx -\frac{\Delta V_{th}}{(V_{gs}-V_{th})(1-\frac{E_cL}{V_{gs}-V_{th}})},\\ \frac{\Delta I_{dsat}}{I_{dsat}} &= n\frac{\Delta V_{th}}{V_{gs}-V_{th}}, \quad 1<n<2.\end{aligned} \tag{15}$$

From the above analysis, we can know that when it comes to short channel, the factor between saturation drain current shift and threshold voltage shift is n $(1<n<2)$, which is smaller than the previously-mentioned factor 2. Hence, when the saturation drain current shift is calculated with threshold voltage shift, factor 2 will make the final calculated value larger than the actual theoretical calculated value. Thus, the ratio of the test value to the calculated value is smaller than 1.

4. Conclusions

In conclusion, the gate length has a significant impact on the device parameter degradation. It does not only affect the

degradation of the most important parameter, threshold voltage, in the NBTI stress process, but also affect that of mobility, drain current, etc. It results in a strong link between parameter degradations' relationship and gate length. The effect of gate length on device degradation is principally because of the potential damages' un-uniform distribution along the channel.

References

[1] Nguyen D D, Kouhestani C, Kambour K E and Devine R A B 2013 *J. Vac. Sci. Technol. B* **31** 030610

[2] Krishnan A T, Chakravarthi S, Nicollian P, Reddy V and Krishnan S 2006 *Appl. Phys. Lett.* **88** 153518

[3] Campbell J P, Lenahan P M, Krishnan A T and Krishnan S 2005 *Appl. Phys. Lett.* **87** 204106

[4] Tang C J, Ma H C, Wang T and Chan C T 2007 *Device and Materials Reliability* **74** 518

[5] Devine R A B, Mee J K, Hjalmarson H P, Quevedo-Lopez M A and Alshareef H N 2009 *J. Appl. Phys.* **106** 024508

[6] Grasser T and Kaczer B 2009 *Electron Devices* **56** 1056

[7] Houssa M, Aoulaiche M, Gendt D S and Groeseneken G 2005 *Appl. Phys. Lett.* **86** 093506

[8] Hussin H, Muhamad M, Abdul W Y and Shahabuddin S 2013 *Electron Devices and Solid-State Circuits* **35** 1

[9] Yang J B, Chen T P, Tan S S, Ng C M and Chan L 2008 *Appl. Phys. Lett.* **93** 013501

[10] Campbell J P, Cheung K P, Suehle J S and Oates A 2008 *Appl. Phys. Lett.* **93** 033512

[11] Grasser T, Entner R, Triebl O and Enichlmair H 2006 *Simulation of Semiconductor Processes and Devices* **68** 330

[12] Ota K, Saitoh M, Nakabayashi Y, Ishihara T, Uchida K and Numata T 2012 *Appl. Phys. Lett.* **100** 212109

[13] Ang D S, Wang S, Du G A and Hu Y Z 2008 *Device and Materials Reliability* **8** 2234

[14] Cellere G, Valentini M G and Paccagnella A 2004 *IEEE Integrated Circuit Design and Technology* **79** 303306

[15] Chung S S, Chen S J, Yang W J and Yang J J 2001 *IEEE International Reliability Physics Symposium* **69** 419424

[16] Chung S S, Yeh C H, Feng H J, Lai C S, Yang J J, Chen C C, Jin Y, Chen S C and Liang M S 2006 *IEEE Device and Materials Reliability* **61** 95101

[17] Lee Y H, Wu K, Linton T, Mielke N, Hu S and Wallace B 2000 *IEEE International Reliability Physics Symposium* **84** 77102

[18] Jha N K, Reddy P S and Rao V R 2005 *IEEE International Reliability Physics Symposium* **21** 524528

[19] Schroder D K and Babcock J A 2003 *J. Appl. Phys.* **94** 0118

[20] Cao Y R, Ma X H, Hao Y and Tian W C 2010 *Chin. Phys. B* **19** 097306

[21] Cao Y R, Ma X H, Hao Y, Zhang Y, Yu L, Zhu Z W and Chen H F 2007 *Chin. Phys.* **16** 1140

[22] Cao Y R, Hu S G, Ma X H and Hao Y 2008 *Chin. Phys. Lett.* **25** 3393

[23] Cao Y R, Ma X H, Hao Y and Tian W C 2010 *Chin. Phys. Lett.* **27** 037301