# Pattern imprinting in deep sub-micron static random access memories induced by total dose irradiation

Zheng Qi-Wen(郑齐文)[a)b)c)], Yu Xue-Feng(余学峰)[a)b)†], Cui Jiang-Wei(崔江维)[a)b)], Guo Qi(郭 旗)[a)b)], Ren Di-Yuan(任迪远)[a)b)], Cong Zhong-Chao(丛忠超)[a)b)c)], and Zhou Hang(周 航)[a)b)c)]

[a)] *Key Laboratory of Functional Materials and Devices for Special Environments, Xinjiang Technical Institute of Physics and Chemistry, Chinese Academy of Sciences, Urumqi* 830011, *China*

[b)] *Xinjiang Key Laboratory of Electronic Information Material and Device, Urumqi* 830011, *China*

[c)] *University of Chinese Academy of Sciences, Beijing* 100049, *China*

(Received 12 February 2014; revised manuscript received 7 April 2014; published online 10 August 2014)

Pattern imprinting in deep sub-micron static random access memories (SRAMs) during total dose irradiation is investigated in detail. As the dose accumulates, the data pattern of memory cells loading during irradiation is gradually imprinted on their background data pattern. We build a relationship between the memory cell's static noise margin (SNM) and the background data, and study the influence of irradiation on the probability density function of ΔSNM, which is the difference between two data sides' SNMs, to discuss the reason for pattern imprinting. Finally, we demonstrate that, for micron and deep sub-micron devices, the mechanism of pattern imprinting is the bias-dependent threshold shift of the transistor, but for a deep sub-micron device the shift results from charge trapping in the shallow trench isolation (STI) oxide rather than from the gate oxide of the micron-device.

**Keywords:** total dose irradiation, static random access memory, pattern imprinting, deep sub-micron

**PACS:** 61.80.Ed, 61.82.Fk, 85.30.Tv, 07.85.–m **DOI:** 10.1088/1674-1056/23/10/106102

## 1. Introduction

Pattern imprinting on irradiated sub-micron static random access memories (SRAMs) was reported by John and Michael.[1] As the dose accumulates, the data pattern of memory cells loading during irradiation is gradually imprinted on their background data pattern, which takes place before permanent burn-in. The background data pattern refers to the data stored in device following a power OFF/ON cycle. Due to the asymmetry caused by transistor variation, memory cells have a preferred state, and they always assume this state upon power-up.[2] Before irradiation, the distribution of background data pattern is typically random and about equally divided between zeros and ones over the entire memory. The distribution is changed when a data pattern is stored in the memory and the memory is then irradiated.

Experimental and theoretical analysis indicates that the bias-dependent shift in threshold of transistors, the so-called "pull-up p-channel metal–oxide–semiconductor (PMOS) transistors" (Q3, Q4) and "pull-down n-channel metal–oxide–semiconductor (NMOS) transistors" (Q1, Q2) as shown in Fig. 1, is the reason for pattern imprinting in these micron devices. Radiation will shift the thresholds of the various transistors by charge trapping in the gate oxide and it is well known that the bias state of the transistor during irradiation affects the magnitude of this threshold shift.[3] For the memory cell, radiation will tend to turn on pull-down NMOS transistors and to turn off pull-up PMOS transistors. Meanwhile, the effect of radiation is larger at ON-bias for NMOS transistor in contrast to OFF bias for PMOS transistor. Due to the bias effects noted above, the larger effect for the NMOS transistor will reinforce the ON-bias NMOS transistor rather than counter the ON-bias PMOS transistor. Thus, in both cases, the radiation should tend to reinforce the state that the memory cell is in during irradiation, and will shift the cell toward a preference for that state at a subsequent power-up.[1]

For deep sub-micron SRAMs, the gate oxide thickness of the transistor is thinner than 6 nm, where the oxide traps generated during total dose irradiation are eliminated by tunnel annealing; therefore, the above analysis for micron device is not applicable for the deep sub-micron device.[3] Although the gate oxides of deep sub-micron transistors are naturally tolerant to total dose irradiation, the shallow trench isolation (STI) oxide used to isolate transistors still has a thickness of several 100 nm, which is expected to be very sensitive to radiation. The charge trapping in the STI oxide results in excessive leakage by inverting the channel of the parasitic transistor in the NMOS transistor.[4] Several studies conducted on total dose effect of deep sub-micron SRAMs have revealed that the OFF-state leakage of pull-down NMOS transistors induced by radiation is bias-dependent, changing the electrical characteristic of a memory cell.[5–8] Moreover, because minimum or nearly minimum-geometry transistors are commonly used in SRAM cells, the charge trapping in the STI oxide also leads to a threshold shift in pull-up PMOS transistors and pull-down NMOS transistors, which is well known as the "radiation-induced narrow channel effect" (RINCE).[9] The threshold shift in a deep sub-micron narrow channel transistor is also bias-dependent, having the same bias-dependence

†Corresponding author. E-mail: yuxf@ms.xjb.ac.cn

© 2014 Chinese Physical Society and IOP Publishing Ltd 

as the threshold shift of micron transistors induced by charge trapping in the gate oxide.[10,11] Then, a question arises that whether pattern imprinting takes place on deep sub-micron SRAMs, and what are the reasons for the bias-dependent OFF-state leakage, threshold shift induced by RINCE, or together? To the best of our knowledge, to date there has been no study to check whether pattern imprinting takes place on deep sub-micron SRAMs under total dose irradiation.

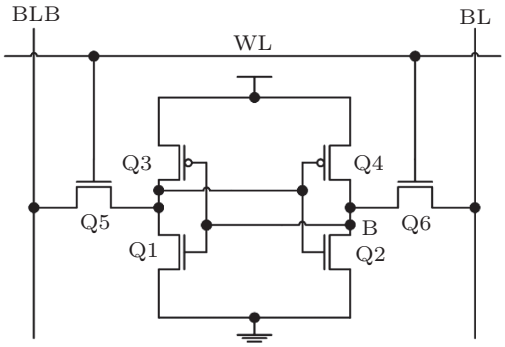



**Fig. 1.** Six-transistor (6-T) SRAM cell. Q1 and Q2 are the pull-down NMOS transistors, Q3 and Q4 are the pull-up PMOS transistors, Q5 and Q6 are the access transistors. WL is the word line, BL and BLB are the bit lines.

In this paper, we select four types of commercial SRAMs, which are fabricated by deep sub-micron complementary metal–oxide–semiconductor (CMOS) technology, to investigate pattern imprinting of those devices. Our study shows that pattern imprinting also takes place on deep sub-micron SRAMs. We build a relationship between background data pattern and SNM of memory cell, and then determine the reason of pattern imprinting by analyzing the effects of the bias-dependent OFF-state leakage and threshold shift on memory cell's SNM.

## 2. Device and experimental procedure

Experiments are performed on four types of commercial SRAMs, which are manufactured by deep sub-micron CMOS technology, detailed information about these devices is listed in Table 1. The radiation experiments are carried out on a $^{60}$Co-$\gamma$ ray in The Xinjiang Technical Institute of Physics and Chemistry, Chinese Academy of Sciences, with a dose rate of 1 Gy(Si)/s. Prior to irradiation, a fixed data pattern (00h, FFh, 55h, AAh) is written into device, and then the device is set to be in standby operation condition during irradiation. Before the irradiation sequence and after each irradiation step, we read and record the background data pattern of the device to observe whether pattern imprinting takes place. At the same time, we make a functional test and measure the standby current with the same and complemental radiation data pattern stored in device. All of the tests are performed on Verigy V93000 SOC autotest equipment.

**Table 1.** Characteristics of the SRAMs used for the experiments.

| Device ID | Vendor | Memory organization | Feature size/μm | Cell type |
|---|---|---|---|---|
| IDT71V124 | IDT | 128 K×8 bit (1 Mbit) | 0.18 | 6-T |
| IS61V5128AL | ISSI | 512 K×8 bit (4 Mbit) | 0.18 | 6-T |
| HM62V8100I | renesas | 1024 K×8 bit (8 Mbit) | 0.18 | 6-T |
| HM62V16100I | renesas | 1024 K×16 bit (16 Mbit) | 0.13 | 6-T |

## 3. Experimental results

Figure 2 shows the background data pattern of device HM62V8100I at each irradiation step, and a fixed data pattern FFh is written into the device during irradiation. Due to the large number of memory cells in a device, we only select a small area to show in the bitmap reading data pattern FFh for device following a power OFF/ON cycle. It can be seen in the figure that the white points represent passed cells; that is, memory cells store "1" as background data. Meanwhile, the black points indicate failed cells; that is, cells store "0" as background data.

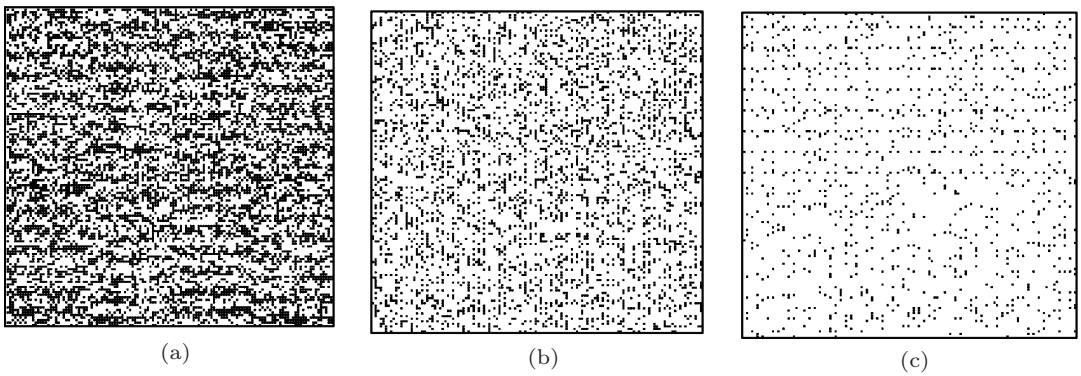



**Fig. 2.** Background data patterns of HM62V8100I in different states: (a) fresh, (b) 2000 Gy(Si), and (c) 3000 Gy(Si).

As we can see from Fig. 2, prior to irradiation, memory cells with "0" and "1" as background data are randomly and almost evenly distributed. As total dose increases, cells with "0" as background data gradually upset to "1". We can calculate that there are 4178737 memory cells with background data "1" before irradiation, accounting for 49.81% of total memory cell array. Accumulated to 2000 Gy(Si), the number is 6550540, occupying 78.09%. Then, at 3000 Gy(Si), the number reaches 7548992, 90% of the total cells. Moreover, similar results are obtained for the case that 00h, 55h, AAh data patterns are written into device during irradiation. The above experimental results show that the data pattern loading during radiation is imprinted on the background data pattern by total dose irradiation for HM62V8100I. The other three types of SRAMs show the same experimental results as HM8100. Therefore, we conclude that patterning imprinting also takes place on these deep sub-micron SRAMs.

## 4. Discussion

### 4.1. Relationship between SNM and background data

Due to the asymmetry caused by transistor variation, memory cells have a preferred state as their background data. The major source of transistor variation is its threshold variation due to the fluctuations in a small number of dopant atoms in the channel.[12] With the scaling of transistor dimensions, microscopic variations in number and the location of dopant atoms in the channel region of the device induce increasingly limiting electrical deviations in the device characteristics. These atomic-level intrinsic fluctuations cannot be eliminated by the external control of the manufacturing process and are most pronounced in minimum-geometry transistors, which are commonly used in area-constrained circuits, such as SRAM cells. Furthermore, intrinsic fluctuations are independent of transistor location on a chip.[13] The threshold mismatch between neighboring cell transistors due to intrinsic fluctuations typically results in a preferred state in SRAM cells.

We can use cell's SNM to quantitate their asymmetry. The SNM of a memory cell is defined as the side length of square with longest diagonal in region I and region II, as shown in Fig. 3. SNM equals the minimum DC noise voltage necessary to flip the state of a cell and characterizes the stability of data storage for SRAM cell, a larger SNM means that the data storage is more stable.[14] If the SNM of the data "0" is larger than data "1", then the background data of cell is data "0" due to data "0" being more stable; inversely, the background data is data "1". So the difference between two data sides of SNM can be used to quantitate the cell's asymmetry, and then determine their background data. We use Eq. (1) to express the relationship between SNM and background data as

$$\Delta\text{SNM} = \text{SNML}-\text{SNMR}, \tag{1}$$

$$\text{Background data} = \begin{cases} \text{"0"} & \Delta\text{SNM} < 0, \\ \text{"1"} & \Delta\text{SNM} > 0. \end{cases} \tag{2}$$

Because the fluctuation of dopant atoms in the channel is random, the threshold of transistor satisfies the Gauss distribution and the standard deviation increases with CMOS scaling. From the International Technology Roadmap for Semiconductors (ITRS), the standard deviation of threshold for minimum area transistor of 0.18-μm process is 23 mV.[12] We can obtain the probability density function of cell's ΔSNM with Monte Carlo simulations using statistical transistor models, including the threshold variation by H Simulation Program with Integrated Circuit Emphasis (HSPICE). Because minimum or nearly minimum-geometry transistors are commonly used in SRAM cells, the standard deviation of threshold in our simulation is selected to be 23 mV. The distribution functions of the threshold and the $W/L$ ratio for SRAM cell transistors used in our simulation are listed in Table 2.

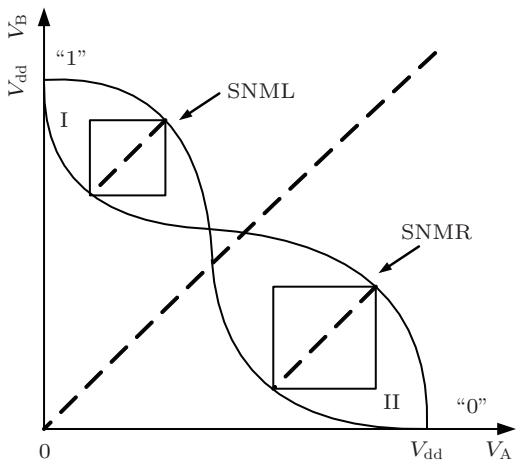



**Fig. 3.** Definition of SNM for memory cell.

**Table 2.** SRAM cell transistors sizing and distribution functions of threshold.

| Transistor type | $W/L$ ratio | Distribution function of threshold |
|---|---|---|
| Pull-up PMOS transistor | 0.22 μm/0.18 μm | GAUSS(0.4639236,0.023) |
| Pull-down NMOS transistor | 0.35 μm /0.18 μm | GAUSS(0.4736658,0.023) |
| Access NMOS transistor | 0.22 μm /0.18 μm | GAUSS(0.4736658,0.023) |

Figure 4 shows the simulation result for ΔSNM, the probability density function determined by threshold variations of SRAM cell transistors. As seen in the figure, the ΔSNM of a SRAM cell also meets a Gauss distribution, the mean value is 0.133 mV, and the standard deviation is 4.172 mV. The mean value of ΔSNM can be approximated to 0 mV relative to the standard deviation, which means that the probability of ΔSNM$>0$ equals that of ΔSNM$<0$, so the cells with "1" as background data have the same number as the cells with "0" as background data, which is in accordance with the experimental data as shown in Fig. 2(a). The randomness of the Gauss distribution for ΔSNM indicates that memory cells with "0" and "1" as background data are randomly distributed over the entire memory. As discussed above, the probability density function of ΔSNM can represent the background data pattern of the device very well.

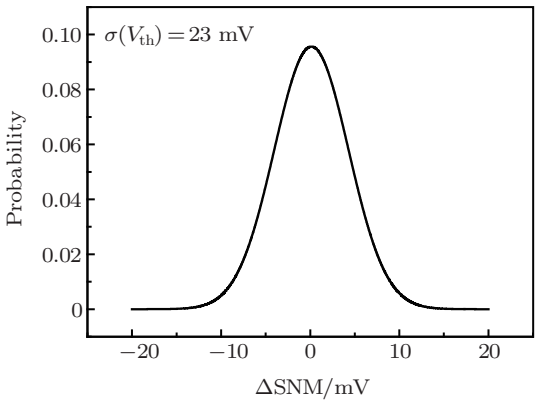



**Fig. 4.** Probability density function of ΔSNM determined by threshold variations of cell transistors. In the Monte Carlo run, 1000 samples are used.

### 4.2. Influence of OFF-state leakage on SNM

As discussed in the Introduction (Section 1), the OFF-state leakage of pull-down NMOS transistor, induced by radiation, is bias-dependent. The experimental test indicates that the device loading the inverse data pattern as irradiation has a larger standby current than loading the same data pattern, which was reported in Refs. [5] and [6]. We obtain the same result in our experiment, which is shown in Fig. 5. The standby current of the device increases as the dose increases, which mainly results from the OFF-state leakage of pull-down NMOS transistor. When the inverse data pattern as radiation is written into the device, the NMOS transistor biased to ON during radiation is turned off to the supply device's standby current. On the contrary, when the same data pattern is written into the device, the NMOS transistor is biased to OFF to stop supplying the device's standby current. Because of the larger OFF-state leakage of the NMOS transistor biased to ON, the device has a larger standby current loading the inverse data pattern as radiation. The bias-dependent OFF-state leakage of pull-down NMOS transistors has an influence on the noise margin of memory cells, and the trend of memory cell's write and read margin changing with radiation is discussed by Yao *et al*. in Ref. [5]. Experimental measurement and circuit simulation show that the write and read noise margins of data stored during radiation increase by radiation while, in contrast, the other data's write and read noise margins decrease. However, they did not analyze the dependence of cell's static noise margin on irradiation, which is directly proportional to cell's background data, which has been discussed in Subsection 4.1.

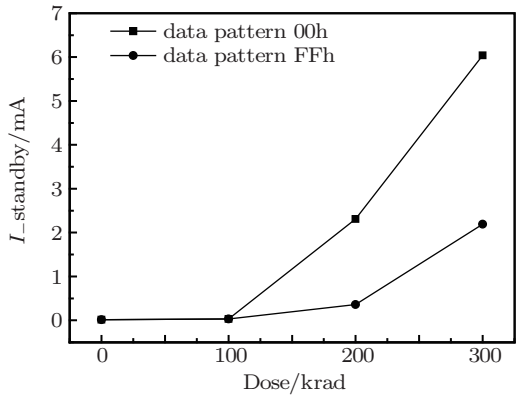



**Fig. 5.** Standby current of HM62V8100I loading the same and inverse data patterns as radiation, showing and device stores data pattern FFh during radiation.

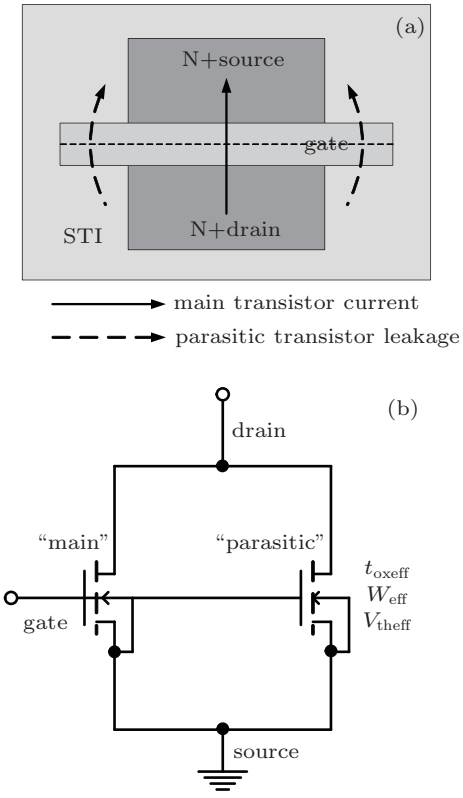



**Fig. 6.** (a) Leakage path of irradiated NMOS transistor, and (b) schematic plot of the circuit-level modeling of the parasitic NMOS transistor connected in parallel with main structure.

We can obtain the information about mechanism for pattern imprinting from the dependence of cell's static noise margin on radiation due to the SNM relating to background data. In order to obtain the dependence of the cell's static noise margin on radiation, we include OFF-state leakage induced by radiation in the NMOS transistor model of our simulation.

The primary cause for OFF-state leakage is the reduction in the threshold ($V_{\text{theff}}$) and the increase in drive current for the parasitic NMOS transistor associated with the edges of the main device shown in Fig. 6(a). Prior to radiation exposure, the leakage current of the parasitic device is low compared with that of the main transistor, owing to the relatively large effective gate oxide thickness ($t_{\text{oxeff}}$) and the small effective width ($W_{\text{eff}}$). Upon irradiation, the $t_{\text{ox}}^2$ dependence of the threshold voltage shift in the parasitic device and the increase in the drive current ultimately lead to a measurable OFF-state leakage current. This effect can be modeled as an additional NMOS transistor connected in parallel with the main transistor, which is illustrated in Fig. 6(b).[14]

By choosing $V_{\text{theff}}$, $t_{\text{oxeff}}$, and $W_{\text{eff}}$, we can obtain different OFF-state leakages in the NMOS transistor. Figure 7 shows the simulation result of the NMOS transistor, including leakage current from parasitic transistor, and it accords very well with experimental data for a deep sub-micron NMOS transistor.[15–18]

Through our experimental data for standby current of device loading inverse data pattern as radiation, we can make a conservative estimation for the unbalance between OFF-state leakages of two pull-down NMOS transistors: the total standby current of the device comes from the cell array, and is only contributed by OFF-state leakage of NMOS transistors biased to ON during radiation. Then, we can obtain the average value of OFF-state leakage for those NMOS transistors, dividing the device's standby current by the number of memory cells, as listed in Table 3. In the above estimation, the OFF-state leakage of NMOS transistor is larger than the true value because the transistors of the peripheral circuit also supply the standby current of the device. Due to the value being much smaller than ON bias, we ignore the OFF-state leakage of the NMOS transistor biased to OFF during radiation, and then obtain the conservative estimation of unbalance between OFF-state leakages of two pull-down NMOS transistors.

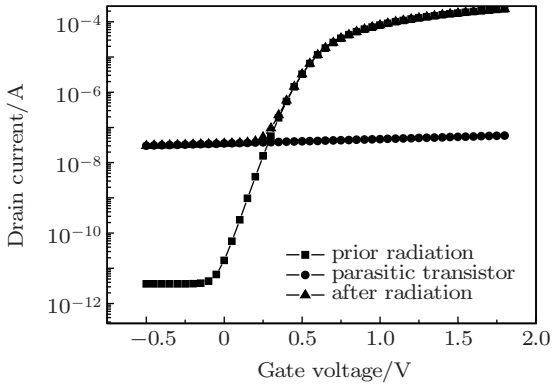



**Fig. 7.** Simulation result of NMOS transistor including leakage current from parasitic transistor.

**Table 3.** Conservative estimations for OFF-state leakages of NMOS transistors during radiation.

| Device ID | Dose/Gy | OFF-state leakage/nA | Percentage of pattern imprinting/% |
|---|---|---|---|
| IDT71V124 | 900 | 25.62 | 99.28% |
| IS61V5128AL | 1000 | 3.29 | 99.48% |
| HM62V8100I | 3000 | 0.6247 | 90% |
| HM62V16100I | 6000 | 0.5609 | 65.46% |

With the NMOS transistor model including OFF-state leakage induced by radiation, and the conservative estimation for the unbalance between OFF-state leakages of two pull-down NMOS transistors, we obtain the probability density functions of ΔSNM with different OFF-state leakages of NMOS transistor during radiation, as shown in Fig. 8. We assume that memory cells store data "1" (Q1, Q4 ON and Q2, Q3 OFF, seen in Fig. 1) during radiation in our simulation. The simulation result indicates that percentage of pattern imprinting, which equals the integral of Gaussian bell curve from zero to positive infinity and represents the percentage of memory cells with data "1" as background data, increases with increasing the OFF-state leakage of Q1, and when OFF-state leakage is 100 nA, the percentage of pattern imprinting is 59%. It is seen from Table 3 that the OFF-state leakage of NMOS transistor is less than 100 nA under conservative estimation, but the percentages of pattern imprinting of devices are mostly larger than 90%. However, under a conservative estimation the unbalance between OFF-state leakages of two pull-down NMOS transistors is not big enough to induce pattern imprinting. Through the above analysis, we conclude that the bias-dependent OFF-state leakage induced by total dose irradiation is not the reason for pattern imprinting on deep sub-micron SRAMs.

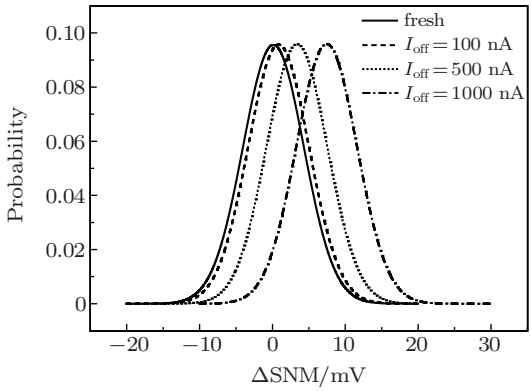



**Fig. 8.** Probability density functions of ΔSNM with different OFF-state leakages of Q1.

As discussed above, OFF-state leakage has only a weak

effect on the SNM of memory cell. Indeed, this is due to the strong drive ability of pull-up PMOS transistors, and it can compensate for the OFF-state leakage of NMOS transistor by only lowering a tiny output voltage; for example, this transistor provides 1-μA current by lowering down 10-mV output voltage.

### 4.3. Influence of RINCE on SNM

As discussed in the Introduction (Section 1), radiation can also induce threshold voltage shift in narrow-width channel MOS transistor fabricated by a deep sub-micron process, which is known as RINCE, and the threshold shift is bias-dependent. So, we should include RINCE in our irradiated transistor's model in order to analyze the influence of RINCE on memory cell's SNM and then determine whether it can induce pattern imprinting.

First of all, we only consider the influence of pull-down NMOS transistor. By assigning different values to the difference between pull-down NMOS transistors' thresholds and assuming memory cells store data "1" during radiation, we obtain the trend of ΔSNM changing with the threshold shift of pull-down NMOS transistor, as shown in Fig. 9. In Fig. 9, $\Delta V_{\rm th}$ represents difference between pull-down NMOS transistors' thresholds, which equals threshold of Q2 minus that of Q1 and has a positive value due to the bias effect of radiation. With the increase of $\Delta V_{\rm th}$, the Gaussian bell curve of ΔSNM gradually shifts to the positive side of coordinate axis representing ΔSNM. When $\Delta V_{\rm th}$ increases to 15 mV, the percentage of pattern imprinting is 99.87%.

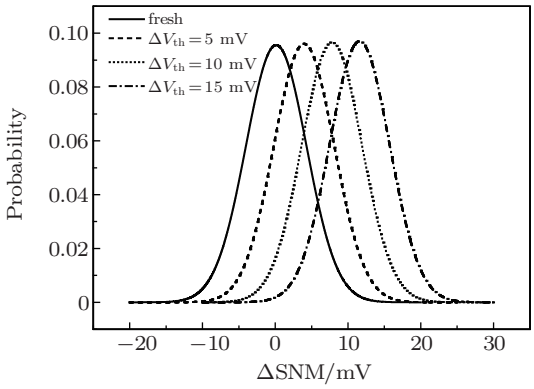



**Fig. 9.** Probability density functions of ΔSNM with different values of $\Delta V_{\rm th}$.

In order to explore the influence of difference between pull-up PMOS transistors' thresholds on ΔSNM, we include the threshold shift of the PMOS transistor in our simulation together with the NMOS transistor's threshold shift. Because the bias-dependence of the PMOS transistor is opposite to that of the NMOS transistor, and the threshold of PMOS transistors is negative, the difference between pull-up PMOS transistors' thresholds has the same sign (positive or negative) as the pull-down NMOS transistors'. The simulation results show that the difference between the pull-up PMOS transistors' thresholds moves the mean value of ΔSNM to the same direction as that between pull-down NMOS transistors thresholds, and their effect can be superposed as shown in Fig. 10. Thus, for both the pull-up PMOS transistors and the pull-down NMOS transistors, the RINCE-induced threshold shift also tends to induce pattern imprinting on deep sub-micron SRAMs, which is the same as micron devices.

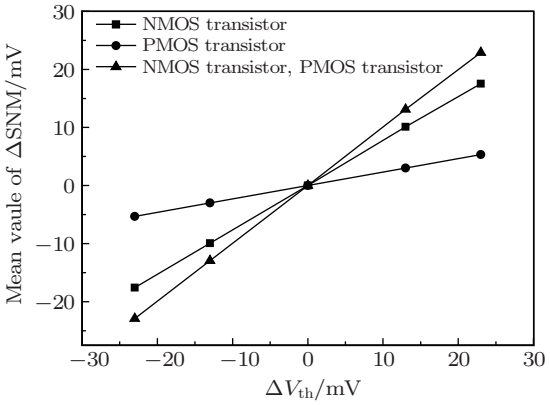



**Fig. 10.** Variations of the mean value of ΔSNM with difference between pull-down NMOS transistors' thresholds $\Delta V_{\rm th}$, where $\Delta V_{\rm th}$ equals the threshold of Q2 minus that of Q1, and for pull-up PMOS transistors, $\Delta V_{\rm th}$ equals the threshold of Q4 minus that of Q3. In simulation, both data "0" and "1" storing in memory cells during radiation are considered.

Although we cannot measure the thresholds of single transistor in commercial SRAMs before and after radiation, we can obtain a rough range of the shift of minimum-geometry transistor's threshold from the research papers about RINCE and our experiment on narrow width transistors.

In Ref. [4], Hu *et al*. studied the total dose effect on a 0.18-μm CMOS technology, their experimental result showed that at a dose level of 2000 Gy(Si), the threshold shift of NMOS transistor ($W/L = 0.22/10$) biased to ON during radiation is 40 mV. Federico and Giovanni also compared the threshold shifts of transistors with different $W/L$ ratios, which were manufactured by a 0.13-μm CMOS process, with the threshold shift of minimum-geometry NMOS transistor ($W/L = 0.16/0.12$) (40 mV after 1000 Gy(Si) of ON bias radiation).[9] In our experiment on a narrow width transistor manufactured by 0.18-μm CMOS process, NMOS transistor ($W/L = 0.22/0.18$) biased to ON has 50-mV threshold shift at a dose level of 4000 Gy(Si).[19,20] Furthermore, Marc *et al*.[10] and Gonella *et al*.[11] have discussed the influence of the bias condition on a RINCE-induced threshold shift, and their experimental data showed that for a NMOS transistor the threshold shift for the ON-bias condition is much larger than for the OFF-bias condition. For example, in Ref. [11], for an NMOS transistor ($W/L = 0.16/0.12$) fabricated by a 0.13-μm CMOS process, the ON-bias condition is 40 mV and OFF-bias condition is 10 mV at a dose level of 1000 Gy(Si). Based on the results presented above, we can conclude that $\Delta V_{\rm th}$ between

two pull-down NMOS transistors induced by irradiation can easily exceed 15 mV to induce pattern imprinting.

The threshold variation of the transistor is the reason why memory cells have a preferred state as their background data. Although neighboring cell transistors have the same mean value of threshold, the threshold mismatch between them, which is induced by intrinsic fluctuations, results in a preferred state in SRAM cells. Because the threshold mismatch is random, the distribution of background data pattern is typically random and is roughly equally divided between zeros and ones over the entire memory. Radiation shifts the threshold of the transistor, and the bias-dependence of the shift results in a difference between the mean values of threshold of neighboring cell transistors. When the difference increases to a level approaching the standard deviation of threshold variation, the threshold shift induced by irradiation will play a more prominent role in determining the cell's background data than the threshold variation that is induced by an intrinsic fluctuation. As a result, most of cells have the preferred state that the memory cell is in during irradiation.

## 5. Conclusion

Pattern imprinting in deep sub-micron SRAMs during total dose irradiation is investigated, and the mechanism of pattern imprinting is discussed in detail. Firstly, we built a relationship between the memory cell's SNM and the background data, showing that the probability density function of a ΔSNM can represent the background data pattern of the device very well. We then studied the influence of radiation on the probability density function of ΔSNM, to explore the reason of pattern imprinting. The results show that the bias-dependent OFF-state leakage of a pull-down NMOS transistor is not large enough to induce pattern imprinting. Due to the strong drive ability of pull-up PMOS transistors, OFF-state leakage has only a weak effect on the probability density function of ΔSNM. The simulation result indicates that pattern imprinting will take place when $\Delta V_{\rm th}$ between pull-down NMOS transistors is larger than 15 mV. Moreover, we demonstrate that the narrow channel width device $\Delta V_{\rm th}$ between pull-down NMOS transistors, induced by radiation, can easily exceed 15 mV to induce the pattern imprinting. We find that for micron and deep sub-micron devices, the mechanism of pattern imprinting is the bias-dependent threshold shift of the transistor, but the threshold shift of deep sub-micron device is induced by charge trapping in STI rather than gate oxide. Next, we plan to design two kinds of SRAMs, of which the memory cells are separately formed by usual narrow width transistors and wide width transistors, to check the influence of RINCE on the cell's SNM.

## Acknowledgments

The authors would like to thank the fellows of Key Laboratory of Functional Materials and Devices under Special Environments, Chinese Academy of Sciences, for their help and attention to this work. The authors also want to thank the fellows in The Xinjiang Technical Institute of Physics and Chemistry for making $^{60}$Co $\gamma$ ray available for all these radiation experiments.

## References

[1] John T S and Michael H Z 1987 *IEEE Trans. Nucl. Sci.* **34** 1404
[2] Daniel E H, Wayne P B and Kevin F 2008 *IEEE T Comput.* **57** 1198
[3] Oldham T R and McLean F B 2003 *IEEE Trans. Nucl. Sci.* **50** 483
[4] Hu Z Y, Liu Z L, Shao H, Zhang Z X, Ning B X, Chen M, Bi D W and Zou S C 2011 *IEEE Trans. Nucl. Sci.* **58** 1347
[5] Yao X Y, Nathan H, Lawrence T C, Keith E H, David R A and Walter M S 2008 *IEEE Trans. Nucl. Sci.* **55** 3280
[6] James A F, Paul E D, Marty R S, James R S and Gerald L H 2006 *IEEE Trans. Nucl. Sci.* **53** 3187
[7] Dhanya N, Richard G and TanjaKarp 2013 *IEEE Trans. Nucl. Sci.* **60** 2611
[8] Liu Z L, Hu Z Y, Zhang Z X, Shao H, Chen M, Bi D W, Ning B X and Zou S C 2011 *Chin. Phys. B* **20** 070701
[9] Federico F and Giovanni C 2005 *IEEE Trans. Nucl. Sci.* **52** 2413
[10] Marc G, Vincent G, Sylvain G, Martial M, Pierre M and Philippe P 2011 *IEEE Trans. Nucl. Sci.* **58** 2807
[11] Gonella L, Faccio F, Silvestri M, Gerardin S, Pantano D, Re V, Manghisoni M, Ratti F L and Ranieri A 2007 *Nucl. Instrum. Methods Phys. Res. A* **582** 750
[12] Azeez J B, Xinghai T and James D M 2001 *IEEE J. Solid-State Circuits* **36** 658
[13] Peter A S, Frans P W and Klaassen D B 1998 *IEEE Trans. Electron Dev.* **45** 1960
[14] Armin W and Julien Z 2005 *Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation Lecture Notes in Computer Science* **3728** 488
[15] Ivan S E, Hugh J B and Michael L A 2005 *IEEE Trans. Nucl. Sci.* **52** 2259
[16] Liu Z L, Hu Z Y, Zhang Z X, Shao H, Chen M, Bi D W, Ning B X and Zou S C 2011 *Nucl. Instrum. Methods Phys. Res. A* **644** 48
[17] Liu Z L, Hu Z Y, Zhang Z G, Shao H, Chen M, Bi D W, Ning B X and Zou S H 2011 *Microelectronics Reliability* **51** 1148
[18] Hu Z Y, Liu Z L, Shao H, Zhang Z G, Ning B X, Chen M, Bi D W and Zou S H 2011 *Microelectron. J.* **42** 883
[19] Cui J W 2012 "Research on Radiation and Reliability Effects of Ultra Deep Sub-micron CMOS Device for Space Application" (Ph. D. Dissertation) (Beijing: University of Chinese Academy of Sciences) (in Chinese)
[20] Cui J W, Yu X F, Ren D Y and Lu J 2012 *Acta Phys. Sin.* **61** 026102 (in Chinese)