Electrical and dielectric properties of Al/p-Si and Al/perylene/p-Si type diodes in a wide frequency range

Ahmet Kaya[a)†], Sedat Zeyrek[b)], Sait Eren San[c)], and Şmsettin Altındal[d)]

[a)] *Opticianry Department, Vocational School of Medical Sciences, Turgut Ozal University, Ankara* 06370, *Turkey*
[b)] *Physics Department, Faculty Sciences, Dumlupınar University, Kütahya* 43000, *Turkey*
[c)] *Physics Department, Gebze Institute of Technology, Kocaeli* 41400, *Turkey*
[d)] *Physics Department, Faculty of Sciences, Gazi University, Ankara* 06500, *Turkey*

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The perylene ($C_{20}H_{12}$) layer effect on the electrical and dielectric properties of Al/p-Si (MS) and Al/perylene/p-Si (MPS) diodes have been investigated and compared in the frequency range of 0.7 kHz–2 MHz. Experimental results show that C–V characteristics give an anomalous peak for two structures at low frequencies due to interface states (N_{ss}) and series resistance (R_s). The increases in C and G/ω at low frequencies confirm that the charges at interface can easily follow an ac signal and yield excess capacitance and conductance. The frequency-dependent dielectric constant (ε') and dielectric loss (ε'') are subtracted using C and G/ω data at 1.5 V. The ε' and ε'' values are found to be strongly dependent on frequency and voltage, and their large values at low frequencies can be attributed to the excess polarization coming from charges at traps. Plots of $\ln(\sigma_{ac})$–$\ln(\omega)$ for two structures have two linear regions, with slopes of 0.369 and 1.166 for MS, and of 0.077 and 1.061 for MPS, respectively. From the C^{-2}–V characteristics, the doping acceptor atom concentration (N_A) and barrier height (Φ_B) for Schottky barrier diodes (SBDs) of MS and MPS types are also obtained to be 1.484×10^{15} and 1.303×10^{15} cm^{-3}, and 1.10 and 1.13 eV, respectively.

Keywords: organic–inorganic based Schottky diodes, perylene ($C_{20}H_{12}$) interfacial layer, electrical and dielectric properties, frequency and voltage dependence

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1. Introduction

To prevent the interface diffusion and reaction between metal and semiconductor, an interfacial insulator or organic polymer layer such as SnO_2,[1] Si_3N_4,[2] TiO_2,[3,4] HfO_2,[5] PVA,[6] polyindole,[7] and perylene[8] layer at metal/semiconductor (MS) interface of a Schottky barrier diode (SBD), rather than conventional SiO_2, has recently captured considerable attention of researchers for device applications. It is well known that, unless specially fabricated in an MS-type SBD, a thin interfacial native insulator/oxide layer can be formed on a semiconductor surface between the metal and the semiconductor. Due to the existence of such interfacial layer at MS interface, MS-type SBDs are converted to metal-insulator/polymer-semiconductor (MIS or MPS) type SBDs. In this case, the applied voltage across the diode will be shared by the interfacial layer (V_i), the depletion layer (V_s), and series resistance (R_s).[9–15] On the other hand, the performance of these devices and their reliability depend on various parameters, such as interfacial insulator/polymer layer and its homogeneity and thickness, R_s, interface states (N_{ss}) localized at interfacial layer/semiconductor interface, the formation of barrier height at MS interface, frequency, and applied bias voltage.[9,10] Among them, R_s plays an important role both in electrical and dielectric properties, and arises from five different sources: (1) contact formed by the probe wire to the gate; (2) back contact of semiconductor; (3) impurities in semiconductor; (4) resistance of quasi-neutral bulk semiconductor; and (5) non-uniform doping distribution in the semiconductor.[10]

In the ideal case, the C–V and G/w–V characteristics are usually independent of frequency and exhibit an increase in capacitance with increasing applied voltage.[2,3,9–15] However, the situation is different especially at low frequencies between weak inverse and weak accumulation regions especially due to the contribution of carriers at N_{ss}, interfacial layer native or deposited. On the other hand, R_s is more effective especially in the strong accumulation region. Therefore, the forward bias C–V plots can reveal two distinct anomalous peaks in the depletion and accumulation regions, and the general consensus is that these peaks can be attributed to N_{ss} and R_s.[3,10,19] Organic materials have opened a new possibility of replacing conventional inorganic devices by the organic ones. Furthermore, many studies have been recently performed for the barrier height (BH) enhancement or modification using the thin organic interfacial layers.[6,16–18] Lee *et al.*[20] suggested that the decrease in leakage current, which means improvement in the diode quality, is related to the growth of interfacial layer and the reduction of oxygen vacancies.

In this study, to make comparison regarding the electrical and dielectric properties and ac electrical conductivity in an MS and an MPS SBD, Al/p-Si (MS) and Al/perylene/p-

†Corresponding author. E-mail: akaya@turgutozal.edu.tr

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Si (MPS) type SBDs are fabricated on the same wafer. The obtained experimental results of these SBDs have been compared in the wide frequency range of 0.7 kHz–2 MHz at room temperature by using admittance spectroscopy measurements. Observation of anomalous peaks in the depletion region especially at low frequencies is explained in terms of a continuous distribution of N_{ss} at MS interface.

2. Experimental procedures

Al/p-Si (MS) and Al/Perylene/p-Si (MPS) type Schottky barrier diodes were fabricated on p-type Si with (100) orientation, thickness of 280 μm, and resistivity of about 20 Ω·cm. Firstly, samples were ultrasonically cleaned in trichloroethylene and ethanol, etched by CP4 (HNO_3:HF:$COOHC_2H_5$:H_2O=3:1:2:2 weight ratio) solutions for 30 s, and then were rinsed by propylene glycol and blown dry with nitrogen gas. Secondly, the Si wafers were etched in a sequence of H_2SO_4 and H_2O_2 20% HF, a solution of $6HNO_3$:1HF:$35H_2O$, 20% HF, and finally rinsed in 18 MΩ·cm deionized water resistivity. Before the deposition of perylene ($C_{20}H_{12}$) on the Si wafers, to ensure the removal of any residual organics, Si wafers were heated up to 400 °C at a pressure of 10^{-8} Torr and sputter cleaned in pure argon ambient. Then, immediately after the Si wafers were transferred into the deposition chamber and high purity (99.999%) Al with about 2000 Å thickness was thermally evaporated onto the whole back side of the p-Si wafer at a pressure of $\sim 10^{-6}$ Torr in high vacuum pump system. To perform with low-resistivity ohmic contact, the sample was annealed at 400 °C.

In order to obtain metal-polymer-semiconductor (MPS) type SBDs, perylene ($C_{20}H_{12}$, polycyclic aromatic hydrocarbon) was solved in 1 M n-hagzane at 70 °C and coated on the front of p-Si wafer by using a spin coating system. The thickness of perylene was obtained from high-frequency (2 MHz) C–V plot at strong accumulation region by using interfacial layer capacitance ($C_i = \varepsilon_i \varepsilon_o A/d_i$). Finally, for two types of diodes, the front rectifier contacts with 1 mm diameter and 1500 Å thickness were formed by deposition of high-purity Al (99.999%) at 70 °C. In this way, both Al/p-Si (MS) and Al/$C_{20}H_{12}$/p-Si (MPS) type SBDs were fabricated on p-type Si wafer, the measurement system and the schematic diagram of the Al/$C_{20}H_{12}$/p-Si (MPS) type SBD are given in Fig. 1. The C–V and G/w–V measurements were carried out with an HP 4192 A LF impedance analyzer meter (5 Hz–13 MHz) in the frequency range of 0.7 kHz-2 MHz at room temperature. All measurements were carried out in dark with the help of a microcomputer through an IEEE-488 AC/DC converter card in the JANES-475 cryostat at about 10^{-3} Torr to avoid an external noise or other effects.

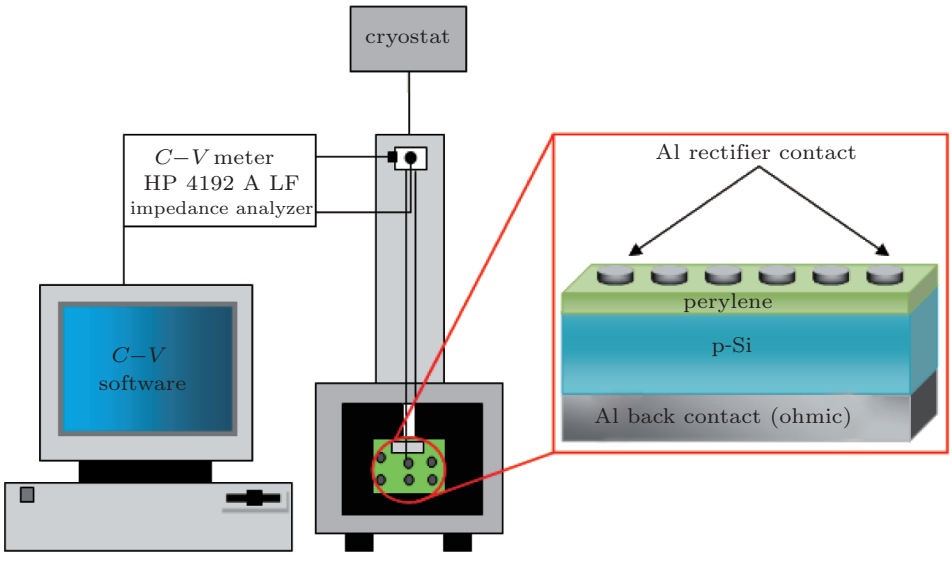


Fig. 1. (color online) Measurement system and schematic diagram of the Al/$C_{20}H_{12}$/p-Si (MPS) type SBD.

3. Results and discussion

The frequency-dependent forward and reverse bias (C–V) and (G/ω–V) measurements of MS and MPS type SBDs were carried out in the frequency range of 0.7 kHz–2 MHz at room temperature and given in Figs. 2(a), 2(b), 3(a), and 3(b). As can be seen in Figs. 2 and 3, the measured capacitance (C_m) and conductance (G_m/ω) are strongly dependent on frequency especially in depletion and accumulation regions. The splitting in C–V and G/ω–V plots in depletion region especially at low frequencies for both SBDs can be attributed to the ex-

istence of N_{ss}. On the other hand, the splitting in C–V plots in accumulation region especially at high frequencies can be attributed to the value of R_s and its magnitude. The other important feature of C–V plots for both SBDs is the unexpected forward bias C–V peaks. Such an anomalous peak is attributed to a particular density distribution of N_{ss}, R_s, and the interfacial polymer layer. The peak position of C_m–V plots shifts towards the negative bias region due to existence of N_{ss} which is in equilibrium with semiconductor and its restructure and reordering under applied bias effect. Similarly, figures 2(b) and 3(b) show the variation in the measured conductance (G_m/ω–V) plots both in the forward and reverse bias regions for the same frequency interval such that G_m/ω–V plots show similar behavior with frequency as C–V plots. The splitting in the C–V and G/ω–V plots, especially at low frequencies in the depletion region, can also be attributed to the existence of N_{ss} and their different carrier life time (τ). It is well known that at high frequencies (the carrier life time τ is much larger than $1/2\pi f$), the charges at interface cannot follow an ac signal contrary to low frequencies.[9,10]

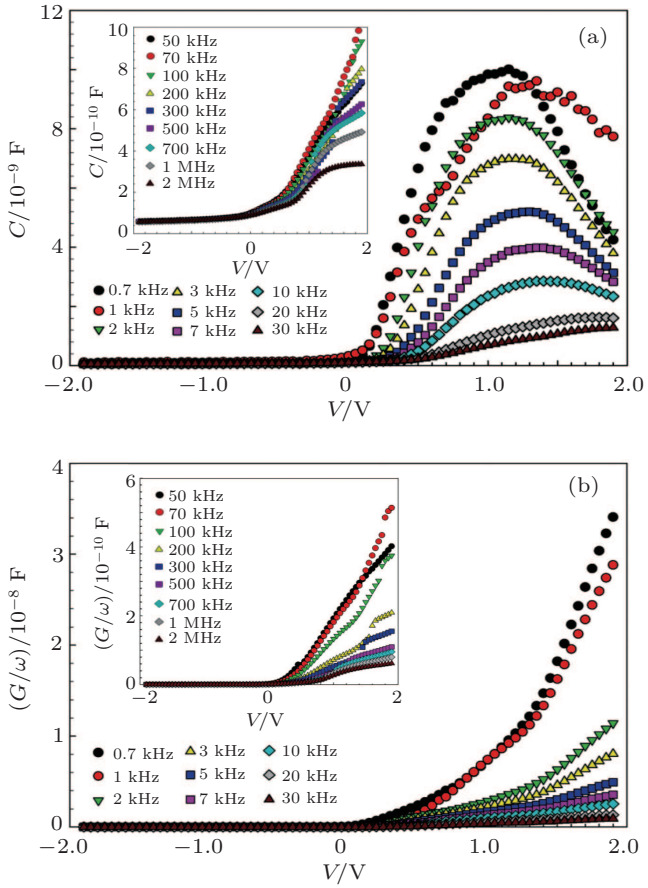


Fig. 2. (color online) Frequency-dependent plots of (a) C–V and (b) G/ω–V characteristics of the Al/p-Si (MS) SBD at room temperature.

In order to see the change in capacitance and conductance with frequency at the accumulation region (at 1.5 V), C–f and G/ω–f plots are provided for both SBDs in Figs. 4(a) and 4(b), respectively. As can been seen in Figs. 4(a) and 4(b), C and G/ω both decrease with increasing frequency, whereas the change in the values of C and G/ω are fairly high at low frequencies rather than high frequencies. Decrease in C and G/ω at high frequencies are due to the fact that the carrier life time τ is much larger than the inverse of angular frequencies ($\tau = 1/2\pi f$), and the charges at interface cannot follow an ac signal.[10] In addition, the change in C and G/ω with frequency for MS-type SBD is higher than MPS-type SBD.

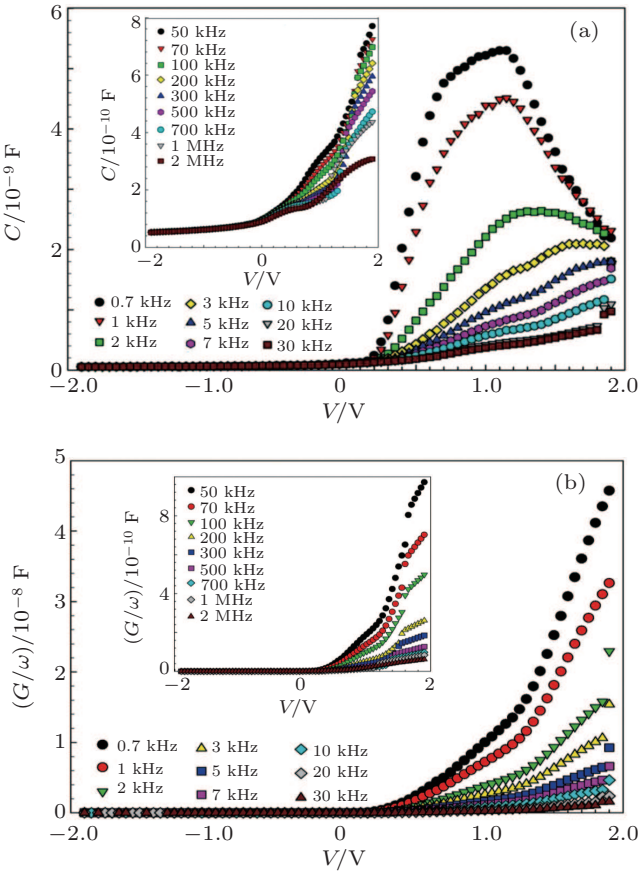


Fig. 3. (color online) Frequency-dependent plots of (a) C–V and (b) G/ω–V characteristics of the Al/Perylene/p-Si (MPS) SBD at room temperature.

Another important parameter is the series resistance (R_s) of diode, and it may cause serious errors in the C–V and G/ω–V characteristics especially in the accumulation region. However, this error can be minimized by adjusting the measured capacitance (C_m) and conductance (G_m/ω) values, with the R_s effect taken into account.[1–5,10] In this study, we use the technique developed by Nicollian and Brews.[10] Thus, the real value of R_s for the MIS, MPS, or MOS structures can be subtracted from the measured C_m and G_m values in the strong accumulation region at sufficiently high frequencies ($f \geq 0.5$ MHz) by using the following equation:[10]

$$R_s = \frac{G_m}{G_m^2 + (\omega C_m)^2}. \quad (1)$$

At the same time, voltage dependence of R_s can be also obtained from any measured C and G values for various applied bias voltages. Usually, the error in the measured C_m and G_m

occurs in the accumulation region rather than the depletion region. Therefore, the voltage-dependent R_s values obtained by Eq. (1) for MS-type and MPS-type SBDs are given in Fig. 5 for 2 MHz. It is expected that the value of resistance increases from the accumulation region to the inversion region. However, the R_i–V plots for two diodes exhibit a peak at about −1 V due to the particular distribution of surface states.

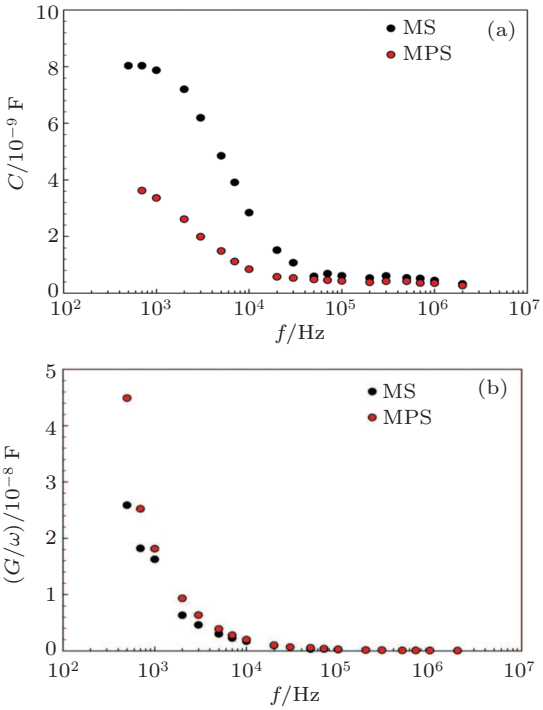


Fig. 4. (color online) Frequency dependence of (a) C–f and (b) G/ω–f plots at 1.5 V for the MS-type and MPS-type SBDs, respectively.

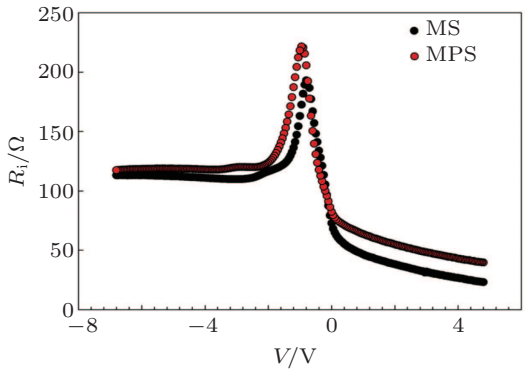


Fig. 5. (color online) Voltage-dependent resistance of Al/p-Si (MS) and Al/Perylene/p-Si (MPS) SBDs at 2 MHz and room temperature.

Some main electrical parameters such as diffusion potential (V_D), Fermi energy level (E_F), doping concentration (N_A), width of the depletion region (W_D), and barrier height (Φ_B) are extracted from the reverse bias C^{-2}–V plots for MS-type and MPS-type SBDs. In order to minimize the contribution of N_{ss}, C^{-2}–V plots are obtained for 2 MHz. Because at this sufficiently high frequency, the charges at interface cannot follow an external ac signal, the contribution of N_{ss} to the total capacitance can be neglected.[10,17,20–24] The C^{-2}–V plots for the MS-type and MPS-type SBDs are given in Fig. 6. As can be seen from this figure, C^{-2}–V plots for two types of SBDs have a linear region.

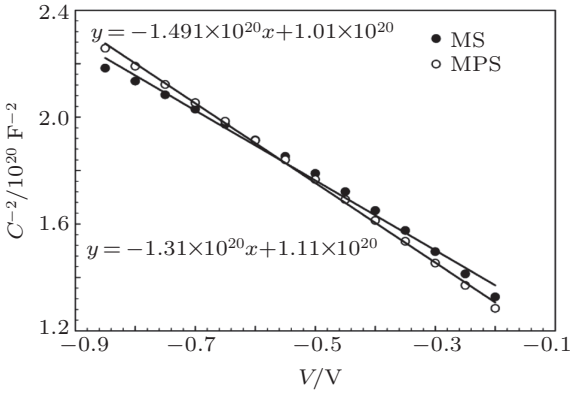


Fig. 6. C^{-2} versus voltage at 2 MHz for MS-type and MPS-type SBDs at room temperature.

The measured depletion capacitance for MS-, MIS-, or MPS-type SBDs can be expressed as[9]

$$\frac{1}{C^2}=\frac{2(V_R+V_0)}{q\varepsilon_s\varepsilon_o N_A A^2}, \tag{2}$$

where A, V_R, V_0, N_A, ε_s, and ε_o are the diode area, the reverse bias voltage, the built-in voltage at zero-bias, the acceptor density, the dielectric permittivity of semiconductor, and the permittivity of vacuum, respectively. The value of N_A is obtained from the slope of the linear part of C^{-2}–V plots (see Fig. 6) for 2 MHz. The value of barrier height Φ_B at the MS interface is calculated for both SBDs by using the voltage intercept V_0 of the C^{-2}–V plots, the Fermi energy level (E_F), and the thermal energy as[9]

$$\phi_B=\left(V_0+\frac{kT}{q}\right)+\frac{kT}{q}\ln\left(\frac{N_V}{N_A}\right)=V_D+E_F. \tag{3}$$

Here, the value of E_F is obtained by using the effective density of states in Si valance band and N_A values.[1–4,9] The obtained N_A, V_D, E_F, and Φ_B values for MS-type and MPS-type SBDs are obtained to be 1.484×10^{15} and 1.303×10^{15} cm^{-3}, 0.872 and 0.876 eV, 0.228 and 0.232 eV, 1.10 and 1.13 eV, respectively. These values are in agreement with reference values, and there is not important discrepancy between MS-type and MPS-type SBDs. Because the linear part of C^{-2}–V plots corresponds to the inverse region, both R_s and N_{ss} values are not effective on C–V plots.

Using the frequency-dependent C–V and G–V plots in the frequency range of 0.7 kHz–2 MHz, the frequency-dependent dielectric constant (ε') and dielectric loss (ε'') values are also obtained from the following equations at accumulation region for 1.5 V (see Figs. 7(a) and 7(b)):[9]

$$\varepsilon'=\frac{C_m}{C_0},\quad \varepsilon''=\frac{G}{\omega C_o}, \tag{4}$$

where ε' and ε'' are the real and imaginary parts of complex permittivity. As can be seen in these figures, ε' and ε'' both decrease with increasing frequency exponentially. For the low frequencies, there is a considerable discrepancy regarding the values of ε' and ε''. Such behavior of ε' and ε'' may arise from the nature of SiO_2, PVA, and its thickness and homogeneity. The dispersion in low frequencies can be attributed to the interfacial polarization and the majority of interfaces.[25] In the low-frequency range, there is a contribution to conductivity from interfacial polarization and the charges at interfaces. Similar results are obtained for different materials.[26–28] The decreasing values of dielectric constant with increasing frequency can be attributed to the Maxwell–Wagner formulas,[29] space charge polarization,[30] and surface charges.[27,28] Contrary to low frequencies at high frequencies, the contributions of the interfacial, dipolar, or ionic polarization become ineffective. Because the interfacial dipoles have less time to orient themselves in the direction of the alternating field.[31,32] The dielectric dispersion at low frequencies is also observed in Refs. [25]–[36].

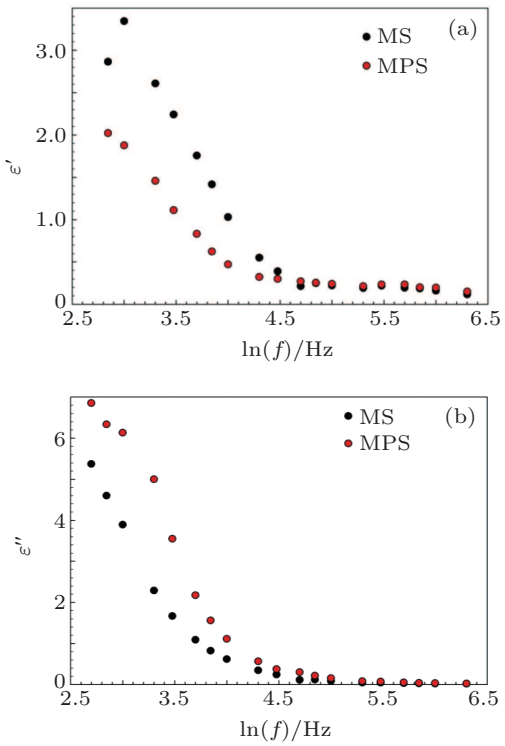


Fig. 7. (color online) Frequency dependence of (a) ε' and (b) ε'' at 1.5 V for MS-type and MPS-type SBDs at room temperature.

In addition, the σ_{ac}–ln(w) plot for MS-type and MPS-type diodes are given in Fig. 8(a). As shown in this figure, the value of σ_{ac} increases with increasing frequency exponentially. This increase in σ_{ac} with increasing frequency can be attributed to a gradual decrease in series resistance with increasing frequency.[31] Similar behavior is also observed in Refs. [31] and [37]–[40]. Frequency dependent of the ac conductivity (σ_{ac}) shows hopping-type conduction mechanism. The increases in σ_{ac} with increasing frequency show that it must be related to the bound carriers trapped in interface states/traps.[41] Such behavior of ε', ε'', and σ_{ac} values are typical for this structure and can be ascribed to the space charge polarization.[30] As the frequency decreases, more and more charge accumulation occurs at interfacial layer–semiconductor interface, which leads to a drop in the conductivity at low frequency.[1] Hopping of carries from trap to trap situated in the band gap of the material may give rise to frequency-dependent ac conductivity and can be expressed as[41,42]

$$\sigma_{ac} = \sigma(0) + A\omega^s, \tag{5}$$

where σ_{ac} is independent of frequency at low frequencies, s is a constant ($0 < s < 1$), A is a constant of proportionality, and $\omega = 2\pi f$ is the angular frequency. As can be seen in Fig. 8, the ln(σ_{ac})–ln(ω) plots for both SBDs have two distinct linear regions with different slopes. Such behavior of these plots confirms that two different conduction mechanisms correspond to the low-frequency and high-frequency regions. Such frequency-dependent behavior of σ_{ac} can be expressed as

$$\sigma_{ac} = \sigma(0) + A\omega^{s_1} + A\omega^{s_2}, \tag{6}$$

where the first term dominates especially at low or moderate frequencies, corresponding to hopping motion ($0 < s_1 < 1$).

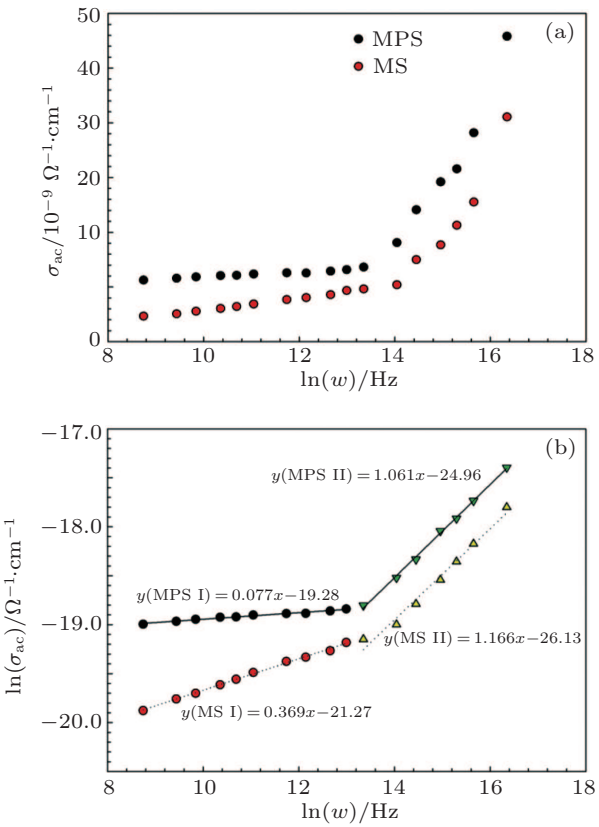


Fig. 8. (color online) The ln(ω) dependence of (a) σ_{ac} and (b) ln(σ_{ac}) at 1.5 V for MS-type and MPS-type SBDs at room temperature.

The second term dominates only at high frequencies and corresponding well-localized hopping and has values in the range of $1 < s_2 < 2$.[42,43] It is clear from Fig. 8 that the $\ln(\sigma_{ac})$–$\ln(\omega)$ plots for MS-type and MPS-type SBDs have two distinct linear regions denoted as I and II, with slopes of 0.369 and 0.077, 1.166 and 1.061, respectively. These results show that the value of s in two regions for MS is greater than MPS. It is clear that the SBD with perylene has low ac resistivity (ρ_{ac}) or high ac conductivity (σ_{ac}) values in the whole frequency range considered, and these values are suitable MS-type and MPS-type SBDs. As a result, the dielectric properties are improved due to the interfacial perylene layer effect.

4. Conclusions

Frequency-dependent electrical, dielectric properties, and ac electrical conductivity of MS-type and MPS-type SBDs have been investigated in the frequency range from 0.7 kHz to 2 MHz at room temperature and compared to study the effect of interfacial perylene ($C_{20}H_{12}$) layer. The increase in C and G/w at low frequencies shows that the charges at various interface/trap levels can easily follow an external ac signal and yield an excess capacitance (C_{ex}) and conductance (G_{ex}/w) to the measured C and G/w values. Other important features of the forward bias capacitance–voltage (C–V) characteristics plots show an anomalous peak for both structures especially at low frequencies due to a continuous distribution of interface states (N_{ss}) and series resistance (R_s) of structures. The frequency-dependence profile of dielectric constant (ε') and dielectric loss (ε'') of perylene are subtracted by using C and G/w data for a constant value of voltage (1.5 V) at accumulation layer and these values are found to be strongly dependent on frequency and applied dc bias voltages. The high values of ε' and ε'' at low frequencies can be attributed to the excess polarization coming from charges localized at the interface state or traps. The $\ln(\sigma_{ac})$–$\ln(\omega)$ plots for both MS-type and MPS-type SBDs are drawn and they have two distinct linear regions (I and II), with slopes of 0.369 and 1.166 for MS, and 0.077 and 1.061 for MPS, respectively. In addition, the concentration of acceptor atoms (N_A)and barrier height (Φ_B) values for MS-type and MPS-type SBDs are obtained from the C^{-2}–V characteristics (for 2 MHz) as 1.484×10^{15} and 1.303×10^{15} cm^{-3}, and 1.10 and 1.13 eV, respectively. In the light of obtained results, it can be seen that the electrical and dielectric properties of the MS-type diodes can be improved by the use of an interfacial perylene layer.

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