Quasi-two-dimensional threshold voltage model for junctionless cylindrical surrounding gate metal-oxide-semiconductor field-effect transistor with dual-material gate*

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(Received 24 April 2013; revised manuscript received 17 June 2013; published 3 December 2013)

Based on the quasi-two-dimensional (2D) solution of Poisson's equation in two continuous channel regions, an analytical threshold voltage model for short-channel junctionless dual-material cylindrical surrounding-gate (JLDMCSG) metal-oxide-semiconductor field-effect transistor (MOSFET) is developed. Using the derived model, channel potential distribution, horizontal electrical field distribution, and threshold voltage roll-off of JLDMCSG MOSFET are investigated. Compared with junctionless single-material CSG (JLSGCSG) MOSFET, JLDMCSG MOSFET can effectively suppress short-channel effects and simultaneously improve carrier transport efficiency. It is also revealed that threshold voltage roll-off of JLDMCSG can be significantly reduced by adopting both a small oxide thickness and a small silicon channel radius. The model is verified by comparing its calculated results with that obtained from three-dimensional (3D) numerical device simulator ISE.

Keywords: junctionless device, surrounding-gate MOSFET, dual-material gate, analytical model

PACS: 85.30.De, 73.40.Qv, 02.60.Cb **DOI:** 10.1088/1674-1056/23/1/018501

1. Introduction

Due to superior gate controllability, the cylindrical surrounding-gate (CSG) metal-oxide-semiconductor field-effect transistor (MOSFET) has been regarded as one of the most promising devices to extend the scaling limit of CMOS technology.[1–3] However, the formation of the abrupt source and drain junctions in the conventional CSG MOSFET imposes several challenges on doping techniques and thermal budget.[4] In order to alleviate these problems, the junctionless (JL) MOSFET has been proposed recently.[5–8] JL MOSFET includes source, drain, and channel regions with the same doping type and uniform high doping concentration. For this reason, JL MOSFET demands simpler fabrication processes than the conventional inversion mode MOSFET. However, the high doping concentration in the channel reduces carrier mobility, leading to degradation of transconductance of JL MOSFET.[4,9,10] In order to improve the carrier transport efficiency and transconductance of junctionless cylindrical surrounding-gate (JLCSG) MOSFET, a new structure called junctionless dual-material cylindrical surrounding gate (JLDMCSG) MOSFET has been proposed and its electrical characteristic has been investigated by using two-dimensional (3D) numerical simulations.[11] For the future use of this JLDMCSG MOSFET in integrated circuits, it is necessary to develop the physics-based analytical model for JLDMCSG MOSFET. Although several previously published literatures have reported analytical models for JLCSG MOSFET,[5,12,13] no analytical model for JLDMCSG MOSFET has been proposed until now.

In this paper, analytical threshold voltage model for JLDMCSG MOSFET is developed based on the quasi-two-dimensional (2D) channel potential approach. Using this analytical model, channel central potential distribution, electric field distribution, and threshold voltage roll-off of JLDMCSG MOSFET are calculated to demonstrate its characteristics. The model is verified by comparing its results with simulated results obtained from the 3D numerical device simulator ISE.

2. Model derivation

A 3D schematic view and a cross section along the channel direction of the JLDMCSG MOSFET are shown in Fig. 1. Considering the gate structure, the channel can be divided into two parts. The lengths of the two metals M_1 and M_2 are L_1 and L_2, respectively. Owing to the cylindrical symmetry of the device structure, a cylindrical coordinate system is employed, which consists of a radial direction r and a horizontal direction z (angular component is not shown in the figure). The symmetry of the structure ensures that the potential and the electric field have no variation with the angular in plane of the radial direction. Hence, a 2D analysis is sufficient.

*Project supported by the National Natural Science Foundation of China (Grant Nos. 61204092 and 61076101) and the Fundamental Research Funds for the Central Universities of Ministry of Education of China (Grant No. K50511250001).

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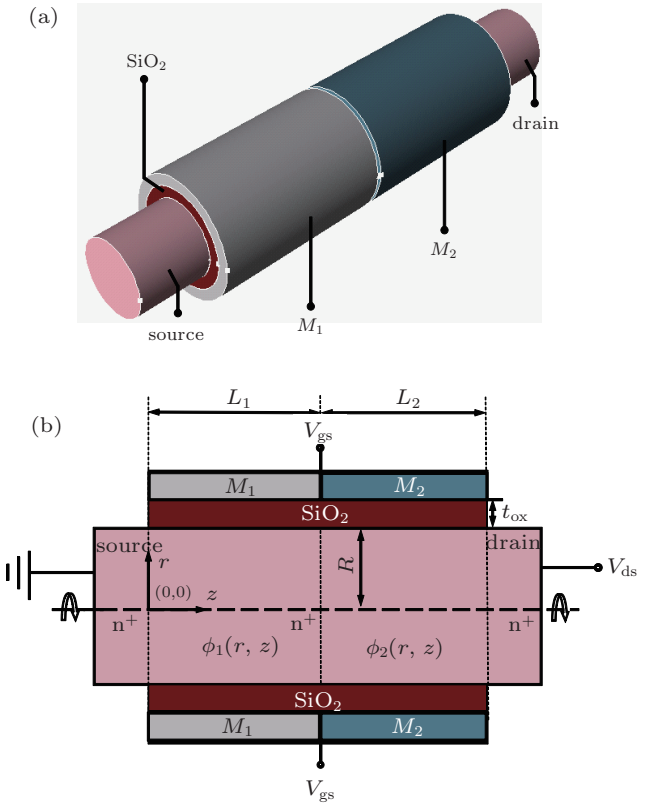


Fig. 1. (color online) Structure of JLDMCSG: (a) 3D schematic view; (b) cross-sectional view.

2.1. Potential model

The surface electrostatic potential and electric field distribution in the silicon can be derived by solving 2D Poisson's equation. Assuming that the influence of charge carriers and fixed charges on electrostatics of the channel can be ignored, the silicon channel is fully depleted when JLDMCSG MOSFET is operated under subthreshold region. Then, the electrostatic potential in two regions of the channel can be written as

$$\begin{aligned}&\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial}{\partial r}\Phi_1(r,z)\right)+\frac{\partial^2}{\partial z^2}\Phi_1(r,z)\\&=\frac{-qN_{\rm d}}{\varepsilon_{\rm Si}},\quad 0\le z\le L_1,\ \ 0\le r\le R,\end{aligned}\tag{1}$$

$$\begin{aligned}&\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial}{\partial r}\Phi_2(r,z)\right)+\frac{\partial^2}{\partial z^2}\Phi_2(r,z)\\&=\frac{-qN_{\rm d}}{\varepsilon_{\rm Si}},\quad L_1\le z\le L,\ \ 0\le r\le R.\end{aligned}\tag{2}$$

where q is the unit charge, $N_{\rm d}$ is the uniform channel doping concentration, $\varepsilon_{\rm Si}$ is the dielectric constant of silicon film, and $L=L_1+L_2$ is the total gate length. By using the parabolic approach, the 2D potential vertical to the channel direction can be assumed as

$$\Phi_j(r,z)=C_1^{(j)}(z)+C_2^{(j)}(z)\,r+C_3^{(j)}(z)\,r^2,\quad j=1,2.\tag{3}$$

In JLDMCSG MOSFET, the electric field in the center of the silicon channel is zero by symmetry

$$\left.\frac{\partial\Phi_j(r,z)}{\partial r}\right|_{r=0}=0,\quad j=1,2,\tag{4}$$

and the electric flux at the interface between the gate dielectric and the silicon channel is continuous

$$\begin{aligned}\varepsilon_{\rm Si}\left.\frac{\partial\Phi_j(r,z)}{\partial r}\right|_{r=R}&=\frac{\varepsilon_{\rm ox}}{t'_{\rm ox}}\left[V_{\rm gs}-\phi_{\rm MS}^{(j)}-\Phi_j(r=R,z)\right],\\&j=1,2,\end{aligned}\tag{5}$$

where $t'_{\rm ox}=R\ln(1+t_{\rm ox}/R)$ is the equivalent oxide thickness.[14] The work function differences are given as

$$\phi_{\rm MS}^{(j)}=\phi_{\rm M}^{(j)}-\phi_{\rm Si},\quad j=1,2,\tag{6}$$

in which, $\phi_{\rm M}^{(j)}$ is the metal work functions of M_1 and M_2 respectively, $\phi_{\rm Si}$ is the silicon work function and can be written as

$$\phi_{\rm Si}=\chi_{\rm Si}+\frac{E_{\rm g}}{2q}-\phi_{\rm F},\tag{7}$$

where

$$\phi_{\rm F}=\frac{kT}{q}\ln\left(\frac{N_{\rm d}}{n_{\rm i}}\right)\tag{8}$$

is the bulk potential, $E_{\rm g}$ is the silicon band gap, $\chi_{\rm Si}$ is the electron affinity, and $n_{\rm i}$ is the intrinsic carrier concentration. From Eqs. (3)–(5), the channel potential can be obtained as

$$\begin{aligned}\Phi_j(r,z)&=\Phi_{\rm C}^{(j)}(z)+\frac{C_{\rm ox}\left(V_{\rm gs}-\phi_{\rm MS}^{(j)}-\Phi_{\rm S}^{(j)}(z)\right)}{\varepsilon_{\rm Si}t_{\rm Si}}r^2,\\&j=1,2,\end{aligned}\tag{9}$$

where $\Phi_{\rm C}^{(j)}(z)$ and $\Phi_{\rm S}^{(j)}(z)$ are the central and surface potential for region j, which should satisfy the following equation:

$$\begin{aligned}\Phi_{\rm S}^{(j)}(z)&=\Phi_{\rm C}^{(j)}(z)+\frac{C_{\rm ox}t_{\rm Si}\left(V_{\rm gs}-\phi_{\rm MS}^{(j)}-\Phi_{\rm S}^{(j)}\right)}{4\varepsilon_{\rm Si}},\\&j=1,2.\end{aligned}\tag{10}$$

By substituting Eqs. (9) and (10) into Eqs. (1) and (2) and eliminating the surface potential, the differential equation for $\Phi_{\rm C}^{(j)}(z)$ can be expressed as

$$\frac{{\rm d}^2\Phi_{\rm C}^{(j)}(z)}{{\rm d}z^2}-\frac{1}{\lambda^2}\left(\Phi_{\rm C}^{(j)}(z)-\phi_{\rm C}^{(j)}\right)=0,\quad j=1,2,\tag{11}$$

where $\Phi_{\rm C}^{(j)}(z)$ is the long-channel central potential for region 1 and λ is the scaling length

$$\frac{1}{\lambda^2}=\frac{16C_{\rm ox}}{4t_{\rm Si}\varepsilon_{\rm Si}+C_{\rm ox}t_{\rm Si}^2},\tag{12}$$

$$\phi_{\rm C}^{(j)}=V_{\rm gs}-\phi_{\rm MS}^{(j)}+\frac{qN_{\rm d}t_{\rm Si}}{4C_{\rm ox}}+\frac{qN_{\rm d}t_{\rm Si}^2}{16\varepsilon_{\rm Si}},\quad j=1,2.\tag{13}$$

The general solution of the ordinary differential equation in Eq. (11) can be found as

$$\Phi_{\mathrm{C}}^{(j)}(z) = a_j \mathrm{e}^{z/\lambda} + b_j \mathrm{e}^{-z/\lambda} + \phi_{\mathrm{C}}^{(j)}, \quad j = 1,2, \tag{14}$$

where a_j and b_j are determined by the following boundary conditions.

(i) The potential at the source end is

$$\Phi_{\mathrm{C}}^{(1)}(z=0) = 0. \tag{15}$$

(ii) The potential at the drain end is

$$\Phi_{\mathrm{C}}^{(2)}(z=L) = V_{\mathrm{ds}}. \tag{16}$$

(iii) The electrostatic potential at the interface of the two regions is continuous

$$\Phi_{\mathrm{C}}^{(1)}(z=L_1) = \Phi_{\mathrm{C}}^{(2)}(z=L_1). \tag{17}$$

(iv) The lateral electric field at the interface of the three regions is continuous

$$\left.\frac{\mathrm{d}\Phi_{\mathrm{C}}^{(1)}(z)}{\mathrm{d}z}\right|_{z=L_1} = \left.\frac{\mathrm{d}\Phi_{\mathrm{C}}^{(2)}(z)}{\mathrm{d}z}\right|_{z=L_1}. \tag{18}$$

With those boundary conditions a_j and b_j can be solved as

$$a_1 = \frac{V_{\mathrm{ds}} - \phi_{\mathrm{C}}^{(2)} + \phi_{\mathrm{C}}^{(1)} \mathrm{e}^{-L/\lambda} + \left(\phi_{\mathrm{MS}}^{(1)} - \phi_{\mathrm{MS}}^{(2)}\right)\cosh(L_2/\lambda)}{2\sinh(L/\lambda)}, \tag{19}$$

$$a_2 = \frac{V_{\mathrm{ds}} - \phi_{\mathrm{C}}^{(2)} + \phi_{\mathrm{C}}^{(1)} \mathrm{e}^{-L/\lambda} + \left(\phi_{\mathrm{MS}}^{(1)} - \phi_{\mathrm{MS}}^{(2)}\right)\cosh(L_1/\lambda)\,\mathrm{e}^{-L/\lambda}}{2\sinh(L/\lambda)}, \tag{20}$$

$$b_1 = \frac{-V_{\mathrm{ds}} + \phi_{\mathrm{C}}^{(2)} - \phi_{\mathrm{C}}^{(1)} \mathrm{e}^{L/\lambda} - \left(\phi_{\mathrm{MS}}^{(1)} - \phi_{\mathrm{MS}}^{(2)}\right)\cosh(L_2/\lambda)}{2\sinh(L/\lambda)}, \tag{21}$$

$$b_2 = \frac{-V_{\mathrm{ds}} + \phi_{\mathrm{C}}^{(2)} - \phi_{\mathrm{C}}^{(1)} \mathrm{e}^{L/\lambda} - \left(\phi_{\mathrm{MS}}^{(1)} - \phi_{\mathrm{MS}}^{(2)}\right)\cosh(L_1/\lambda)\,\mathrm{e}^{L/\lambda}}{2\sinh(L/\lambda)}. \tag{22}$$

2.2. Threshold voltage model

For JLDMCSG, the channel under the gate M_1 will not conduct until the channel under the gate M_2 is turned on. This implies that the threshold behavior is mainly controlled by the gate M_1, which has the larger work function. The minimum central potential in region 1 can be found as

$$\Phi_{\mathrm{C}}^{(1)} = 2\sqrt{a_1 b_1} + \phi_{\mathrm{C}}^{(1)}. \tag{23}$$

By setting minimum central potential to be zero and solving for the gate bias of V_{gs} , one can obtain the short-channel threshold voltage for the JLDMCSG MOSFET as

$$V_{\mathrm{th}} = \frac{\left[-(2\alpha\kappa + 2\gamma\beta + \omega_1) + \sqrt{(2\alpha\kappa + 2\gamma\beta + \omega_1)^2 - (4\alpha\gamma - 1)(4\beta\kappa - \omega_1^2)}\right]}{(4\alpha\gamma - 1)}, \tag{24}$$

where

$$\alpha = \frac{\left(\mathrm{e}^{-L/\lambda} - 1\right)}{2\sinh(L/\lambda)}, \tag{25}$$

$$\beta = \frac{V_{\mathrm{ds}} + \omega_2 - \omega_1 \mathrm{e}^{-L/\lambda} + \left(\phi_{\mathrm{MS}}^{(1)} - \phi_{\mathrm{MS}}^{(2)}\right)\cosh(L_2/\lambda)}{2\sinh(L/\lambda)}, \tag{26}$$

$$\gamma = \frac{\left(1 - \mathrm{e}^{L/\lambda}\right)}{2\sinh(L/\lambda)}, \tag{27}$$

$$\kappa = \frac{-V_{\mathrm{ds}} - \omega_2 + \omega_1 \mathrm{e}^{L/\lambda} - \left(\phi_{\mathrm{MS}}^{(1)} - \phi_{\mathrm{MS}}^{(2)}\right)\cosh(L_2/\lambda)}{2\sinh(L/\lambda)}, \tag{28}$$

$$\omega_j = \phi_{\mathrm{MS}}^{(j)} - \frac{qN_{\mathrm{d}}t_{\mathrm{Si}}}{4C_{\mathrm{ox}}} - \frac{qN_{\mathrm{d}}t_{\mathrm{Si}}^2}{16\varepsilon_{\mathrm{Si}}}. \tag{29}$$

3. Results and discussion

Using the derived analytical models, the performance of JLDMCSG MOSFET is examined in terms of channel central potential distribution, channel central electric field distribution, carrier transport efficiency, and threshold voltage roll-off. To verify the analytical model, the 3D device simulator ISE is employed to simulate the device characteristics. ISE is a multi-dimensional, electro-thermal, mixed-mode device, and circuit simulator for one-dimensional (1D), 2D, and 3D semiconductor devices. It incorporates advanced physical models and robust numeric methods for the simulation of most types of semiconductor devices ranging from very deep submicron sil-

icon MOSFET to large bipolar power structures. Unless otherwise stated, the channel doping concentration $N_d = 10^{19}$ cm^{-3}, and the work function of M_1 and M_2 are 4.97 eV and 4.27 eV respectively. In Fig. 2, the central potential is plotted against distance from source for JLSMCSG and JLDMCSG with different ratios of L_1 and L_2. It is shown that there exists a step in channel central potential of JLDMCSG. This step potential ensures better screening of the channel region near the source from drain voltage of JLDMCSG.[3] In addition, good agreement between the results of our model and those of ISE is obtained.

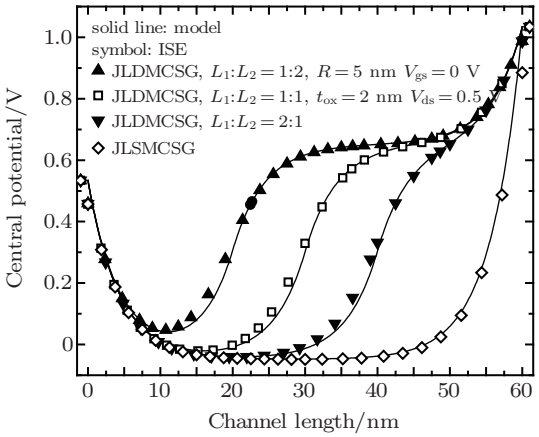


Fig. 2. Channel central potential along the channel for JLSMCSG and JLDMCSG with different ratios of L_1 and L_2.

Figure 3 shows the central potential profile for JLSMCSG and JLDMCSG with different drain voltages. It is clear that, owing to the potential step in JLDMCSG, there is no significant change in central potential under M_1 as the drain bias is increased even up to 2 V. Hence, JLDMCSG accounts for effective suppression of DIBL. For JLSMCSG, although the central potential is lower than that for JLDMCSG, the channel potential is severely affected by drain voltage. As the drain bias increases, the position of the minimum central potential for JLSMCSG shifts toward the source while the minimum channel potential pulls up, resulting in intense DIBL.[15]

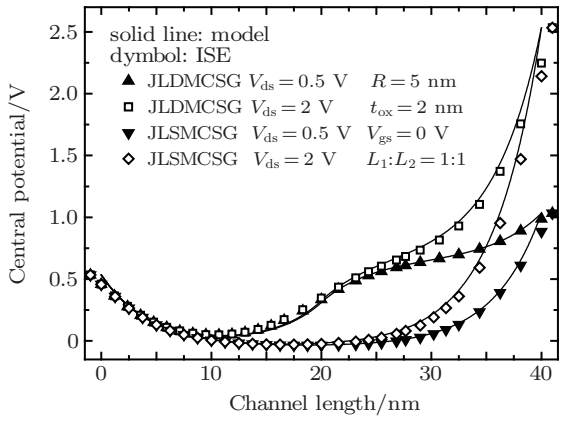


Fig. 3. Channel central potential along the channel with various drain voltages.

The central horizontal electric field distribution along the channel is shown in Fig. 4. It is found that there exists one electric field peak for JLDMCSG, which ensures a better average electric field across the channel as compared with JLSMCSG. Therefore, carrier transport efficiency and device speed are increased in JLDMCSG.[16] The difference at $z = 30$ nm between model result and ISE result is mainly caused by the accuracy of the mesh grid when constructing the device structure.

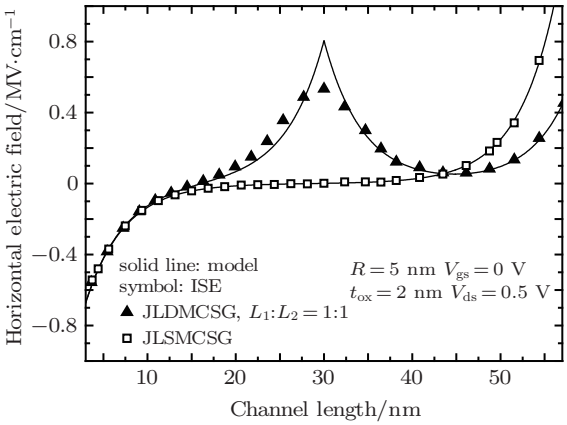


Fig. 4. Horizontal central electric field along the channel for JLSMCSG and JLDMCSG with different ratios of L_1 and L_2.

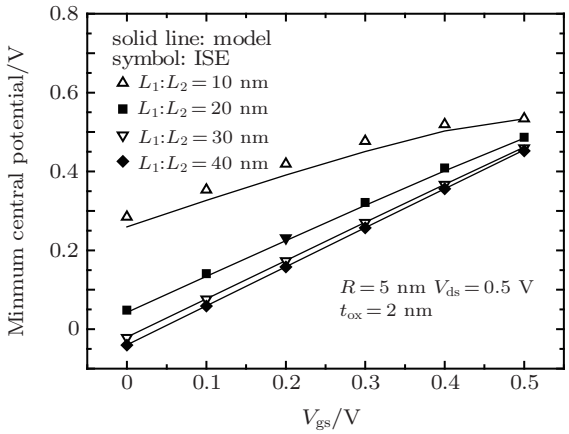


Fig. 5. Variation of the minimum central potential of region 1 with the gate bias V_{gs} for different channel lengths.

Figure 5 shows the dependence of the minimum central potential of region 1 on the gate bias with channel length as a parameter. It is revealed that with the channel length decreasing, the minimum central potential of region 1 is pulled up, which leads to the decrease of threshold voltage. It is worth noting that for a long channel device (such as $L_1 = L_2 = 40$ nm), the variation of the minimum central potential of region 1 is linearly dependent on gate bias, while for a short channel device (such as $L_1 = L_2 = 10$ nm), the minimum central potential of region 1 deviates from the linear relation with V_{gs}. The main reason is that as the channel length decreases, the threshold voltage of JLDMCSG is decreased (for $L_1 = L_2 = 10$, V_{th} is smaller than 0.4 V), thus, when V_{gs} is over

0.4 V, the device is no longer under the subthreshold condition. When channel length is too short (such as $L_1 = L_2 = 10$ nm), the source/drain diffusion problem will cause small errors between model results and ISE results.

The dependence of the threshold voltage roll-off on the channel length L for different oxide thicknesses is shown in Fig. 6. The plot indicates that a larger oxide thickness will induce a greater threshold voltage roll-off. The gate gradually loses control of the channel as the oxide thickness increases. This is because a large oxide thickness will resist the vertical electrical field from the metal gate into the channel, resulting in degradation of threshold behavior. Therefore, to suppress the threshold voltage roll-off, a thin oxide is preferred.

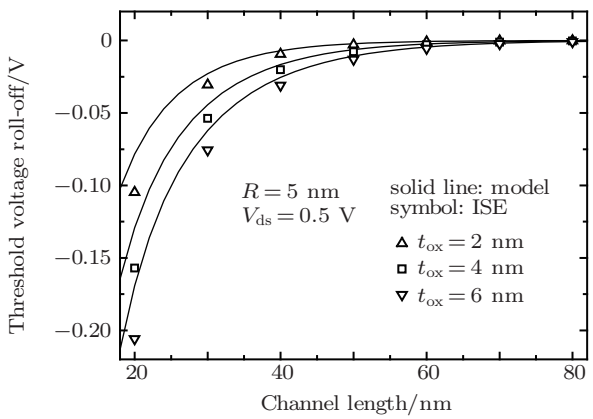


Fig. 6. Threshold voltage roll-off versus the channel length for different gate oxide thicknesses.

Figure 7 shows the threshold voltage roll-off of JLDMCSG against channel length with various radii of the silicon channel. A small radius of the silicon channel leads to less threshold voltage roll-off. However, when the radius of the silicon channel is less than 5 nm, the quantum effects that cause different device characteristics will become important. In this paper, we are only evaluating a device with a silicon channel radius larger than 5 nm. Therefore, quantum effects can be ignored.[17]

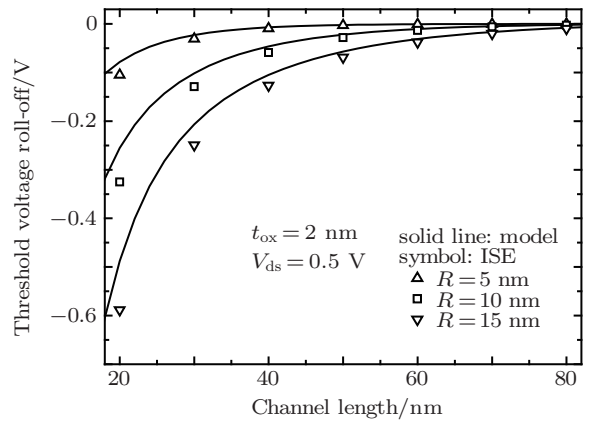


Fig. 7. Threshold voltage roll-off versus the channel length for different silicon radii.

The effect of the gate ratio L_1 to L_2 on the threshold voltage roll-off is illustrated in Fig. 8. The smallest ratio of L_1 to L_2 (1:2) degrades the threshold voltage much more than other ratios. It can be concluded that a larger ratio of control gate length to the total gate length can efficiently lower the channel potential barrier and enhance the immunity to SCE. From Fig. 6 to Fig. 8, the small error between model results and ISE results is mainly caused by the different threshold voltage definitions. In this paper, threshold voltage is defined as the gate voltage when the minimum central potential is equal to zero, while in the ISE simulator threshold voltage is obtained through I–V curves.

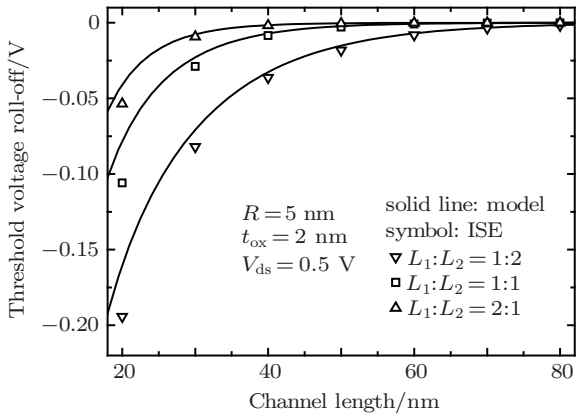


Fig. 8. Effect of the gate ratio of L_1 to L_2 on threshold voltage roll-off.

4. Conclusions

By solving 2D Poisson's equation in the two channel regions, an analytical model comprising channel central potential and threshold voltage for a short-channel JLDMCSG MOSFET has been developed. For JLDMCSG MOSFET, a large ratio of control gate length to total gate length, a thin gate oxide thickness and a thin silicon radius are needed for the device to exhibit good threshold voltage behavior. The results obtained from the models agree well with the simulated results obtained from ISE. This paper not only provides accurate analytical models, but also a basic guidance for JLDMCSG MOSFET.

Acknowledgment

The authors would like to thank Prof. T K Chiang for helpful discussion.

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