TOPICAL REVIEW — Low-dimensional nanostructures and devices

Field-effect transistors based on two-dimensional materials for logic applications*

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Field-effect transistors (FETs) for logic applications, based on two representative two-dimensional (2D) materials, graphene and MoS_2, are discussed. These materials have drastically different properties and require different considerations. The unique band structure of graphene necessitates engineering of the Dirac point, including the opening of the bandgap, the doping and the interface, before the graphene can be used in logic applications. On the other hand, MoS_2 is a semiconductor, and its electron transport depends heavily on the surface properties, the number of layers, and the carrier density. Finally, we discuss the prospects for the future developments in 2D material transistors.

Keywords: graphene, MoS_2, two-dimensional (2D) materials, field-effect transistors

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1. Introduction

The dimensions of modern silicon metal-oxide-semiconductor field-effect transistors (MOSFETs) have been shrinking exponentially for over four decades, following the prediction of Moore's law. Such scaling makes the transistors perform faster from generation to generation, but at the same time, requiring more power density. As the critical dimension of transistors is below 50 nm, the conventional planar structure faces more and more challenges in heat management, simply, because the gate gradually loses control over the channel and is not as efficient in switching off the devices, the so-called short-channel effects.[1] As a result, much leakage current passes through the transistors even when they are at the "off" state, giving rise to huge power consumption. This has been one of the major issues preventing further scaling down of MOSFETs. In order to minimize such effects, many new approaches have been implemented based on silicon technology, including the use of high-k dielectrics[2] and multiple gates[1] to better switch off the devices. On the other hand, people have also been seeking other materials to complement or even replace silicon technology. From electrostatics point of view, it is favorable to use thinner channel materials, as the characteristic channel length to eliminate short-channel effects is proportional to $\sqrt{t_{\rm ch}t_{\rm ox}}$, where $t_{\rm ch}$ and $t_{\rm ox}$ are the thicknesses of channel and gate oxide respectively.[1] Fortunately, there are many two-dimensional (2D) materials with only one or few atomic layers and attractive attributes that may enable future electronic devices. In recent years, they have been the focus of attention from both academia and industry. Transistors of 2D materials benefit from the ultrathin body, and are expected to show better electrostatics and reduced short-channel effects toward further scaling.

Most 2D materials exist in bulk form, stacked vertically via weak van der Waals interactions, while the in-plane bonds are covalent in nature.[3,4] Such properties enable the exfoliation process to isolate 2D materials down to single atomic layer. For logic applications, the minimum requirements from a materials perspective include high carrier mobility, a bandgap on the order of 1 eV and the ability to form Ohmic contacts, while the requirements from the integration perspective include large scale, a cost effective synthesis method, processability with CMOS technology and other compatibilities with CMOS technology.[5] Such materials have yet to be identified. However, in the past few years, we have witnessed major progress in the area of 2D materials and electronic devices, which we believe represents one of the most promising directions in nano-electronics. Although 2D materials can exhibit diverse properties, ranging from insulator, semiconductor, metal to even superconductor,[3,4] they all share one common feature: high specific surface area. Therefore, 2D materials are extremely sensitive to surface and interface properties, which, on the other hand, can be exploited to change the properties of the materials. In this review, we select two representative 2D materials, graphene and MoS_2, and focus on the engineering of material properties for transistor applications.

The review is organized as follows. In Section 2, the graphene FETs are discussed, with a focus on the engineer-

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ing of bandgap, doping and interface to achieve high on/off ratio and high mobility transistors. In Section 3, we review the basic properties of MoS_2, a member of the transition metal dichalcogenides (TMDs), and the effects of interfaces, numbers of layers and carrier densities on transistor performance. In Section 4, we discuss the prospects for future developments in 2D material transistors.

2. Graphene field-effect transistors

Graphene has been the center of focus of 2D material research since its successful isolation in 2004.[6–10] Graphene has a hexagonal lattice structure, with two equivalent sublattices in each unit cell (Fig. 1(a)). The low energy electronic band structure of graphene is drastically different from that of conventional semiconductors[9,10] (Fig. 1(b)). First, graphene has zero bandgap, with degenerate conduction and valance bands at the six corners of the Brillion zone. Second, near the zone corners, the dispersion relation is linear rather than quadratic which resembles ultrarelativistic particles and can be described by the massless Dirac equation. Therefore, the electrons in graphene are called massless Dirac fermions and the zone corners are called Dirac points. Third, the density of states at the Dirac points is zero, making graphene a semimetal with a tunable Fermi level. The unique band structure of graphene has led to many intriguing phenomena, e.g., the half-integer quantum Hall effect,[11,12] Klein tunneling,[13] and electron focusing.[14]

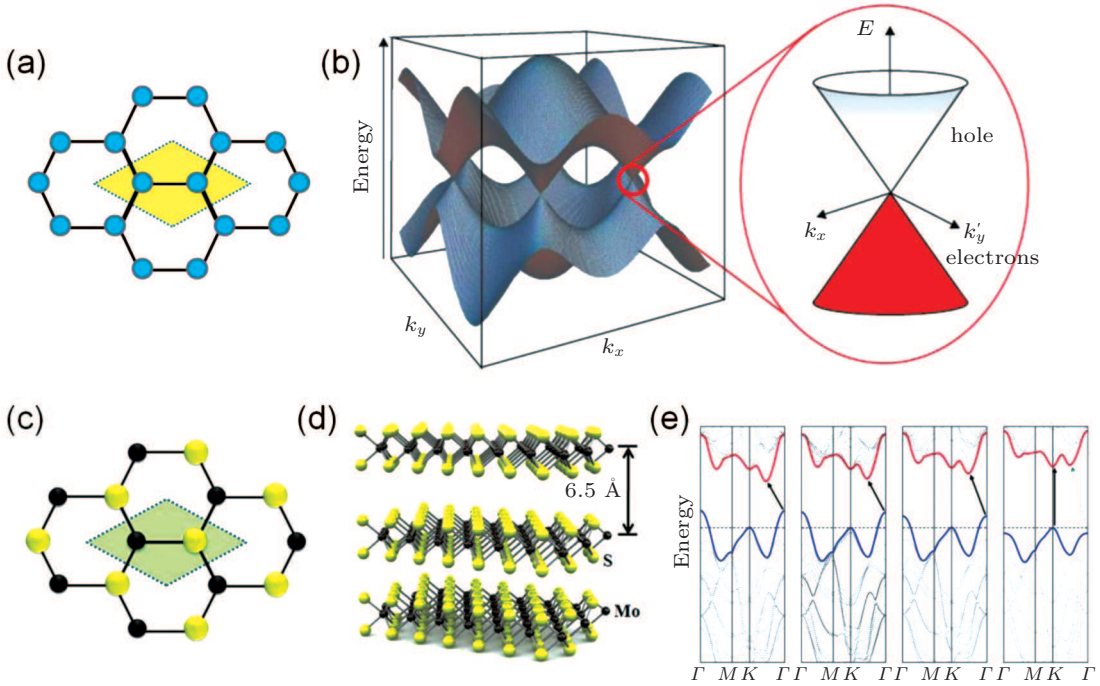


Fig. 1. (a) The lattice structure of graphene with the yellow region as the unit cell. (b) Graphene band structure. Enlargement of the band structure close to the K and K', points showing the Dirac cones.[10] (c) Lattice structure of MoS_2 with the green region as the unit cell.[4] (d) Three-dimensional (3D) representation of the structure of MoS_2. Single layers, 6.5-Å thick, can be extracted using scotch tape-based micromechanical cleavage.[81] (e) Calculated band structures of (first) bulk MoS_2, (second) quadrilayer MoS_2, (third) bilayer MoS_2, and (fourth) monolayer MoS_2. The solid arrows indicate the lowest energy transitions. Bulk MoS_2 is characterized by an indirect bandgap. The direct excitonic transitions occur at high energies at the K point. With reduced layer thickness, the indirect bandgap becomes larger, while the direct excitonic transition barely changes. Monolayer MoS_2, in the right panel, is a direct bandgap semiconductor.[78]

Graphene is very attractive in electronics applications, mainly due to its high mobility.[6] Theory predicts that the room temperature intrinsic mobility for both electrons and holes can be higher than 10^5 cm^2/(V·s), limited by phonon scattering.[15] Such a value is much greater than the room temperature electron mobility of most III-V compound semiconductors, not to mention the much worse hole mobility in III-V.[16] The highest reported mobility in graphene is $\sim 2 \times 10^5$ cm^2/(V·s), measured on suspended graphene at ~ 5 K.[17] In addition, graphene (and other 2D materials) has planar structure and is intrinsically compatible with the planar technology used in the microelectronics industry, which is important for future-generation electronics. The compatibility issue is much worse for one-dimensional carbon nanotubes (CNTs) and semiconducting nanowires, where one has to solve the problem of deterministic placement over a large area for real applications. Today, the CVD method enables the synthesis of millimeter-scale single crystal graphene,[18] and meter-scale poly-crystals.[19] The latter was successfully transferred onto 200-mm silicon wafers, showing promising compatibility.[5]

Although graphene is a promising candidate for next generation electronics, the unique electronic structure is actually not ideal for logic device applications. Graphene does not have

a bandgap, so at finite temperature, electrons are thermally excited to the conduction band. As a result, graphene transistors usually have an on/off ratio lower than 10 at room temperature, far below the requirement for logic applications. In addition, the massless spectrum at the Dirac point makes it difficult to confine electrons in a certain region, as they can easily tunnel through energy barriers by Klein tunneling. Therefore, we need to engineer the Dirac point in order to implement graphene in logic applications, the most important aspects being bandgap opening, doping control, and interface engineering.

2.1. Graphene bandgap opening

The primary concern about graphene being used in transistor applications is the absence of a bandgap.[5,6] There are several approaches to create a gap in graphene, including quantum confinement,[20,21] using AB-stacked bi-layers,[22,23] strain engineering,[24–26] and heterogeneous integration with other substrates.[27] The former two approaches are more feasible in experiment, while the latter two still await demonstrations in FETs.

AB-stacked bi-layer graphene is a zero-bandgap semiconductor due to the inversion symmetry between the two layers (Figs. 2(a) and 2(b)). However, a bandgap can be created when the symmetry is broken by a vertical electric field (gating), or asymmetric doping on both sides[22,28,29] (Fig. 2(b)). Usually, this is achieved by using both bottom and top gates to independently tune the carrier density and vertical displacement field. The size of the bandgap can be tuned continuously by the magnitude of the displacement field $D = (D_b + D_t)/2$, where $D_b = \varepsilon_b \left(V_b - V_b^0\right)/d_b$ and $D_t = -\varepsilon_t \left(V_t - V_t^0\right)/d_t$, whereas the carrier density is proportional to $D_b - D_t$. Here ε, d, and V^0 represent the dielectric constant, the thickness of the dielectric layer and the initial offset voltage due to unintentional doping.[29] The bandgap opening in bi-layer graphene has been confirmed both optically and electrically. In particular, Zhang *et al.* found that the optical absorption peak due to the electronic transition between the valance and conduction bands can be tuned continuously as expected.[29] The bandgap can be as large as 250 meV, consistent with self-consistent tight-binding and *ab initio* calculations (Fig. 2(c)). On the other hand, Xia *et al.* used a similar dual gate geometry to realize bi-layer graphene FETs with on/off ratios up to 100 at room temperature, which is the record for similar devices.[30] The extracted transport bandgap based on a Schottky barrier model was $\sim$ 130 meV when $D = 2.2$ V/nm, sightly smaller than the optical bandgap.

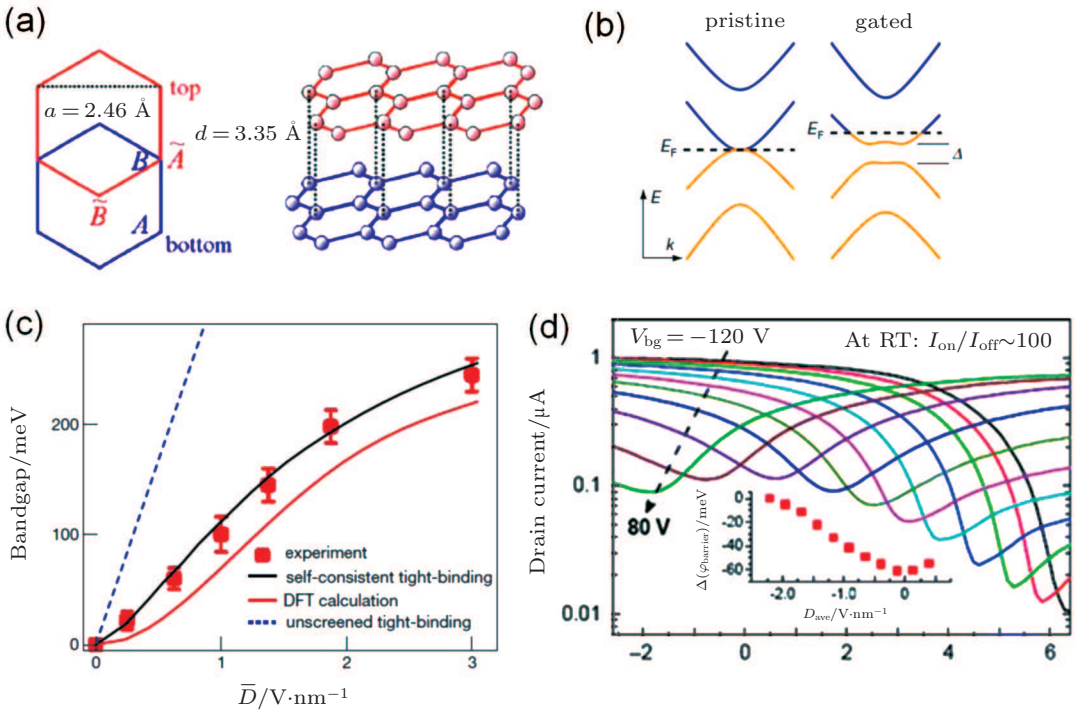


Fig. 2. (a) Structure of a graphene bilayer with honeycomb lattice constant $a = 2.46$ Å and interlayer separation $d = 3.35$ Å.[22] (b) Schematics of band structure of bilayer graphene. Left, the electronic structure of a pristine bilayer has zero bandgap (κ denotes the wavevector). Right, upon gating, the displacement fields induce a non-zero bandgap Δ and a shift of the Fermi energy E_F.[29] (c) Electric-field dependence of tunable energy bandgap in graphene bilayer. Experimental data (red squares) are compared with the theoretical predictions based on self-consistent tight-binding (black trace), *ab initio* density functional (red trace), and unscreened tight-binding calculations (blue dashed trace). The error bar is estimated from the uncertainty in determining the absorption peaks in the spectra.[29] (d) The room temperature transfer characteristics of a dual-gate bilayer graphene FET, V_{bg} is varied from -120 V to 80 V at steps of 20 V. Inset: variation of the Schottky barrier height, $\Delta(\varphi_{barrier})$, as a function of the average electrical displacement, D_{ave}, inferred from the off currents at the charge-neutrality point.[30]

Although bi-layer graphene offers a system wherein the bandgap can be continuously engineered, it has several drawbacks. First, theoretical studies have shown that the bandgap is up to ~ 200 meV-250 meV for high fields (1 V/nm -3 V/nm).[22,28] The relatively small bandgaps could only enable transistors with room temperature on/off ratios ~ 100. In addition, a sizable bandgap can be created only under a large electric field close to the breakdown value of gate oxides, which could cause reliability issues in device operation.

Another important way to open a bandgap is to use quantum confinement. Theoretical investigations of this possibility started as early as 1996. In their pioneering work, Nakada *et al.* used tight-binding calculations to show that the band structure of graphene nanoribbons (GNRs) depends heavily on the orientation (edge structure) and width.[20] In particular, GNRs with armchair edges (Fig. 3(a)) could be either metallic or semiconducting, depending on the number of repeating unit cells across the width direction (Fig. 3(b)), whereas GNRs with zigzag edges (Fig. 3(d)) are always metallic due to localized edge states (Fig. 3(e)). This first-order picture is further refined by first-principles calculations, which include edge termination groups and other subtle edge effects.[21,31] It was shown that hydrogen-terminated armchair and zigzag GNRs always have non-zero direct bandgaps, albeit for different reasons. For armchair ribbons, the bandgap opens up due to the combinational effect of quantum confinement and shortened inter-atomic distance (thus an increased hopping integral) at the edges. For zigzag edges, the bandgap opens up because of a staggered sublattice potential on the hexagonal lattice, which is due to edge magnetization. For both cases, the gaps are roughly inversely proportional to the width of the GNRs (Fig. 3(c)).[21] More interestingly, the localized state in zigzag GNRs could be antiferromagnetic (i.e., with opposite spin directions) when the ribbon is narrow enough. In such a system, one could achieve half metals with an electric field across the width direction, as one can close the gap for one spin while increasing the gap for the other (Fig. 3(f)).[32]

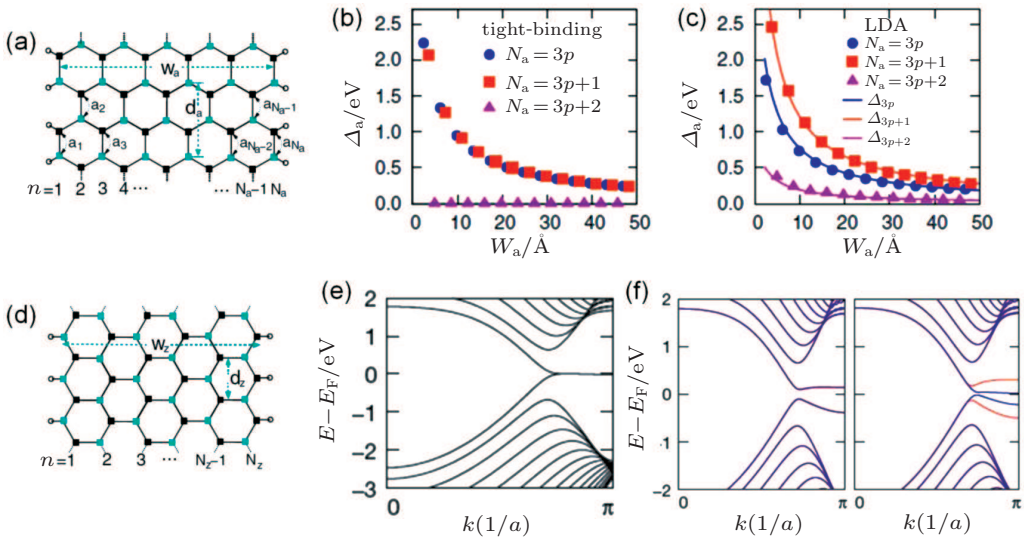


Fig. 3. (a) Schematic of a 11-AGNR. The empty circles denote hydrogen atoms passivating the edge carbon atoms, and the black and gray rectangles represent atomic sites belonging to a different sublattice in the graphene structure. The one-dimensional (1D) unit cell distance and ribbon width are represented by d_a and w_a, respectively. The carbon–carbon distance on the n-th dimer line is denoted by a_n.[21] (b) The variation of band gaps of N_a-AGNRs as a function of width (w_a) obtained from tight-binding calculations with $t = 2.70$ eV.[21] (c) The variation of band gaps of N_a-AGNRs as a function of width (w_a), obtained from first-principles calculations (symbols). The solid lines in (c) are the perturbative solutions of the Hamiltonian.[21](d) Schematic of a 6-ZGNR. The empty circles and rectangles follow the same convention described in panel (a). The 1D unit cell distance and the ribbon width are denoted by d_z and w_z, respectively.[21] (e) The spin-unpolarized band structure of a 16-ZGNR. The Fermi energy (E_F) is set to zero.[32] (f) From left to right, the spin-resolved band structures of a 16-ZGNR with E_{ext} 50.0 and 0.05 VÅ^{-1}, respectively. The red and blue lines denote the bands of a-spin and b-spin states, respectively. The Fermi energy (E_F) is set to zero.[32]

Although GNRs offer an appealing approach to engineering the bandgap, they are non-trivial to synthesize experimentally. As a rule of thumb, $E_g \sim 1/w$ (E_g and w are in units of eV nm) in GNRs (Fig. 3(c)). Therefore, in order to achieve a 1-eV gap, the width of the ribbon has to be on the order of 1 nm, and such a ribbon is extremely challenging to make. For logic applications, it is highly desirable to use sub-5-nm GNRs. Another issue is the edge structure. Most of the appealing properties of GNRs rely on atomically well-defined edges. However, most experimental techniques to produce GNRs do not have such capability – the only exception being bottom-up synthesis from aromatic precursors (Fig. 4(c)).[33] As we can see, the lack of control over the edges adds further complications in analyzing a GNR's properties. Next, we discuss several ways

to synthesize GNRs.

One of the most common ways to make GNRs is by plasma etching (Figs. 4(a) and 4(b)), wherein one uses resists, metals or nanowires as a mask and etch away the exposed graphene regions.[34–36] With this approach, Han *et al.* fabricated GNRs down to ∼ 14 nm using electron beam lithography (EBL) and observed that the transport gap was inversely proportional to the ribbon width.[34,37] The transport gap, induced by edge disorders, is different from the bandgap and is highly undesirable.[38] As a result, electrons are localized and hopping transport occurs near the Dirac point.[37] We note that even with EBL, making sub-5-nm features on graphene is very challenging due to the roughness of the resist. Bai *et al.* used nanowires as etching masks and were able to push the narrowest ribbon width to ∼ 8 nm. The GNRFETs based on this method showed an on/off ratio as high as ∼ 100 at room temperature.[39] However, it was difficult to control the positions of the masking nanowires. In order to fully exploit the scalability of lithographic patterning to address the sub-5-nm GNR challenge, Wang *et al.* designed a two-step process.[36] In the first step, GNR arrays with ∼ 20-nm width were fabricated with EBL. Then, a gas-phase etching process was developed to uniformly narrow the GNRs by heating graphene in a mixture of O_2 and NH_3 to 800 °C. Interestingly, such a process could only etch graphene from the edges without creating defects in the basal plane, due to the higher chemical reactivity of the edges. The etching rate could be as low as 1 nm/min, making it possible to control the width of GNRs in the nanometer regime. GNRs down to 4 nm (limited by the roughness of the starting GNRs) were successfully fabricated, and the FETs showed an on/off ratio up to ∼ 10^4 at room temperature, the record among lithographically patterned GNRs.

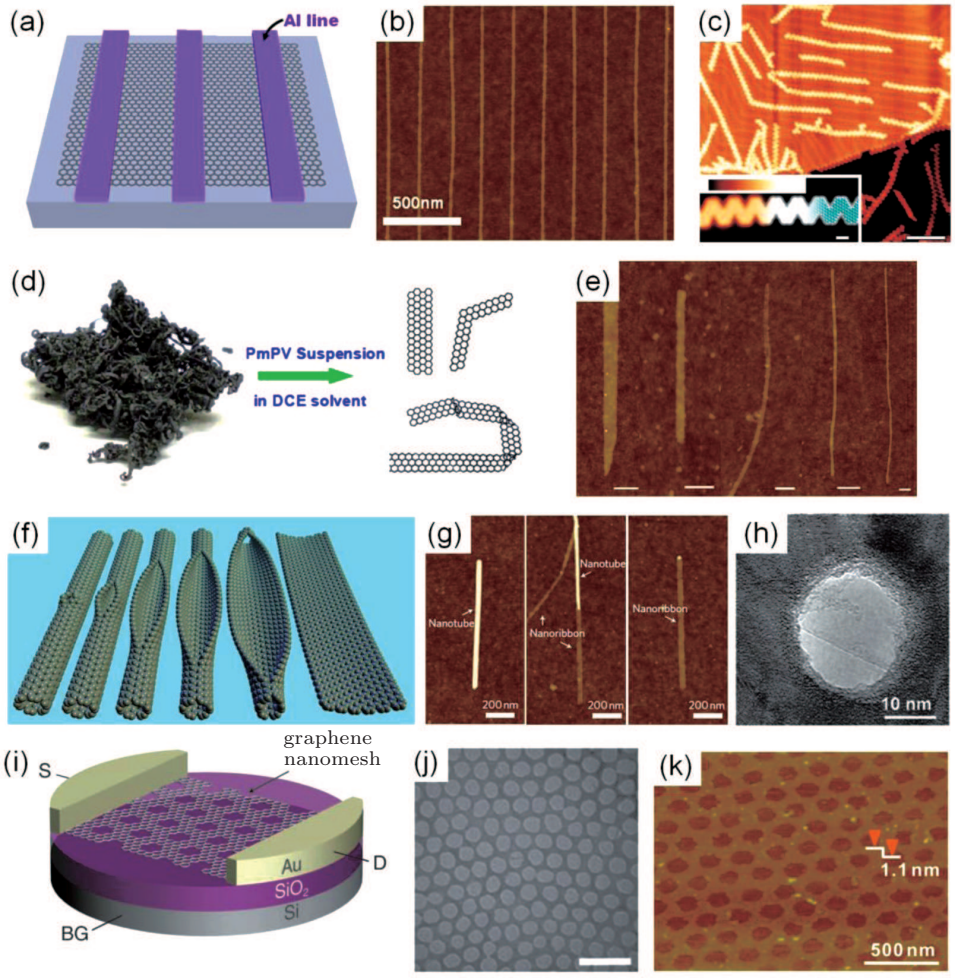


Fig. 4. (a) Schematics of the fabrication process of lithographically etching GNRs. The Al lines serve as etching masks.[36] (b) AFM image of a $w \approx 20$ nm GNR array at ∼ 200-nm pitch.[36] (c) STM image of bottom-up synthesized chevron-type GNRs fabricated on a Au(111) surface (T = 35 K, U = 22 V, I = 0.02 nA). The inset shows a high-resolution STM image (T = 77 K, U = 22 V, I = 0.5 nA) and a DFT-based simulation of the STM image (greyscale) with partly overlaid molecular model of the ribbon (blue, carbon; white, hydrogen).[33] (d) A schematic drawing of the sonochemical approach to GNR synthesis.[40] (e) AFM images of selected GNRs with widths in the 50-nm, 30-nm, 20-nm, 10-nm and sub-10-nm regions, respectively. [40] The scale bars are 100 nm. (f) Representation of the gradual unzipping of one wall of a carbon nanotube to form a nanoribbon. [43] (g) AFM images of pristine, partially and fully unzipped nanotubes using sonication method.[45] (h) Low magnification TEM images of GNRs with straight edge lines. Polymer residues are visible on the ribbons.[46] (i) Schematic of a graphene nanomesh patterned using block-copolymer-based lithography.[8] (j) Graphene nanomesh with a periodicity of 39 nm and neck width of 7.1 nm, obtained with additional over-etching. Scale bars, 100 nm.[48] (k) AFM image of graphene nanomesh structure by CVD growth with a thickness of 1.1 nm.[50]

Poor edge quality is an inevitable result of physical etching. On the other hand, chemistry could offer new possibilities. As an extreme example, Cai *et al.*[33] demonstrated a bottom-up synthesis of GNRs from the self-assembly of molecular precursors on metal surfaces (Fig. 4(c)). The GNR edge structure is atomically well-defined, and is determined by the precursor monomer, which opens up the possibility of bottom-up design of GNRs. In a more technologically relevant sono-chemical approach, commercial expandable graphite was sonicated in 1,2-dichloroethane with PmPV surfactant. After ultracentrifugation, $\sim$ 2-nm–50-nm wide GNRs were found in the solution (Figs. 4(d) and 4(e)).[40] Since many GNRs are micrometers long, it is possible to make FETs on SiO_2/Si substrate (Fig. 5(a)). The on/off ratio was found to depend exponentially on the width of the ribbons (Fig. 5(c)). The sub-5-nm GNRs obtained this way afforded graphene devices with on/off ratios over 10^6 for the first time (Fig. 5(b)). The high on/off ratio transistors suggest that a bandgap opening exists in narrow GNRs due to the quantum confinement. Using a Schottky barrier model, the bandgap of $\sim$2-nm GNRs was estimated to be $\sim$ 400 meV, consistent with theoretical calculations. They also systematically studied the transistor performance of these narrow GNRs. The on-state current density could be as high as $\sim$ 2000 μA/μm while maintaining a high on/off ratio. However, the mobility of these sub-5-nm GNRs was $\leq$ 200 $cm^2/(V{\cdot}s)$, probably due to the edge scattering.[41]

Another major discovery enabling chemical synthesis of GNRs involves longitudinally unzipping CNTs (Figs. 4(f)–4(h)). So far, several methods have been demonstrated, including metal nanoparticle catalysis,[42] oxidation and reduction,[43] plasma etching,[44] and sonication.[45] Although the first two of these approaches could enable large-quantity synthesis. Here, we focus on the latter two as they can produce ribbons with higher quality and are more suitable for transistor applications. For plasma etching, controllability is key because CNTs are easily etched away. Jiao *et al.*[44] embedded multiwalled CNTs in a PMMA polymer matrix to partially protect the CNTs. Most of the ribbons obtained were 10-nm–20-nm wide and 1–3 layers thick. Raman measurements suggest high quality of the GNRs with a low defect peak. FETs with on/off ratio up to $\sim$ 100 were demonstrated. Further improvement of GNR quality was achieved by using a sonication based method (Fig. 4(g)).[45] First, the multiwalled CNTs were mildly burned in air to etch away the impurities and oxidize away the defects. Then sonication in 1,2-dichloroethane with PmPV surfactant was used to unzip the CNTs with high efficiency. Finally, the GNR solution was obtained by ultracentrifugation. The yield of GNRs was much higher than in the sono-chemical approach discussed previously. Most of the ribbons were below 20 nm and 1–3 layers (Fig. 4(g)). TEM study revealed that a portion of the GNRs had atomically smooth edges (Fig. 4(h)).[46] GNRs made this way have the highest mobility ($\sim$ 1500 $cm^2/(V{\cdot}s)$) among ribbons of similar widths, and the theoretically predicted edge states were observed by STM for the first time.[47]

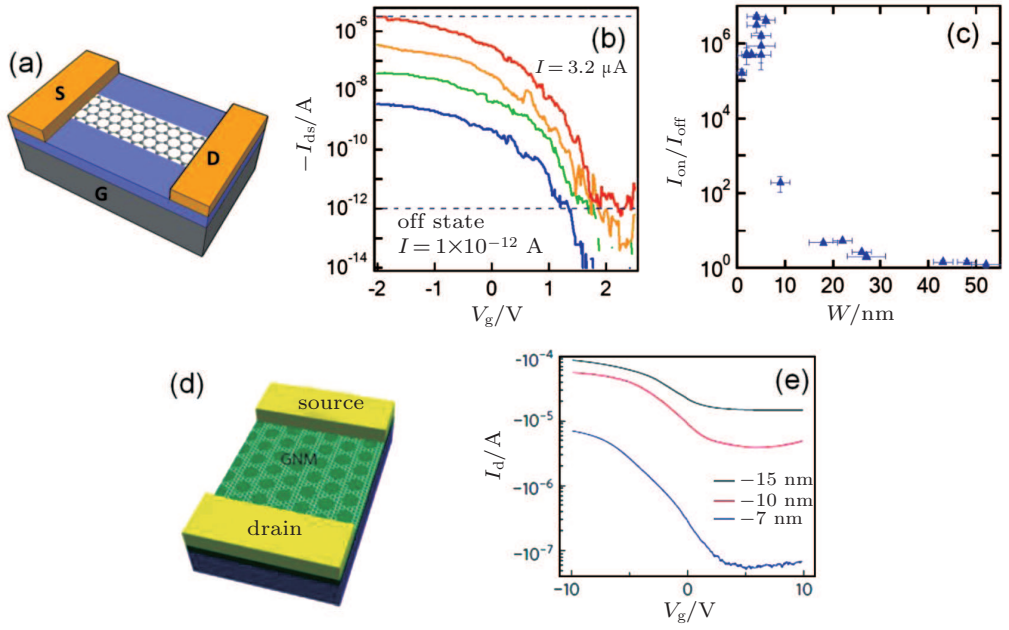


Fig. 5. (a) Schematics of backgated GNR FETs. Highly doped silicon is used as backgate.[41] (b) Transfer characteristics (the current versus thte gate voltage I_{ds}–V_{gs}) under various V_{ds} for a $w \sim 2$ nm±0.5 nm, $L \sim$236 nm GNRFET, $I_{on} = I_{off}$ ratio of $> 10^6$ is achieved at room temperature.[41] (c) The I_{on}/I_{off} ratios (under $V_{ds} = 0.5$ V) for GNRs of various ribbon widths of various ribbon width made by the sonochemical approach.[40] (d) Schematic of a graphene nanomesh FET. The device is fabricated on a heavily doped silicon substrate with 300-nm SiO_2 as the gate dielectric.[48] (e) Transfer characteristics at $V_d = -100$ mV for graphene nanomesh FET with different estimated neck widths of $\sim$ 15 nm (device channel width 6.5 μm and length 3.6 μm), $\sim$ 10 nm (channel width 2 μm and length 1 μm), and $\sim$ 7 nm (channel width 3 μm and length 2.3 μm).[48]

Although GNRs offer the possibility of bandgap engineering, one also needs to closely pack them to deliver high drive current in high performance applications. In this regard, graphene nanomesh, a derivative of GNR, is advantageous. A graphene nanomesh is a network of GNRs interconnected in a 2D manner (Fig. 4(i)). Similar to GNRs, the bandgap is determined by the narrowest neck width. Several methods have been demonstrated to produce graphene nanomesh, including block copolymer lithography,[48] anodic aluminum oxide (AAO) template,[49] and direct growth.[50] In particular, Bai *et al.*[48] used poly(styreneblock-methyl methacrylate) block copolymer to produce hexagonal patterns on graphene followed by plasma etching to create nanomesh (Fig. 4(j)). The width of the neck can be controlled by the etching time to be $\sim$ 5 nm–15 nm, with the highest on/off ratio $\sim$ 100 at room temperature (Figs. 5(d) and 5(e)). Since the density of the mesh was quite high, a single nanomesh device could deliver drive current $\sim$100 times higher than that of a single-GNR device. In another approach, Zeng *et al.*[49] used AAO as the template to create similar nanomesh patterns on graphene, with a neck width as small as 15 nm. To get large-area nanomesh, direct growth using CVD is desirable. Wang *et al.*[50] used nanosphere lithography to pattern a Cu substrate, leaving a hexagonal pattern of SiO_2 spheres on the Cu to prevent direct graphene growth in the CVD process. As a result, a large-area nanomesh with neck width $\sim$ 65 nm–75 nm was successfully grown and transferred onto SiO_2/Si substrate (Fig. 4(k)). The mobility of the grown nanomesh was three times higher than that of etched counterparts due to better edge quality. Although the aforementioned methods successfully demonstrated the advantages of graphene nanomesh, a technologically relevant approach still remains to be developed which requires low cost, minimal processing, and the ability to produce sub-10-nm nanomesh over wafer-scale.

2.2. Graphene doping control

In addition to the bandgap engineering, the doping control is also a critical issue in graphene. CMOS (complementary metal-oxide-semiconductor) technology is at the heart of modern integrated circuitry, which requires both p-type (hole doped) and n-type (electron doped) transistors to build the complex circuits. Since graphene has only one atomic layer, care must be taken to prevent excessive damage of graphene's lattice during the doping process. Otherwise, the properties of graphene will not be preserved. There are generically two approaches to dope graphene: chemical and physical approaches. The chemical methods normally rely on chemical bonding of foreign species with graphene, more or less like the conventional way to dope semiconductors. The physical methods on the other hand, do not involve chemical bonding. This is usually achieved by charge transfer from an electron donor or acceptor, which is quite effective because every atom of graphene is on its surface.

Since pristine graphene is very stable due to the absence of dangling bonds, chemical doping can be difficult when no defects and edges are present. A commonly used n-type doping element is nitrogen, which has one more electron than carbon. Wang *et al.*[51] found that GNRs can be n-doped when electrically annealed in NH_3 environment to a few hundred degrees Celsius. The doping was attributed to chemical reaction of NH_3 molecules with defects and edges, which was consistent with the theoretical calculations showing n-type doping by edge nitrogen groups (Fig. 6(a)). The doping level can be tuned by the electrical annealing power which determines the temperature of the GNR device. With this method, a high on/off ratio p-type GNRFET was transformed to n-type device *in situ*, with similar on- and off-state currents, indicating the GNR structure was not damaged during the process (Fig. 6(b)). For the pristine graphene, NH_3 plasma has to be used for appreciable chemical doping. For weak plasma, the nitrogen groups form initially at the edges because of the high chemical reactivity there.[52] When the plasma is strong enough to damage the graphene lattice, nitrogen can be incorporated to dope the graphene from the plane.[53] Similarly, for p-type doping, chlorine plasma was found to have slow reaction kinetics with graphene and afford controllable p-doping (Fig. 6(c)).[54]

When graphene is defective, foreign species can bond with it more easily. A model system in this case is graphene oxide (GO) with many oxygen groups and dangling bonds.[55] Li *et al.*[56] found that nitrogen can be incorporated into graphene oxide by thermal annealing at a temperature as low as 300 °C, when the GO can be simultaneously reduced. However, for GO pre-annealed in H_2, the same annealing gives much less nitrogen signal, suggesting that defect sites are needed to form the nitrogen groups and dope the graphene. Indeed, molecular dynamics simulations suggest that both carbon vacancies and the surrounding oxygen groups are necessary to form the nitrogen groups. Nitrogen can take various forms in graphene including 5- and 6-member rings and substitutional sites depending on the initial local structure and annealing temperature.[57] These nitrogen species are responsible for the n-type doping in graphene as confirmed by first-principles calculations.

Another approach to chemically n-dope graphene is to introduce nitrogen during *in situ* growth, which is especially useful for CVD graphene. Wei *et al.*[58] introduced CH_4 and NH_3 at the same time during CVD growth and observed a nitrogen signal in the graphene (Fig. 6(e)). The nitrogen can be substitutional, pyridinic or pyrrolic, as can be determined from the X-ray photoelectron spectroscopy (Fig. 6(d)). The resulting graphene showed n-type transistor behavior as expected (Fig. 6(f)). Such *in situ* growth of doped graphene could be potentially used for other elements as well.

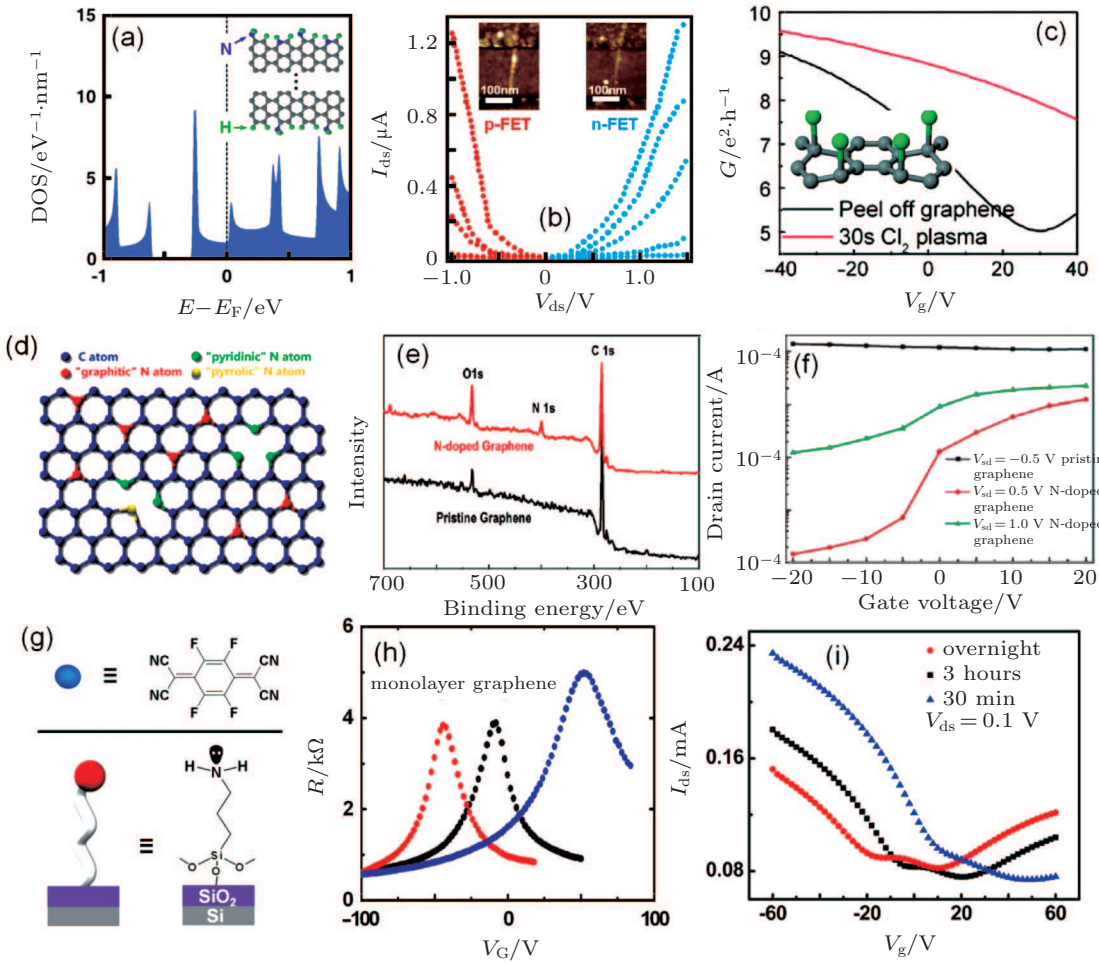


Fig. 6. (a) Calculated DOS of a 21-armchair GNR with nitrogen-containing groups on the edge sites, which is an n-type semiconductor. (Inset) Two unit cells of the edge structures of the simulated GNR. Each unit cell has one NH and two C–NH_2 groups.[51] (b) The I_{ds}–V_{ds} curves of the same device before and after electrical annealing in NH_3. Red curves were taken on an as-made device: $V_{gs} = -40$ V, −37 V, −34 V, −31 V, and −28 V from top to bottom. Blue curves were taken on e-annealed device: $V_{gs} = 40$ V, 35 V, 30 V, 25 V, and 20 V from top to bottom. (Insets) AFM images of the device before and after e-annealing. Height was reduced by ∼ 0.4 nm after e-annealing due to removal of PmPV coatings.[51] (c) The I_{ds}–V_g characteristics of a graphene sheet device before and after chlorine plasma treatment, taken at $V_{ds} = 1$ mV. (Inset) Atomistic structures of the chlorine functionalized graphene.[54] (d) Schematic representation of the N-doped graphene. The blue, red, green, and yellow spheres represent the C, "graphitic" N, "pyridinic" N, and "pyrrolic" N atoms in the N-doped graphene, respectively.[58] (e) XPS spectra of the pristine graphene and the N-doped graphene.[58] (f) Transfer characteristics of the pristine graphene (V_{ds} at −0.5 V) and the N-doped graphene (V_{ds} at 0.5 V and 1.0 V).[58] (g) Chemical structures of NH_2-functionalized SAMs on a SiO_2/Si substrate (bottom) and F4-TCNQ (top).[62] (h) Current–Voltage transfer characteristics of monolayer graphene FETs with molecular doping agents.[62] (i) Drain-source current versus gate voltage as a function of heating time for a graphene p–n junction.[63]

Since graphene has one atomic layer, charge transfer by surface functionalization is very effective. Compared with the chemical methods discussed above, these physical methods have some advantages. First of all, they do not rely on chemical bonding, so the pristine nature of graphene is largely preserved. Secondly, it is easier to locally engineer the doping of graphene and create novel device structures. Chen *et al.*[59] evaporated potassium onto graphene to realize controlled n-doping. However, the mobility of graphene was gradually degraded due to charge impurity scattering. In addition, the potassium is not air-stable, limiting its use in electronic devices. Alternatively, self-assembled monolayers (SAMs) have been shown to effectively modulate graphene doping. SAMs are widely used to passivate the surfaces of metals, oxides and semiconductors.[60,61] They form strong covalent bonds to the underlying surfaces and are self-assembled in a close-packed manner. Depending on the chemical group at the end of a SAM, it can be either charge-donating or -withdrawing. For examples, SAMs with the most electronegative fluorine element (such as fluoroalkyltrichlorosilane, or FTS) tend to withdraw electrons from surroundings and cause p-doping, while those with an amine group (such as (3-aminopropyl)triethoxysilane, or APTES) tend to donate electrons and cause n-doping. Park *et al.* exfoliated graphene on APTES functionalized substrates to achieve n-doping. Additionally, they deposited 2,3,5,6-tetrafluoro-7,7,8,8-tetracyanoquinodimethane (F4-TCNQ) on graphene to achieve p-doping (Figs. 6(g) and 6(h)).[62] With APTES and F4-TCNQ sandwiching a bi-layer graphene vertically, a built-in electric field was established to open a bandgap, af-

fording FETs with on/off ratio ∼26. The ability to pattern SAM also allows for graphene lateral heterojunctions. Sojoudi *et al.*[63] used lithography to pattern strips of alternating APTES and perfluorooctyltriethoxysilane (PFES) and transferred graphene across the interfaces. This way, the graphene was locally doped differently and acted as a pn junction, with two distinct Dirac points in the transfer characteristics (Fig. 6(i)). More complex elements or even circuits are envisioned based on such local doping control techniques.

2.3. Graphene interface engineering

One distinct feature of graphene is its 2D nature, with all the atoms on the surface. Various properties of graphene depend highly on surface and interfaces, which, on one hand, can be exploited to engineer the graphene, such as doping, but on the other hand, such actions inevitably introduce extra scattering. The most commonly used substrate for graphene devices is SiO_2. It has been found that the room temperature mobility of graphene devices on SiO_2 is limited by surface phonons to $\sim 4 \times 10^4$ cm^2/(V·s), much inferior to the intrinsic limit.[64] In reality, this value is further degraded to less than $\sim 1 \times 10^4$ cm^2/(V·s) by charged impurities and surface roughness on the substratel.[3] Such degradation highlights the importance of interface engineering in graphene (and other 2D materials).

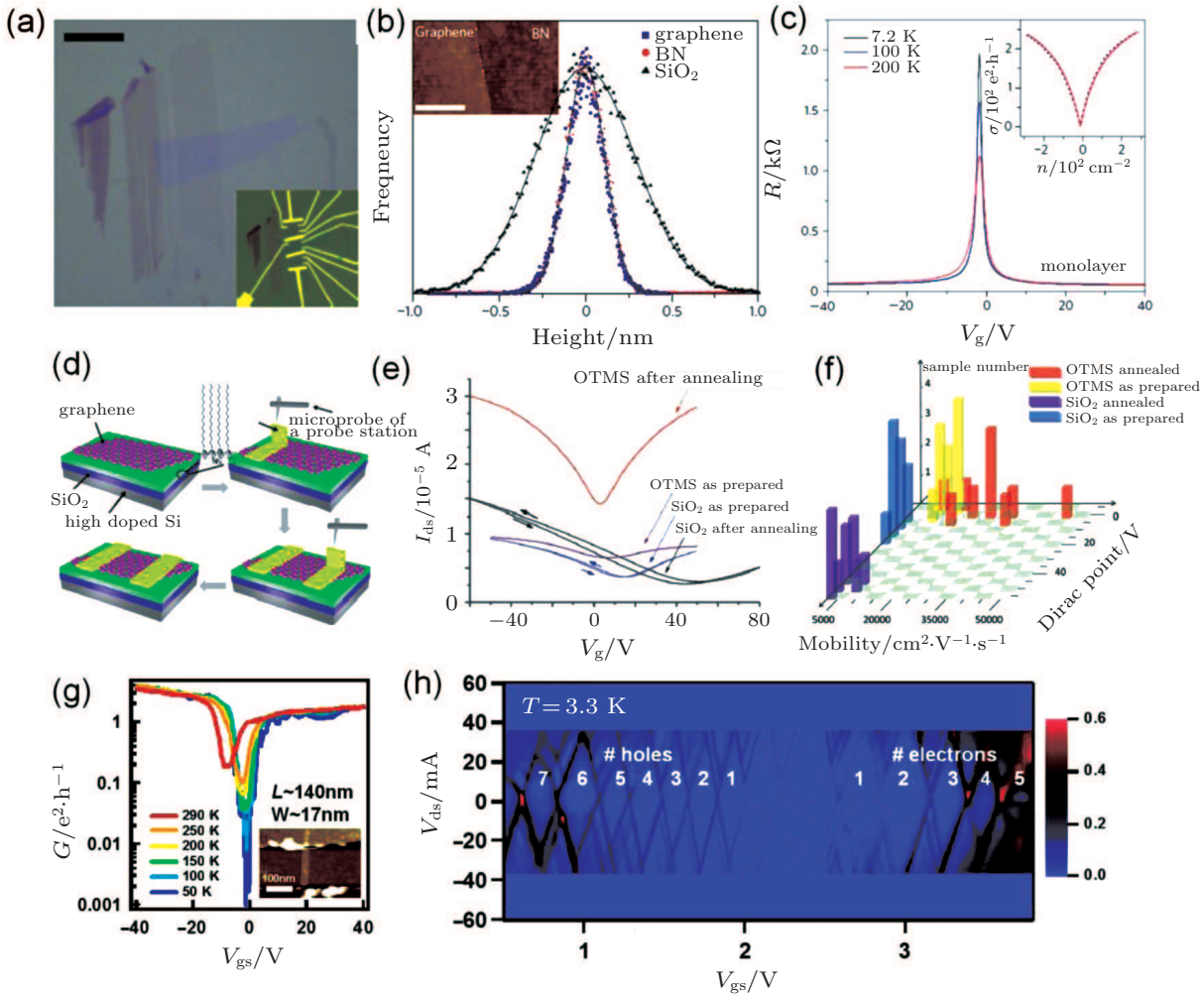


Fig. 7. (a) Optical images of graphene after transfer onto BN. Scale bars, 10 mm. Inset: optical image after electrical contact fabrication.[65] (b) Histogram of the height distribution (surface roughness) measured by AFM for SiO2 (black triangles), h-BN (red circles) and graphene-on-BN (blue squares). Solid lines are Gaussian fits to the distribution. Inset: high resolution AFM image showing a comparison of graphene and BN surfaces. Scale bar, 0.5 mm.[65] (c) Resistance versus applied gate voltage for monolayer graphene on h-BN. Insets: corresponding conductivity.[65] (d) Schematic illustration of the lithography-free process used in graphene FET fabrication on SAM functionalized SiO_2 substrate.[72] (e) Drain–source current versus gate voltage for graphene FET on as-prepared OTMS SiO_2/Si before and after annealing, and on as-prepared bare SiO_2/Si before and after annealing. The devices are the same size ($L/W = 7$), and both were measured at 290 K under ambient conditions.[72] (f) Histogram of mobility and the Dirac point of different graphene FETs on bare SiO_2/Si and on OTMS-modified SiO_2/Si substrates. The measurements are performed at room temperature under ambient conditions.[72] (g) Low-bias ($V_d = 1$ mV) G–V_{gs} characteristics for an unzipped high-quality GNR device under various temperatures down to 50 K. Inset: AFM image of the device.[74] (h) Differential conductance as a function of V_{gs} and V_{ds} at 3.3 K near the bandgap showing regular Coulomb blockade patterns and excited states. The number of electrons and holes in the quantum dot are marked.[74]

Perhaps the best graphene substrate is its mother material graphite, because of the weak van der Waals interaction and atomic flatness. However, the metallic nature of graphite makes it impossible to fabricate graphene devices on it. Therefore, the insulating brother of graphite, the layered hexagonal boron nitride (hBN, sometimes called white graphite) is an ideal choice. hBN has a lattice structure similar to that of graphene. The two different atoms in the unit cell make hBN a band insulator with bandgap above 5 eV. In addition, hBN has many unique properties for an ideal substrate: atomic flatness, absence of charge traps, and large optical phonon modes, all of which lead to reduced carrier scattering in graphene. Similar to graphene, hBN flakes down to single layer can also be exfoliated onto SiO_2/Si substrates. Dean *et al.*[65] first demonstrated a dry transfer process to place graphene on hBN flakes on a SiO_2/Si substrate (Fig. 7(a)). During the dry transfer, the side of graphene facing hBN was never in contact with any liquid, so as to preserve the pristine nature of the interface, which turned out to be very important. AFM and STM characterizations indicated that graphene is much flatter on hBN than on SiO_2 and much more homogeneous (Fig. 7(b)).[66] Subsequent electrical measurements showed a Hall mobility of 25,000 $cm^2/(V\cdot s)$, while the field-effect mobility was as high as 1.4×10^5 $cm^2/(V\cdot s)$ (Fig. 7(c)), close to that of suspended graphene.[65] So far, graphene sandwiched between hBN offers the cleanest sample on any substrate, where many exciting quantum states have been observed, including fractional quantum Hall states,[67] quantum Hall isospin ferromagnetic states,[68] and Hofstadter spectra.[69–71]

Although hBN is an ideal substrate for investigating quantum phenomena and device demonstrations, it is difficult to use in large scale applications because the hBN flakes are usually only tens of micrometers in size and the transfer process is rather tedious. To solve this problem, a SAM with neutral end groups such as octadecyltrimethoxysilane (OTMS) and octadecyltrichlorosilane (OTS) can be used instead. These SAMs can be grown directly on SiO_2 substrates prior to graphene transfer to significantly reduce charged impurities and surface phonon scattering in the SiO_2. Obviously, such a process can be scaled up. Wang *et al.*[72] used OTMS-treated SiO_2 as substrate and fabricated graphene FETs with mobility of 4.7×10^4 $cm^2/(V\cdot s)$, nearly one order of magnitude higher than devices on SiO_2 (Figs. 7(d)–7(f)). They attributed the increase of mobility to the reduction of charged impurities and remote interfacial phonon scattering.

For GNRs, the most important interface is the edges, which greatly affect the charge transport and device performance. As we discussed previously, electron transport in etched GNRs is dominated by defect states introduced by edge roughness.[37,38,73] At low temperature, those GNRs exhibit transport gap (not bandgap) and multiple quantum dot behavior. However, drastically different behavior was observed for GNRs unzipped from CNTs by sonication. Wang *et al.* reported the observation of metallic behavior and a signature of bandgap in unzipped high-quality GNRs, indicating that edge disorder is not dominant,[74] consistent with TEM observations.[46] In contrast to etched ribbons, the unzipped ribbons behave like high-quality single quantum dots at low temperature with well-defined Coulomb blockade and excited states (Figs. 7(g) and 7(h)). Furthermore, they were a few hundred times more conductive than those obtained by oxidative unzipping of CNTs.[74,75] Therefore, these GNRs may have potential as new types of quantum wires to explore the widely predicted magnetic edge states and realize novel spintronic devices.

3. MoS_2 field-effect transistors

MoS_2 is a member of the layered TMDs which take the form of XM_2, where X represents a transition metal and M represents a chalcogen. The TMDs include 44 stable compounds that can form 2D structures, ranging from metals (e.g., $NbTe_2$, $TaTe_2$) and semiconductors (e.g., MoS_2, $MoSe_2$, WS_2) to superconductors (e.g., NbS_2, $NbSe_2$, TaS_2).[3,4,76] Similar to graphene, TMDs are layered materials with weak van der Waals interlayer interactions, and thus can be exfoliated down to single layer. Among TMDs, MoS_2 is one of the most investigated materials with potential electronic and optoelectronic device applications.[3] In the following discussion, we will focus on MoS_2.

The lattice structure of MoS_2 is depicted in Figs. 1(c) and 1(d). Figure 1(e) shows the band structure of MoS_2 with different numbers of layers. Single-layer MoS_2 is a direct gap semiconductor with bandgap $\sim$ 1.8 eV. For two layers and above, it is an indirect gap semiconductor with decreasing bandgap with increasing layers, reaching 1.1 eV for bulk MoS_2.[77,78] Compared with graphene, MoS_2 is a 2D material with bandgap suitable for logic device applications. Theoretical simulations based on a ballistic MOSFET model have shown that MoS_2 (and other TMDs) transistors outperform silicon transistors in terms of ballistic on-current at the scaling limit, where thin high-k dielectrics are used.[79] This is because the atomically thin body of TMDs offers better gate control, despite their larger effective electron mass. Therefore, TMDs are believed to be promising channel materials for nano-electronic device applications.

Earlier investigations of backgated single-layer MoS_2 FETs indicated n-type transistor behavior with mobility below $\sim$ 1 $cm^2/(V\cdot s)$.[80] In 2011, Radisavljevic *et al.*[81] fabricated dual gated MoS_2 transistors with ALD HfO_2 as topgate dielectrics (Fig. 8(a)). They found a significant increase of mobility to $\sim$ 200 $cm^2/(V\cdot s)$ after topgate integration, and attributed such an increase to dielectric screening of charged

impurities. Their devices showed an impressive on/off ratio $\sim 10^8$ and subthreshold swing of 74 mV/decade. The transfer characteristics are depicted in Fig. 8(b). This work is spurring great interest in electronic devices based on MoS_2 and other TMDs.

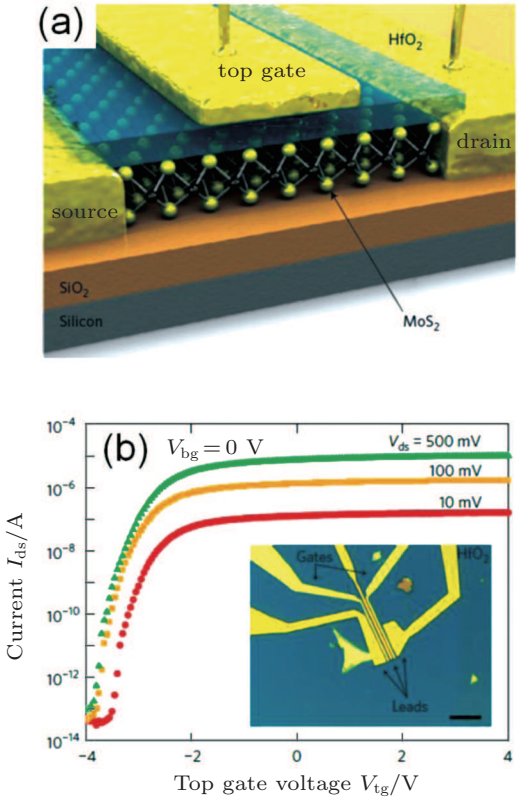


Fig. 8. (a) The 3D schematic view of dual-gated MoS_2 monolayer transistors.[81] (b) The I_{ds}–V_{tg} curve recorded for a bias voltage ranging from 10 mV to 500 mV. Measurements are performed at room temperature with the back gate grounded. Top gate width, 4 μm; top gate length, 500 nm. The device can be completely turned off by changing the top gate bias from −2 V to −4 V. For $V_{ds} = 10$ mV, the I_{on}/I_{off} ratio is $> 10^6$. For $V_{ds} = 500$ mV, the I_{on}/I_{off} ratio is $> 10^8$ in the measured range while the subthreshold swing $S = 74$ mV · dec^{-1}. Inset: Optical image of a device. The device consists of two field-effect transistors connected in series and defined by three gold leads that serve as source and drain electrodes for the two transistors. Monolayer MoS_2 is covered by 30 nm of ALD-deposited HfO_2 that acts both as a gate dielectric and a mobility booster. Scale bars, 10 mm.[81]

The performance of MoS_2 transistors depends highly on environment, number of layers and carrier density. Qiu *et al.*[82] found that after a mild annealing, the mobility of backgated MoS_2 FETs in high vacuum can be 50–100 times higher than in atmospheric ambience (Fig. 9(a)). The devices were degraded upon exposure to O_2 and can be recovered by annealing. They attributed such dramatic change to the absorption of O_2 and H_2O molecules, likely on defect sites. This is a very surprising result pointing to the importance of surface properties and passivation in MoS_2 and other TMD devices. For example, PMMA could be used to passivate MoS_2 devices to reduce the effect of O_2.[83]

In addition, the mobility of backgated MoS_2 FETs is sensitive to the number of MoS_2 layers. Several studies have shown that such a dependence is not monotonic but has a mobility peak around tens of nanometers (Fig. 9(b)).[84,85] At small thickness, the dielectric screening of long-range disorder (possibly Coulomb impurities) is very poor, leading to low mobility. For very thick samples, since the metal leads are only in direct contact with the bottom layer and the backgate is most effective in gating the bottom layers, the effective mobility is reduced. Many studies have shown that the mobility of backgated few-layer (meaning ≤3-layer) MoS_2 is on the order of 10 cm^2/(V·s),[81,82,86,87] while that of thicker samples can be as high as hundreds of cm^2/(V·s),[84,85,88] which is close to the upper limit determined by phonon scattering.[89] Furthermore, thick MoS_2 exhibits metallic behavior near room temperature,[88] again indicating phonons as the dominant scattering source. Another interesting observation is that single- or few-layer MoS_2 FETs are always n-type, regardless of the work function of the metal contact, while thicker MoS_2 can be ambipolar.[84] The origin of the electron doping is still unclear but could be related to the defects in MoS_2.[90]

The charge transport of MoS_2 also depends on the carrier density. Ye *et al.*[91] used ionic liquid as topgate dielectrics for MoS_2 transistors. The ionic liquid has extremely large gate capacitance due to the electrical double layer formation, and can be used to tune the carrier density up to $\sim 10^{14}$ cm^{-2}, far beyond the limit of conventional oxide dielectrics.[92] They found an insulator–metal–superconductor transition as the carrier density was gradually increased. The insulator–metal and metal–superconductor phase transitions occurred at $\sim 10^{12}$ cm^{-2} and 10^{13} cm^{-2} respectively. The insulator–metal transition has also been observed in a dual-gated single-layer MoS_2 transistor, at the carrier density $\sim 10^{13}$ cm^{-2} (Figs. 9(c) and 9(d)).[93] The insulator–metal transition was attributed to the electron–electron interactions in 2D MoS_2.

Although the TMDs have been studied for many decades, intensive research on related transistors has just started. Therefore, there are still many important issues to solve on a device level. For example, realizing CMOS-like devices and circuits requires p-type transistors, which have not been possible for single-layer MoS_2. This is related more fundamentally to the mysterious n-doping in MoS_2. Furthermore, the mobility of few-layer MoS_2 needs to be improved to hundreds of cm^2/(V·s) in order to be competitive with silicon. Presently, many possible charge scattering mechanisms are proposed, such as phonons, Coulomb impurities, substrate roughness, and short-range defects.[3] To reduce the influence of these factors probably involves interface engineering similar to that applied to graphene. However, the intrinsic room temperature mobility limit of ~ 400 cm^2/(V·s), determined by phonons, together with the large bandgap of 1.8 eV mean that MoS_2 is more suitable for low-power applications.

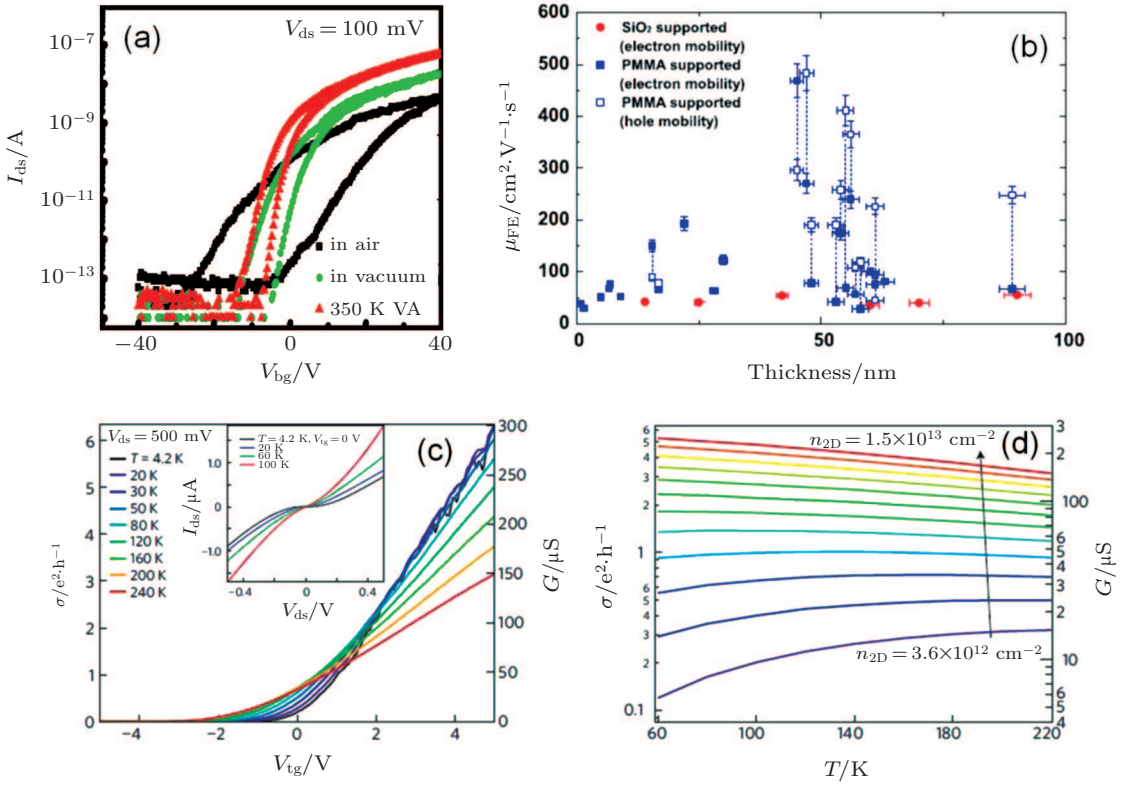


Fig. 9. (a) Double sweep I_{ds}–V_{bg} characteristics of the bi-layer MoS_2 FET, probed in air (square), in vacuum (circle), and after 350-K vacuum annealing for 24 h (triangle). Here, $V_{ds} = 100$ mV for all cases.[82] (b) Room temperature field effect mobility μ_{FE} as a function of thickness t for 25 PMMA-supported (blue squares) and 6 SiO_2-supported MoS_2 (red circles) devices. Only electron mobility is shown for SiO_2-supported devices. PMMA-supported devices with measurable ambipolar behavior are indicated as dashed-line connected hollow squares (corresponding to the hole carrier mobility) and solid squares (corresponding to the electron carrier mobility).[84] (c) Conductance G as a function of the top gate voltage V_{tg} at various temperatures. For low values of the top-gate voltage V_{tg}, the conductance follows a thermally activated behavior and decreases with temperature. Above $V_{tg} \sim 1$ V–2 V, depending on the temperature, monolayer MoS_2 enters a metallic state, manifested by an increasing conductance as the temperature is decreased. Inset: I_{ds} versus V_{ds} for $V_{tg} = 0$ V under $T = 100$ K, 60 K, 20 K, and 4.2 K, showing more obvious non-linearity at low temperature.[93] (d) Temperature dependence of the conductance for different values of charge density n_{2D}.[93]

4. Conclusion and outlook

Almost ten years have passed since graphene, the first real 2D material, was successfully isolated in 2004. We have already witnessed tremendous progress in electronic and optoelectronic devices based on 2D materials. Here, we only review the material considerations and devices for logic applications. Other areas like radio-frequency transistors,[94–97] photodetectors,[98–100] optical modulators,[101,102] and transparent conductive electrodes[19] have also made impressive achievements.

For graphene, the next question is: when is the first major application? Earlier this year, the European Union launched "graphene" as one of the two future emerging technology flagships. The purpose of this ten year, 1 billion Euro project is to "take graphene and related layered materials from academic laboratories to society, revolutionize multiple industries and create economic growth and new jobs in Europe."[103] For electronic device applications, graphene still faces many challenges. The cost of CVD growth which is one of the most promising industrial production methods, is still too high because of the high-temperature process and the removal of underlying metal substrate.[5] Further effort is needed to develop low temperature growth processes and non-disruptive transfer processes for graphene. Even more desirable is to grow high-quality graphene directly on dielectric materials. Another challenge is to improve the quality of graphene, which is particularly important for high-end device applications. So far, in academic laboratories, a graphene domain of millimeter scale can be synthesized by CVD.[18] However, the long growth time and high temperature make it economically unfavorable. In the end, we will need to develop a process to produce graphene with a controlled domain size, numbers of layers, and a defect density. In the device fabrication, we need to develop large-area processes that can create sub-10-nm features with controlled orientations, edge structures, and passivation in order to control the bandgap and reduce the electron scattering. Despite of all these challenges, the first electronic application of graphene is expected in the next few years, likely on touch screens and e-papers.[5] For transistor applications, it is likely that graphene is first implemented not as the active channel material, but as passive components in silicon integrated circuits such as interconnects.[5] The possibility of graphene replacing silicon and III-V for logic and RF applications remains to be evaluated.

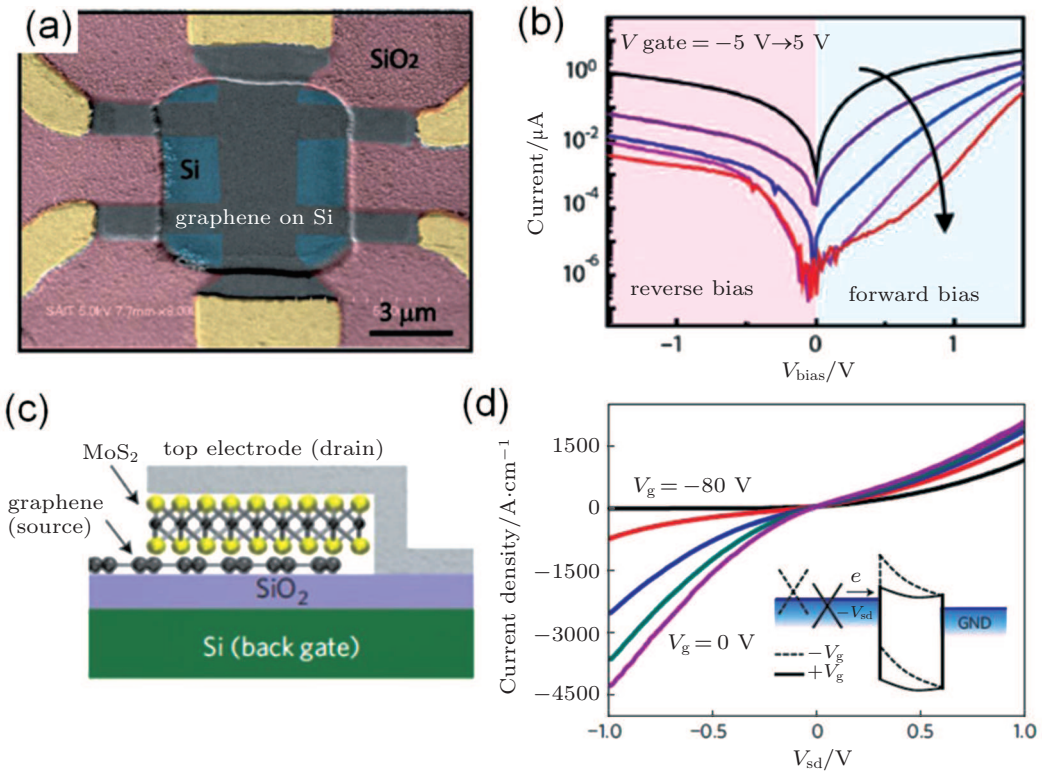


Fig. 10. (a) False-colored scanning electron microscopy image of a graphene barristor before the top gate fabrication process.[105] (b) Switching behavior of p-type graphene barristor in reverse (orange background) and forward (blue background) bias regimes. The graphene barristor current is plotted against the source drain bias at various fixed gate voltages, $V_{\rm gate}$ varies in the range of −5 V to 5 V, with a step of 2 V. The black arrow indicates the direction of increasing $V_{\rm gate}$.[105] (c) Cross-sectional schematic of a vertical MoS_2 transistor, with the graphene and top metal thin-film functioning as the source and drain electrodes, and the MoS_2 layer as the vertically stacked semiconducting channel, with its thickness defining the channel length. A silicon back gate is used with a 300-nm SiO_2 dielectric layer.[108] (d) The $I_{\rm sd}$–$V_{\rm sd}$ output characteristics of a vertical transistor. The current is normalized by the area. (Inset) The band structure at negative source bias at graphene ($V_{\rm sd} < 0$) with the top metal electrode connected to ground under positive (solid) or negative (dashed) $V_{\rm g}$.[108]

For other 2D materials, many fundamental issues remain to be solved before we can seriously consider their electronic device applications. One of the promising research directions recently is heterostructures based on 2D materials (Fig. 10). Such heterostructures are usually composed of lateral or vertical stacks of layered materials and take advantage of the gate-tunability of the barrier heights or work functions to achieve electronic[104–108] or optoelectronic devices.[109] For example, Yang *et al.*[105] demonstrated a barristor with a graphene/silicon interface, wherein the Schottky barrier can be electrically tuned by the gate (Figs. 10(a) and 10(b)). Such a device could achieve an on/off ratio greater than 10^5 without the need to engineer the bandgap. They also fabricated complementary p-and n-type barristors on 150-mm wafers, inverter and half-adder logic circuits, demonstrating the possibility of integrating graphene with silicon technology. In another work, graphene and MoS_2 were stacked together vertically to form a tunneling transistor.[108] The device achieved an on/off ratio of 10^3 while maintaining high drive current of 5000 A/cm^2, due to a large contact area and a thin MoS_2 tunnel barrier. The current is much higher than that of the conventional planar structure, opening up the possibilities for 3D integration of logic devices using 2D materials. Since there are many 2D materials with diverse properties, the possibilities of the heterostructures are even more diverse, making it possible to design a wide range of functionality based on pure 2D materials.[5]

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