Performance improvement of charge trap flash memory by using a composition-modulated high-k trapping layer*

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A composition-modulated $(HfO_2)_x(Al_2O_3)_{1-x}$ charge trapping layer is proposed for charge trap flash memory by controlling the Al atom content to form a peak and valley shaped band gap. It is found that the memory device using the composition-modulated $(HfO_2)_x(Al_2O_3)_{1-x}$ as the charge trapping layer exhibits a larger memory window of 11.5 V, improves data retention even at high temperature, and enhances the program/erase speed. Improvements of the memory characteristics are attributed to the special band-gap structure resulting from the composition-modulated trapping layer. Therefore, the composition-modulated charge trapping layer may be useful in future nonvolatile flash memory device application.

Keywords: composition modulated films, memory device, charge trap, atomic layer deposition

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1. Introduction

With the feature size of conventional floating gate type nonvolatile memory approaching its scaling limitation, tremendous effort has been made to explore low cost, high density, and nonvolatile solid state memory devices for usage in mobile electronics.[1–4] Among the family of nonvolatile memories, the charge trap flash memory (CTFM) devices have received much attention in electronic industry due to their advantages such as better scalability, low power, and process simplicity.[5] However, conventional CTFM devices have a fundamental problem with the trade-off between data retention and program/erase speed.[6,7] In order to solve the problem, extensive research has been carried out in recent years, involving the use of high-k dielectrics[8] and nanolaminated films as the charge trapping layer.[9] Tunneling barrier engineering using the high-k/low-k dielectric stacks was also proposed to improve the performances of the nonvolatile memory.[10] Tan *et al.*[11] reported that the memory characteristics can be enhanced with an Al_2O_3 doped HfO_2 charge trapping layer.[11] Tang *et al.*[12] also investigated the memory devices using an $(HfO_2)_{0.8}(Al_2O_3)_{0.2}$ film as the charge trapping layer. It was found that doping Al_2O_3 in HfO_2 can improve the program/erase speed of the memory device. This is attributed to the increase of the band offset between the tunneling layer and the charge trapping layer. In order to achieve the trade-off among the memory window, program/erase speed, and data retention, a promising engineering technique using composition-modulated $(HfO_2)_x(Al_2O_3)_{1-x}$ (CM-HA) dielectrics as the charge trapping layer in the CTFM device to improve the charge storage characteristics is proposed in this paper. This involves the formation of a peak and valley shaped band gap due to varying Al atomic ratio in the charge trapping layer.

2. Experiment

First, p-type Si (100) substrates with a resistivity of 3–20 Ω·cm were cleaned by the standard Radio Corporation of America (RCA) process to remove the native oxide. Then a 4-nm SiO_2 film as the tunneling layer was thermally grown in dry O_2 ambience. A 10-nm CM-HA (x is the HfO_2 mole fraction) film was deposited as the charge trapping layer (CTL) by the atomic layer chemical vapor deposition (ALD) using precursors $HfCl_4$ and $Al(CH_3)_3$. The percentage of Al in the CTL first increased and then decreased by controlling the number of ALD deposition cycles. Subsequently, a 12-nm Al_2O_3 layer was deposited by ALD as the blocking layer. A post-deposition annealing process was carried out at a temperature of 800 °C for 30 s in N_2 ambience. The X-ray diffraction (XRD) and selected area electron diffraction (SAED) pattern were used to investigate the crystalline behavior of the CTL as shown in Fig. 1. It was found that there was no diffraction peak after the high temperature annealing treatment for the CTL. On the other hand, SAED was also performed in the

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region of the CTL, as shown in the inset of Fig. 1, and there was no diffraction spot. The results also demonstrated that the CTL was still in an amorphous state after rapidly thermo-annealed at 800 ° for 30 s in N_2 ambient. Finally, a Pt gate electrode was formed by magnetron sputtering. The memory device was denoted as S1. To confirm the role of the CM-HA in the CTFM performance, samples with single uniform 10 nm $(HfO_2)_{0.2}(Al_2O_3)_{0.8}$(HA) or HfO_2 as the CTL were simultaneously fabricated, which were named S2 and S3, respectively. The electrical characteristics of the memory devices including memory windows, program/erase speed, and data retention characteristics were analysed by a Keithely 4200 semiconductor characterization system. The cross-sectional microstructures of the CTFM devices were characterized by transmission electron microscopy (TEM).

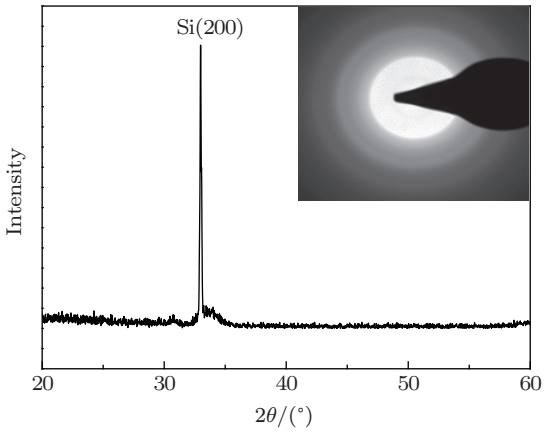


Fig. 1. XRD pattern of the CTL after annealing treatment. The inset is a selected area electron diffraction pattern of the CTL.

3. Results and discussion

The elemental compositions of CM-HA, HA, and HfO_2 films were measured by X-ray photoelectron spectroscopy (XPS), and the results are shown in Fig. 2(a). It can be seen that the Al composition (at.% $=2(1-x)/(5-2x)$) first increases and then decreases, and the maximum value near the CM-HA center is about 34.5%, while in HA and HfO_2 films the Al percentages are almost constant. The insets show the cross-sectional TEM images of S1, S2, and S3, indicating distinct interfaces of Si/tunneling layer, tunneling layer/CTL, and CTL/blocking layer. According to the previous report, the band gap of the $(HfO_2)_x(Al_2O_3)_{1-x}$ film can be adjusted by the Al (Hf) percentage in the film, which increases with increasing Al percentage in the film, while it decreases with decreasing Hf percentage.[13] So, a peak and valley shaped band gap should be formed due to the compositional distributions of Al in the CM-HA for S1. Hence, the band alignments for S1, S2, and S3 can be depict schematically as shown in Fig. 2(b).

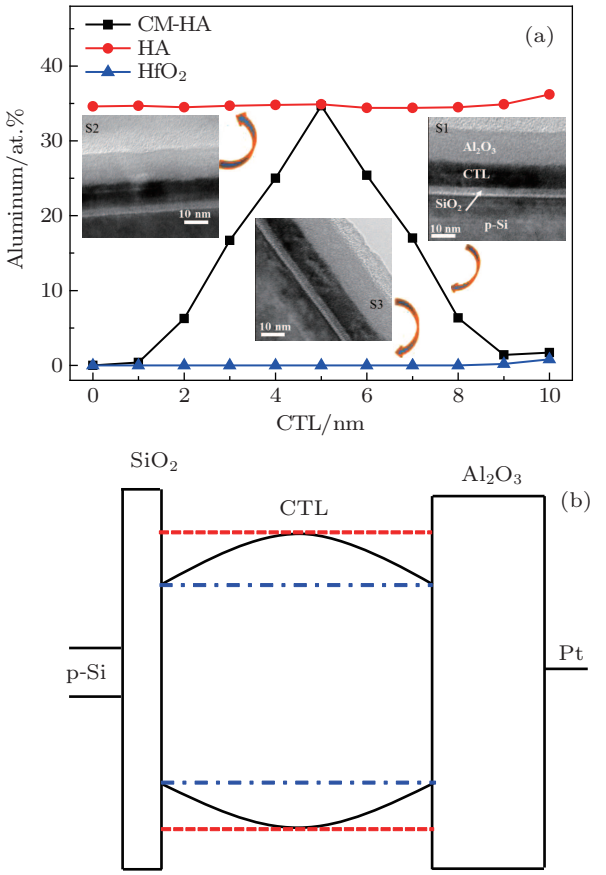


Fig. 2. (color online) (a) Al compositional distribution in the CTL. The insets show the cross-sectional TEM images of S1, S2, and S3. (b) Schematic energy band alignment for S1 (solid line), S2 (dotted line), and S3 (dash dotted lines).

The memory window ΔV_{FB} (flat-band voltage shift) can be extracted from the 1 MHz capacitance–voltage (C–V) curves under different sweeping voltages, and the results are shown in Fig. 3(a). The memory window of S1 is much larger than that of S2 and S3, indicating that a large number of electron traps exist in the CM-HA. The inset of Fig. 3(a) presents the C–V curve of S1 in a voltage sweep range of ± 12 V. It is found that the memory window is about 11.5 V. The injected electrons are first caught by the shallow trap levels and then migrate into the deeper ones through lateral hopping[14] due to the peak and valley shaped band gap, which increases the accessibility of the deep level traps. However, the memory window is reduced after post-deposition annealing due to the crystallization of HfO_2 CTL in S3.[15] The crystallization of films will generate grain boundaries, which can act as current leakage paths. Hence, there will be an increase in lateral conduction, which can result in poorer charge trapping.[11] To confirm the differences in charge trapping and storage behavior among the above three memory devices, the charge trap centroid (X_{cent}) from the metal/CTL interface is extracted via the constant current stress method by using the Pt/CTL/SiO_2/Si capacitors with the same CTL and tunneling layer thickness,[16]

which is expressed as

$$X_{\text{cent}} = t_{\text{OX}} \left(1 - \frac{\Delta V_{\text{g}-}}{\Delta V_{\text{g}+}}\right)^{-1}, \quad (1)$$

where t_{OX} is the thickness of the gate dielectrics, and $\Delta V_{\text{g}-}$ and $\Delta V_{\text{g}+}$ are the negative and positive gate voltage shifts, respectively. As shown in Fig. 3(b), X_{cent} shifts toward the opposite gate side as the sweeping voltage increases, whereas in S1, X_{cent} gradually shifts toward the CTL center as the sweeping voltage increases to $\pm$12 V. The results could be attributed to the peak and valley shaped potential barrier, which effectively prevents the injected electrons from moving to the gate side.

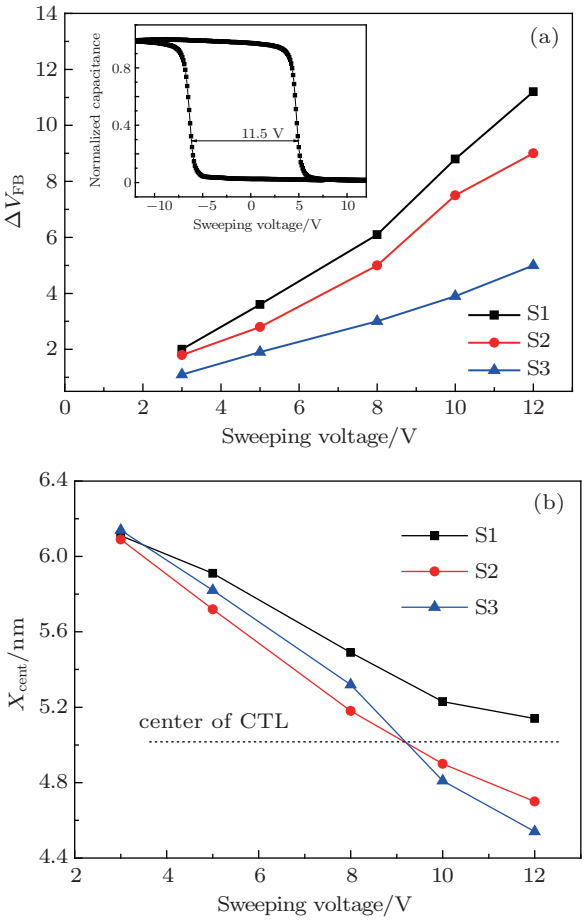


Fig. 3. (color online) (a) The hysteresis memory windows of S1, S2, and S3. The inset shows the *C*–*V* curve of S1 in a voltage sweep range of $\pm$12 V. (b) Dependences of charge trap centroid X_{cent} on the sweeping voltage.

The retention characteristics of the three CTFM devices were measured after 10^4 s at different temperatures, and the results are shown in Fig. 4. It is found that the slopes of charge loss below 50 °C are 0.03, 0.04, and 0.06, respectively, which exhibit only a weak dependence on temperature. However, at temperatures over 50 °C, the charge loss slopes for the S2 and S3 samples increase drastically with increasing temperature, indicating that the retention characteristics are much dependent on the temperature. However, the charge loss slope for the S1 sample only increases slightly compared with that in the lower temperature state (below 50 °C). It is known that the injected electrons are easily captured by the shallow level traps near the tunneling layer/CTL interface and the conduction band of the CTL, whereas for the deep level traps, they are buried underneath and may not be able to catch electrons easily.[17] In the retention state, trapping electrons into band (TB) tunneling and thermal excitation (TE) of electrons are the important charge loss mechanisms and jointly contribute to the charge loss for the memory device.[18] Below 50 °C, the TB tunneling is the dominant charge loss mechanism, which is not temperature sensitive, therefore, the electrons trapped by the shallow level traps can back tunnel to the Si substrate via the TB tunneling as shown in the inset of Fig. 4. The probability of the injected electrons tunneling back to the substrate is reduced for the S1 sample due to the higher barrier height between CTL/tunneling layer compared to that of S2 ($\Phi_{\text{S1}} > \Phi_{\text{S2}}$). As mentioned above, the poor retention characteristics of the S3 sample should be attributed to the crystallization of HfO_2. At an elevated temperature, the TE becomes a key charge loss mechanism: trapped electrons are thermally exited to the CTL conduction band, then tunnel back to the Si substrate. Since more deep level traps for charge storage exist in the CM-HA trapping layer for S1 due to its special band gap, the trapped charges are immune to the TE compared with S2 and S3. In addition, there is an internal electrical field in the retention state, which pushes the trapped electrons in the CTL toward the blocking and the tunneling layers, while the electrons are mainly confined in the left of the CTL due to the peak shaped potential barrier in the S1 sample. Since the out-tunneling current toward the blocking layer is effectively suppressed, as a consequence, the retention characteristic could be significantly improved.

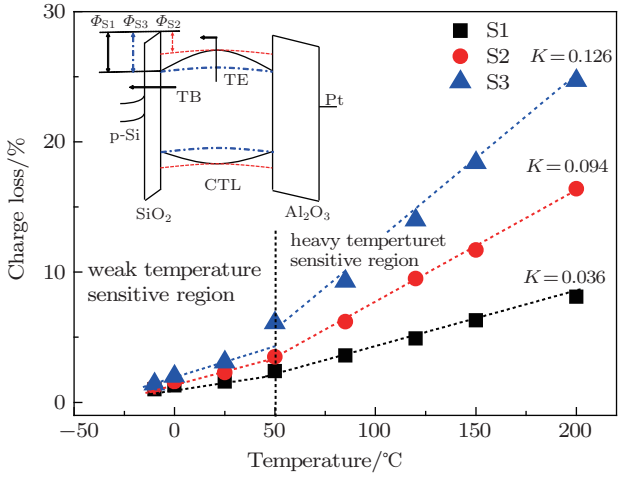


Fig. 4. (color online) Dependences of charge loss on the retention temperature. The inset shows the schematic energy band alignment diagram at the retention state for S1 (solid line), S2 (dotted line), and S3 (dash dotted line).

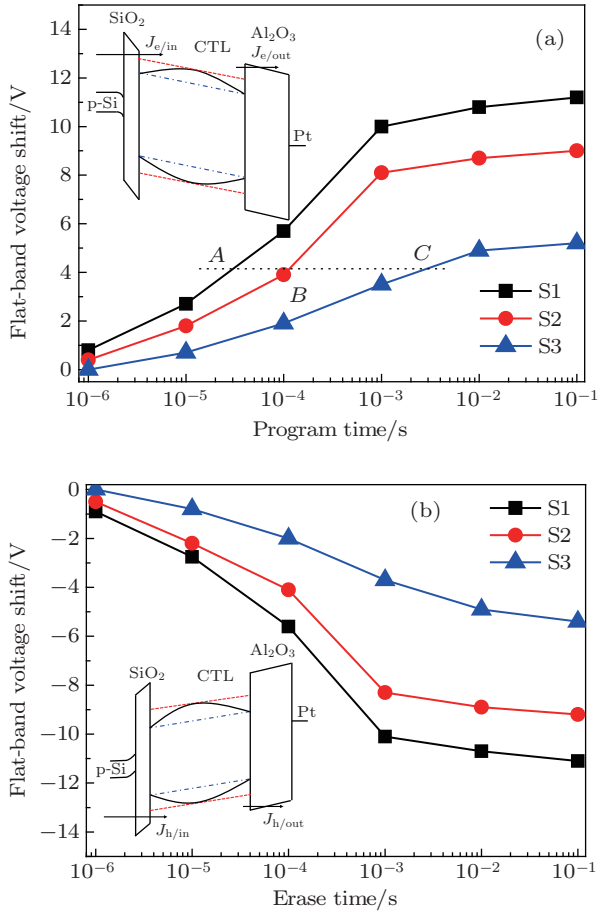


Fig. 5. (color online) Transient (a) program and (b) erase characteristics. The insets in panels (a) and (b) show the schematic energy band alignments at program and erase states, respectively (S1: solid line, S2: dottd line, S3: dash dotted line).

The comparison of program and erase transient characteristics among the above three memory devices is shown in Fig. 5 to demonstrate the effect of the peak and valley shaped band gap on the operating speed. The samples are charged at ±12 V by a single electrical pulse with different width. It is observed that S1 exhibits a faster program and erase speed than S2 and S3. For example, the program times at a memory window of 4 V for S1, S2, and S3 samples are 20 μs, 100 μs, and 3 ms (points *A*, *B*, and *C*), respectively, as shown in Fig. 5(a). The results can be explained by the band-gap diagram shown in the inset of Fig. 5(a). In a program transient state, the program speed depends on the dynamic equilibrium between the injected electron current $J_{e/in}$ and the out-tunneling electron current $J_{e/out}$ in the storage nodes of the trapping structure.[19,20] According to the results of X_{cent}, more electrons are trapped close to the blocking layer, which will greatly increase $J_{e/out}$ towards the blocking layer for S2 and S3, while in the S1 sample, the electrons are mainly confined in the left of the CTL due to the peak shaped potential barrier. The electron density near the blocking layer is correspondingly reduced, resulting in a smaller $J_{e/out}$ and a faster program speed for S1. For the erase state as shown in the inset of Fig. 5(b), the hole density is higher in the left of the CTL due to the existing of the valley shaped potential barrier for S1, resulting in a reduced out-tunneling hole current $J_{h/out}$ through the blocking layer and a fast erase speed compared with that of S2 and S3.

4. Conclusion

In summary, a high-*k* based charge trap flash memory with the composition modulated $(HfO_2)_x(Al_2O_3)_{1-x}$ charge trapping layer, SiO_2 tunneling layer, and Al_2O_3 blocking layer has been fabricated and investigated. A good trade-off among the memory window, program/erase speed, and data retention is achieved. The results are attributed to the special band-gap structure of the trapping layer. Based on this work, the charge trap flash memory device with composition modulated $(HfO_2)_x(Al_2O_3)_{1-x}$ trapping layer may offer promise as a potential candidate in future nonvolatile flash memory device applications.

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