Field plate structural optimization for enhancing the power gain of GaN-based HEMTs*

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A novel source-connected field plate structure, featuring the same photolithography mask as the gate electrode, is proposed as an improvement over the conventional field plate (FP) techniques to enhance the frequency performance in GaN-based HEMTs. The influences of the field plate on frequency and breakdown performance are investigated simultaneously by using a two-dimensional physics-based simulation. Compared with the conventional T-gate structures with a field plate length of 1.2 μm, this field plate structure can induce the small signal power gain at 10 GHz to increase by 5–9.5 dB, which depends on the distance between source FP and dramatically shortened gate FP. This technique minimizes the parasitic capacitances, especially the gate-to-drain capacitance, showing a substantial potential for millimeter-wave, high power applications.

Keywords: GaN-based HEMTs, breakdown characteristics, field plates, power gain

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1. Introduction

GaN-based high electron-mobility transistors (HEMTs) hold great promise for power electronics and radio-frequency (RF) applications due to their high breakdown field, high-mobility two-dimensional electron gas (2DEG), and good thermal stability. Field plate (FP) structures have been experimentally and theoretically demonstrated to be effective in the enhancement of the breakdown voltage by redistributing the electric field in the gate–drain access region[1–4] and suppressing the DC-RF dispersion.[5,6] More than 40 W/mm of output power density at 4 GHz was achieved with double FPs.[7] However, in general, the field plates suffer from a dramatic increase in parasitic capacitances, thus resulting in a degraded power gain.[8] In order to mitigate the undesired effect, a reduction in the extension of FP towards drain is of great necessity, although this will deteriorate the breakdown characteristics to some extent. Recently, several FP techniques have been presented to achieve better power–gain tradeoff characteristics, which include slant field plates,[9–11] source-connected FP placed on the second-layer insulator,[7,12,13] and multiple grating field plates (MGFPs).[14] Although a 3 dB higher power gain has been achieved experimentally by reducing gate-to-drain capacitance C_{gd},[13] these FP techniques have placed great emphasis on improving the off-state blocking capability. On the contrary, few reports on the FP design optimization for improving the frequency performance are available, despite the fact that the introduction of various FP designs becomes a main factor restricting the high frequency application.

In this paper, the profile of electric field in the conventional T-gate structure is examined, and an optimized FP structure is developed. This FP structure can be obtained by shortening the gate FP length and introducing an additional source FP. The physics-based simulation is implemented to illustrate the design concept, which combines the internal 2D electric field distribution, three-terminal breakdown behavior, and frequency response. The simulation results indicate that the inclusion of a source-connected FP can change the frequency behavior remarkably, whereas it has a limited influence on the breakdown characteristics.

2. Simulation conditions and FP-HEMT structures

The structures of FP HEMTs studied are shown in Fig. 1. The conventional T-gate structure (Fig. 1(a)) and the proposed source FP structure (Fig. 1(b)), which is comprised of a shortened gate FP and a source-connected FP, are mainly compared in the present work. An HEMT without any FP and an HEMT with double gate FPs are also simulated as references. Figure 1(c) shows the schematic cross section of double FP HEMTs. The first FP is the T-type one but with a much shorter FP length, while the second one can be connected to the source or gate electrode, accordingly, they are denoted as HEMTs with source FP and HEMTs with double gate FPs,

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respectively. Here L_{FP1} and L_{FP2} represent the corresponding FP lengths. In particular, D_{is} is defined as the separation between the two FPs (see Fig. 1(c)). The device characteristics are calculated using 2D device simulator Silvaco ATLAS.

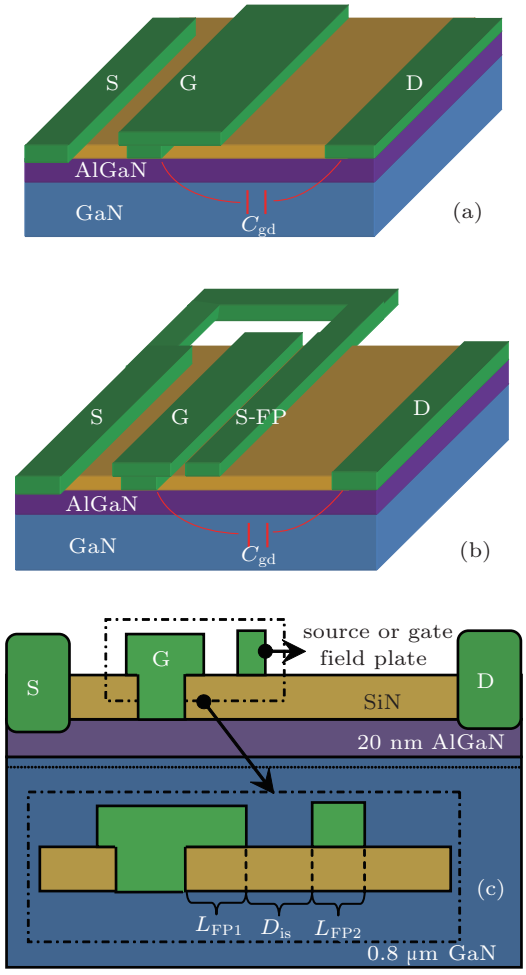


Fig. 1. (color online) (a) T-gate HEMT structure, (b) HEMT with source FP, and (c) schematic cross section of double FP HEMTs. The definition of D_{is} is also shown.

The detailed simulation conditions are as follows. The doping concentrations of AlGaN and GaN layers are assumed to be 1×10^{15} cm^{-3} and 1×10^{13} cm^{-3}, respectively. The electron mobility in the GaN buffer is assumed to be 1600 cm^2/Vs. The net charge due to spontaneous and piezoelectric polarizations is taken into account by employing positive sheet charge $\sigma_{pol} = 1\times10^{13}$ cm^{-2} at the interface between AlGaN and GaN. The trap states at the interface between the passivation film and the semiconductor and in the semiconductor bulk are not modeled, so the DC-RF dispersion is out of consideration. The impact ionization is utilized for breakdown voltage calculations and modeled as $\alpha_0 \exp(-E_C/E)$ with $\alpha_0 = 2.9\times10^8$/cm and $E_C = 3.4\times10^7$ V/cm for GaN.[1] P-type doping is introduced into the GaN buffer to achieve a realistic leakage current level of around 1 mA/mm when the breakdown occurs. The breakdown simulation is conducted under off-state conditions with the gate biased at -6 V. Here, breakdown voltage V_{BR} is defined as the drain voltage for a drain current of 1 mA/mm. Beyond this point, a rapid increase in leakage current is observable due to the avalanche breakdown.

In addition, the parameters for frequency response simulation are carefully extracted from in-house 100 μm AlGaN/GaN HEMTs by using the standard small signal extraction method.[15] Parasitic resistances and inductances are given bellow: $R_{IN} = 4.75$ Ω, $R_{OUT} = 5.6$ Ω, $R_{GORUND} = 1.24$ Ω, $L_{IN} = 6.27\times10^{-11}$ H, $L_{OUT} = 6\times10^{-11}$ H, and $L_{GROUND} = 6.27\times10^{-12}$ H. Insignificant parasitics are necessary for the exclusive consideration of the influence of FP structure on the frequency response.

Unless otherwise stated, the devices have the same designed physical dimensions, each with a gate length of 0.3 μm, a gate–source distance of 1.5 μm, and a gate–drain spacing of 3.2 μm. Besides, for the frequency simulation, a gate width of 100 μm is utilized. Under these conditions, the pinchoff voltage is -3.2 V. A maximum transconductance of 265 mS/mm is obtained at $V_{gs} = -1.4$ V, where a current gain cutoff frequency (f_T) of 35 GHz is deduced from simulated $|h_{21}|$ for a device without any FPs.

3. Breakdown characteristics

An FP over the gate electrode towards the drain electrode is successfully employed to boost the breakdown characteristics by managing the electric field profile in the gate–drain access region. The effects of critical geometrical variables (FP length, insulator thickness, and gate–drain distance) on V_{BR} have been examined systematically in Ref. [1]. As demonstrated in the paper, for a specific insulator thickness combined with a fixed gate–drain separation, there is an optimized L_{FP} beyond which V_{BR} no longer increases. Accordingly, in our simulation, with an 80 nm Si_3N_4 under the FP, an FP length of 0.5 μm leads to a maximum V_{BR} of 325 V in the T-gate structure, as shown in Fig. 1(a).

A further analysis into the electric field distribution of the device with a single 0.5 μm gate FP at the interface between AlGaN and Si_3N_4 is carried out. Obviously, two electric field peaks are observed at the gate edge and FP edge when the simulation is performed at $V_{ds} = 50$ V (see square symbols in Fig. 2(a)). However, it should be noted that the integration area under the electric field curve between the two peaks contributes little to the total area, from which we are encouraged to remove the metal electrode between these two peaks so that double gate-FP HEMTs (as shown in Fig. 1(c)) are formed. Interestingly, a slight difference between the two devices is indeed observed probably due to the strong electrostatic coupling effect between the two gate FPs as compared in Fig. 2(a), which supports the proposed concept about the separation of a single T-type FP into two spatially isolated FPs.

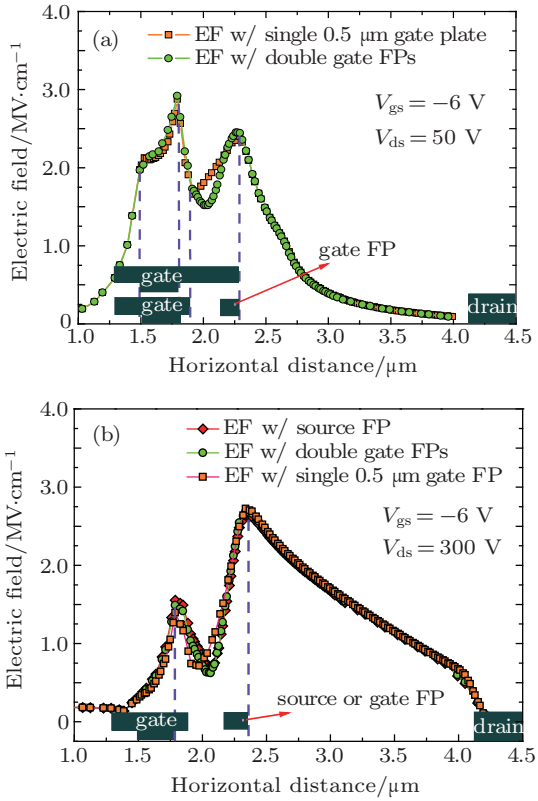


Fig. 2. (color online) (a) Comparison of simulated electric field distribution between 0.5 μm gate-FP HEMTs and double gate-FP HEMTs at the interface between AlGaN and Si_3N_4 at $V_{ds} = 50$ V. (b) Simulated electric fields in the GaN channels for devices with 0.5 μm gate FP, double gate FPs, and source FP at $V_{ds} = 300$ V. Here D_{is}, L_{FP1}, and L_{FP2} are 0.25 μm, 0.12 μm, and 0.13 μm, respectively. The thickness of Si_3N_4 dielectric under the field plate is 80 nm.

Moreover, due to the small potential difference between the source and the gate electrodes, a device with the second plate connected to the source (namely, source FP) instead of the gate is then proposed (Fig. 1(b)). Figure 2(b) shows the electric field distributions in the GaN channels of these three FP-HEMT structures, where the maximal electric fields all occur at the second FP edge. The simulations are performed at V_{ds}=300 V. The Si_3N_4 passivation under the field plate has a thickness of 80 nm. Similar magnitudes of the peak electric fields can be clearly seen in all FP-HEMTs. Further, the same breakdown voltage is achieved as confirmed by the simulated off-state breakdown curve (see Fig. 3). The discrepancy in the drain leakage prior to the avalanche breakdown is believed to be due to a minimal difference in peak electric field at the gate edge (as shown in Fig. 2(b)).

When we attemtp to enhance the frequency characteristics using FP designs, the slightest degradation in the electric field distribution is highly desirable. This is not only because the electric field in the GaN channel deteimines the breakdown characteristics, but also the electric field at the interface between the barrier layer and the passivation dielectric has a critical influence on the gate lag characteristic.[16] Besides, the simulations above demonstrate that the three FP HEMTs have almost the same breakdown characteristics, indicating that the tradeoff characteristics between breakdown voltage and frequency response can be achieved by using the proposed source FP and double gate FPs structures.

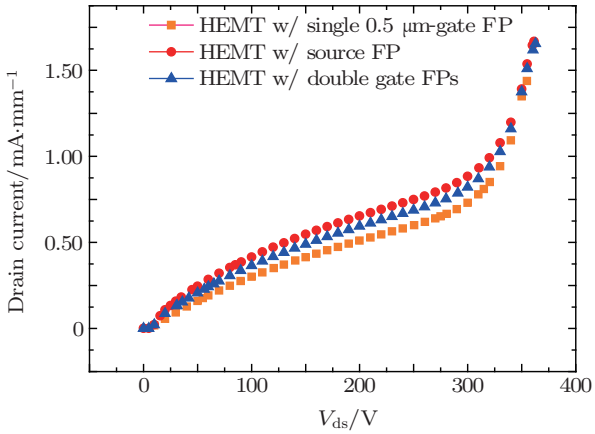


Fig. 3. (color online) Simulated off-state *I*–*V* characteristics for devices with 0.5 μm gate FP, source FP, and double gate FPs.

4. Small signal gain characteristics

To investigate the effect of FPs on the frequency response, a small signal RF analysis is carried out, with frequency ramped from 2 GHz to 70 GHz. The current gain (h_{21}), the maximum stable gain (MSG), and the maximum available gain (MAG) are calculated for all devices. The device parameters including gate-to-drain capacitance C_{gd} and total gate capacitance C_g are extracted to gain an insight into the physical basis.

Figure 4(a) shows the frequency dependences of the small-signal gain calculated at a gate bias of −1.4 V and a drain bias (V_{ds}) of 20 V. The gate bias is chosen so that the same maximum g_m is reached for all the three HEMTs. The three structures are HEMTs without FP, HEMTs with source FP, and HEMTs with 0.5 μm gate FP. The device dimensions and the SiN thickness used are the same as those in Fig. 2. The HEMTs with double gate FPs show gain characteristics the same as those of the HEMTs with 0.5 μm gate FP, which may be due to the fact that both HEMTs at the bias point have almost the same electric field shapes (not shown). This indicates that the double gate FP structure is not an option for power gain enhancement. The gain characteristics as a function of frequency are plotted in Fig. 4(a). At 10 GHz, the values of $|h_{21}|$ in these three structures are 11.6 dB, 6.5 dB, and 4.88 dB, and the values of MSG are 17 dB, 20.17 dB, and 13.38 dB, respectively. As can be clearly seen, the introduction of the 0.5 μm gate FP leads to the worst gain characteristics. In contrast, the inclusion of the source FP enables the power gain to increase by 6.79 dB compared to that of the HEMT with gate FP. This significant enhancement in power gain can be attributed to the shrinking of the gate FP length (3.62 dB higher) and the shielding effect induced by the source FP (3.17 dB higher).

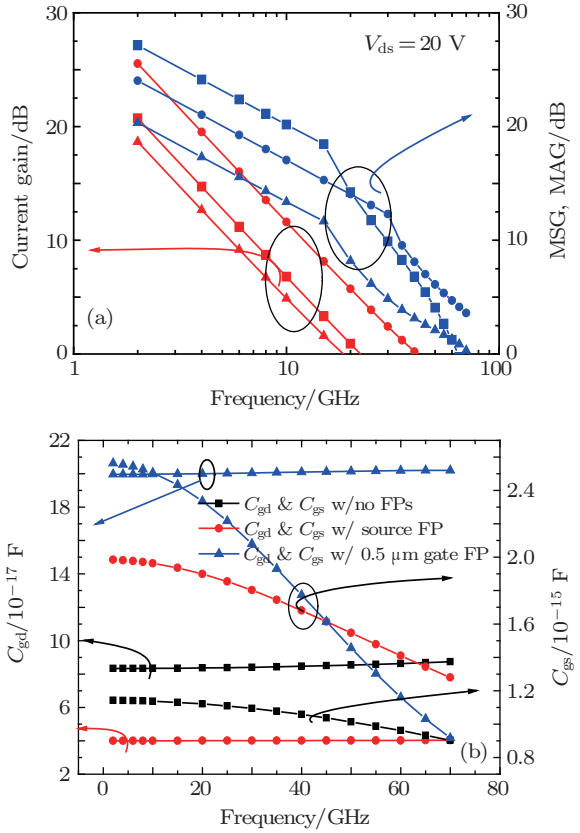


Fig. 4. (color online) (a) Simulated current gains and power gains (MSG/MAG). Dot line represents HEMTs without FP, square line denotes HEMTs with source FP, and triangle line refers to HEMTs with 0.5 μm gate FP. (b) C_{gs} and C_{gd} as a function of frequency.

The frequency dependences of simulated C_{gd} and C_g are shown in Fig. 4(b). It can be obviously observed that C_{gd} is one order of magnitude smaller than C_g. As C_g is the sum of C_{gd} and C_{gs}, $|h_{21}|$ is mainly determined by C_{gs}. Therefore, while the current gain with the source FP is higher than that with the 0.5 μm gate FP, the introduction of additional C_{gs} due to the interaction between gate electrode, gate FP and source FP is truly responsible for the 5 dB smaller current gain compared to that of the devices without FP. Nevertheless, it should be noted that the HEMT with source FP exhibits an increase of 6.8 dB in power gain. As illustrated in Fig. 4, the C_{gd} of HEMTs with source FP shows approximately one fifth that introduced by the 0.5 μm gate FP at 10 GHz. Given the values of C_{gd} obtained in different structures, the quantitative difference in power gain can be fully explained using MSG (dB) $\approx 10\log|g_m/(\omega C_{gd})|$, where the values of g_m are identical for the three devices. Hence, we believe that this improvement on gain can be attributed to the fact that the reduction in C_{gd} leads to better isolation between input and output ports, thereby improving the power gain (as denoted in Fig. 1).

To further confirm our developed concept of optimized FP structures for enhancing the power gain, we also investigate the variation of frequency response with D_{is}. With 200 nm-thickness Si_3N_4, the breakdown voltage is saturated at the FP length of 1.2 μm. As exhibited in Fig. 5(a), the peak electric field at the gate edge relaxes slightly as D_{is} decreases, whereas the electric field at the source FP edge shows an opposite trend. Despite that, there is no significant difference in electric field shaping among these curves, therefore leading to a similar breakdown voltage as demonstrated above. When D_{is} = 0.25 μm, the electric field distribution of the source FP HEMTs closely resembles that of the 1.2 μm gate FP HEMTs.

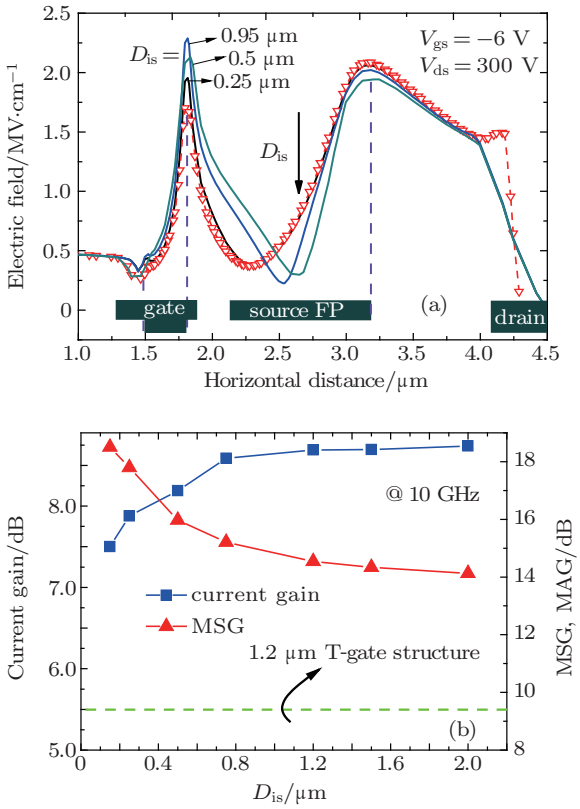


Fig. 5. (color online) (a) Simulated electric field distributions versus D_{is} at V_{ds} = 300 V, where L_{FP1} = 0.12 μm, $L_{FP1}+D_{is}+L_{FP2}$ = 1.2 μm. Triangle line denotes the electric field of the conventional 1.2 μm T-gate structure. (b) Small single gain versus D_{is} simulated at 10 GHz. Dashed line at the bottom represents gains of 1.2 μm T-gate structure as a reference, with a current gain of 5.5 dB and an MSG of 9.5 dB.

There is an obvious nonlinear relationship between D_{is} and the current/power gain (see Fig. 5(b)). When D_{is} exceeds 0.4 μm, a rapid reduction in power gain and a dramatic increase in current gain are simultaneously observed. In this case, L_{FP1} remains constant (0.12 μm) and only L_{FP2} is adjusted to keep the location of the source-FP edge fixed. Hence, both substantial changes can be ascribed to the continuously weakening shielding effect from the source field plate because of the increasing gap between the source FP and the gate electrode. When D_{is} approaches to 2.0 μm, the HEMT shows only 3% difference in gain characteristic as compared with the gate FP HEMT with L_{FP1} = 0.12 μm which has a power gain of 13.8 dB and a current gain of 8.75 dB at 10 GHz. This indicates that the shielding effect no longer acts when D_{is} is beyond 2 μm. For comparison purpose, the gain characteristics of a device with 1.2 μm gate FP are also shown at the bottom of

Fig. 5(b). Therefore, a shorter length of the gate FP is responsible for the increase of 5 dB in power gain, and a source FP with $D_{is} = 0.15$ adds an additional increase of 4.5 dB. It can be concluded that the gain improvement should be partially due to the minimization of the parasitic capacitance caused by the gate FP and partially due to the shielding effect introduced by the source FP.

5. Summary

Based on a probe into the conventional gate FP structures, two FP structures are creatively developed, which are double gate FPs and source FP structures. As far as we know, for the first time, both electric field and frequency characteristics are simultaneously compared based on physics-based simulations, which presents us with a theoretical perspective into the device operation. For the proposed source FP HEMTs, different degrees of enhancement in gain characteristic can be obtained with a minimal degradation of breakdown characteristics, which depends on the FP separation D_{is}. However, no improvement on gain characteristics is observable for double gate FPs. In addition, the source FP structure as a module can be integrated into a multilayer-FP structure to further improve the device characteristics. Simulation results imply that this FP design can realize the possibility of achieving both high breakdown voltage and high frequency characteristics.

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