High-performance 4H-SiC junction barrier Schottky diodes with double resistive termination extensions*

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4H-SiC junction barrier Schottky (JBS) diodes with a high-temperature annealed resistive termination extension (HARTE) are designed, fabricated and characterized in this work. The differential specific on-state resistance of the device is as low as 3.64 mΩ·cm^2 with a total active area of 2.46×10^{-3} cm^2. Ti is the Schottky contact metal with a Schottky barrier height of 1.08 V and a low onset voltage of 0.7 V. The ideality factor is calculated to be 1.06. Al implantation annealing is performed at 1250 °C in Ar, while good reverse characteristics are achieved. The maximum breakdown voltage is 1000 V with a leakage current of 9×10^{-5} A on chip level. These experimental results show good consistence with the simulation results and demonstrate that high-performance 4H-SiC JBS diodes can be obtained based on the double HARTE structure.

Keywords: 4H-SiC, junction barrier Schottky (JBS) diode, high-temperature annealed resistive termination extension (HARTE)

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1. Introduction

Silicon carbide (SiC) is very useful for power devices, especially in the high-voltage and high-temperature environments,[1–3] because of its high breakdown electric field (2×10^6–4×10^6 V/cm), high thermal conductivity (4.9 W/cm·K), and excellent reliability, which allow SiC power devices to have thinner and higher doped epitaxial layers than Si-based devices. As a result, much lower series resistance and power dissipation can be achieved. Among all polytypes, 4H-SiC is the most attractive one for its high electron mobility and large bandgap. Unipolar current conduction is more preferred for rectifiers because there is no reverse recovery current when the device is switched from the on-state to the off-state, which can improve switch frequency and reduce power losses. The most commonly used unipolar power diode is the Schottky rectifier that utilizes a metal–semiconductor barrier to produce current rectification. To further reduce the reverse leakage current and improve the blocking voltage, junction barrier Schottky (JBS) diodes have been widely used in the fabrication of SiC power devices. The forward conduction is determined by the Schottky contact as long as a low forward drop is realized, and the reverse leakage is controlled by the p–n junction. Besides, the switching speed of the device is still fast as the current is supplied predominantly by Schottky injection at low forward bias, and there is no minority carrier charge storage.

However, the devices suffer electric field crowding at high reverse voltage, which dramatically reduces the blocking voltage of the device. Among several different kinds of edge terminations, such as field plate (FP),[4] floating metal ring (FMR),[5] junction termination extension (JTE),[6] and multi-step junction termination extension (MJTE),[7] the JTE is the most effective one to improve the breakdown voltage of the device. However, the JTE structure requires high-temperature annealing (1600–1700 °C) to activate the P-type implant in the JTE region. The process is costly and does not match with the existing Si-based process line.

Another type of edge termination ring is the resistive termination extension (RTE), which utilizes either P-type[8] or neutral implants[9] without activation to create a highly damaged resistive layer at the surface. However, their leakage currents are much higher than those of the devices with JTE structures, which may be caused by severe lattice damage after high energy implantation. In this work, 4H-SiC JBS diodes with double high-temperature annealed RTE (HARTE) layers are designed, fabricated, and characterized. The HARTE layers are prepared by Al implantation and subsequent 1250 °C annealing, which effectively repairs the implant damage and reduces the leakage current. The devices show good forward and reverse characteristics.

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2. Simulation

Before the fabrication of SiC JBS diodes, four different HARTEs are designed and simulated. The simulation is performed by Sentaurus version E-2010.12-SP1. The forward and reverse *I*–*V* characteristics of the device can be simulated by setting proper physical model in the simulation. The HARTE regions are formed by Al implant doping. As the activation rate of Al is extremely low, we set this value to be 1% in the simulation. The active concentration of Al is set to be 1×10^{16} cm^{-3} and the concentration of Al implant without activation is set to be 9.9×10^{17} cm^{-3} in the HARTE regions. The thickness and doping concentration of the n$^-$ epilayer used in the simulation are 10.4 μm and 3.8×10^{16} cm^{-3}, respectively, which are the same as the materials used in the experiment.

The two-dimensional equal electric potential profiles at breakdown point are demonstrated in Figs. 1(a)–1(d). Figure 1(a) shows a JBS device without an HARTE structure. The device suffers from pre-breakdown caused by electric field crowding at the edge of the contact. In Fig. 1(b), an HARTE-1 is added and the electric field crowding is effectively reduced. The implantation temperature of the HARTE layer is selected so that most of the lattice damage can be repaired but the dopant is not fully activated, which creates a high density of deep traps in the HARTE regions. As a result, a small lateral leakage current is permitted to flow into the 4H-SiC substrate at the blocking state causing a lateral potential drop which reduces the electric field crowding. When the HARTE-2 is added, the depletion region area increases. Thus, higher breakdown voltage is expected. The depletion region in Fig. 1(c) is larger than that in Fig. 1(d). Thus, the structure shown in Fig. 1(d) is expected to have the largest breakdown voltage. Figure 1(e) shows that the electric field of the p–n junction in the active area is about 1.5×10^6 V/cm when the breakdown happens in Fig. 1(a), while the electric field of the p–n junction in the active area increases to 3×10^6 V/cm when the breakdown happens in Figs. 1(b)–1(d), which are due to the higher breakdown voltage in Figs. 1(b)–1(d).

In addition, the one-dimensional distributions of the absolute value of the electric field parallel to the *x* axis in the field plate oxidation layers at the breakdown point are illustrated in Fig. 1(f), in which the electric fields of Figs. 1(b)–1(d) are much higher than that in Fig. 1(a). This is also due to higher breakdown voltages in Figs. 1(b)–1(d). However, the maximum electric fields in the field plate oxidation layers are about 4.5×10^6–5.5×10^6 V/cm when the devices are broken down, which is far from the critical breakdown electric field (1×10^7 V/cm) of SiO_2. Therefore, the safety of the field plate oxidation layer can be ensured until avalanche breakdown occurs in the device.

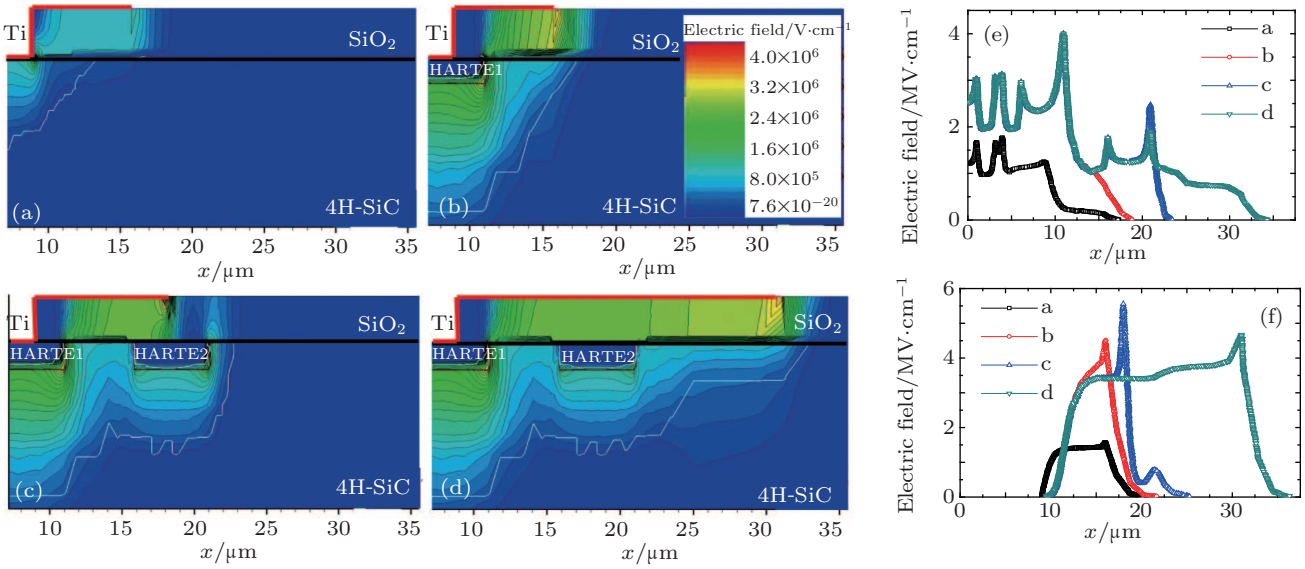


Fig. 1. (color online) The simulation results of the two-dimensional equal electric potential lines of four devices with different HARTE designs: (a) without an HARTE; (b) with only one HARTE ring; (c) with two HARTE rings and the metal edge overlapped part of HARTE-2; (d) with two HARTE rings and the metal edge outstripping that of HARTE-2 by 5–15 μm. (e) The electric field distributions at the p–n junction point vertical to the *y* axis of the four different HARTE designs at the breakdown point. (f) The electric field distributions in the field plate oxidation layers at the breakdown point.

The leakage current can be reduced by narrowing the Schottky regions, but this can also result in increasing forward voltage drop.[6] The reason lies in the simulation results of the two-dimensional electrostatic potential distributions of the devices with different widths of Schottky regions, as demonstrated in Fig. 2. The widths of p$^+$ regions and Schottky regions are 2 μm and 0.5 μm in Fig. 2(a), while 2 μm and 1 μm in Fig. 2(b). Figure 2(c) shows the one-dimensional electrostatic potential distribution curves extracted from Figs. 2(a) and 2(b) in the Schottky regions in the vertical direction when the Schottky contact and Ohmic contact both with a bias of 0 V. As the widths of the Schottky regions decrease from

1 μm to 0.5 μm, the depletion regions are connected with each other, as shown in Fig. 2(a). As a result, the electrostatic potential of the Schottky regions adjacent to the p^+ regions decreases, which leads to a negative electric potential difference of −1.3 V (see Fig. 2(c)) between surface and the substrate, resulting in the increase in the onset voltage.

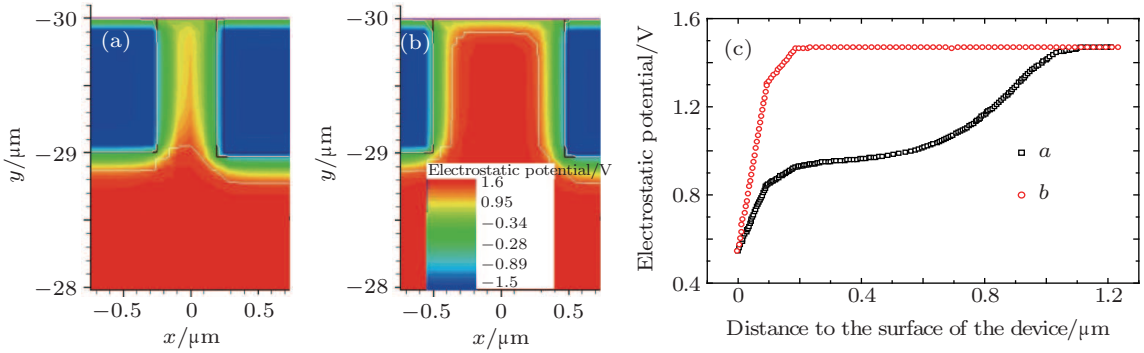


Fig. 2. (color online) The simulation results of the two-dimensional electrostatic potential distributions of the devices with different Schottky region widths. (a) The width of p^+ region and the width of Schottky region are 2 μm and 0.5 μm, respectively; (b) the width of p^+ region and the width of Schottky region are 2 μm and 1 μm, respectively; (c) the one-dimensional electrostatic potential distribution curves extracted from panels (a) and (b) in the Schottky regions in the vertical direction when both the Schottky contact and Ohmic contact with a bias of 0 V.

The forward *I*–*V* characteristics of the devices with different Schottky contact widths are demonstrated in Fig. 3(a). The width of the p^+ region is set to be 2 μm according to the etching precision. The device is not turned on even at a forward voltage of 2.5 V when the Schottky contact width is 0.5 μm, which confirms the prediction stated above. Other devices with Schottky contact widths of 1–6 μm show similar forward characteristics. As no current passes through the p^+ region at low forward voltage (0–3 V), the devices with the same total area but different p^+ region areas show differences in their forward current values.

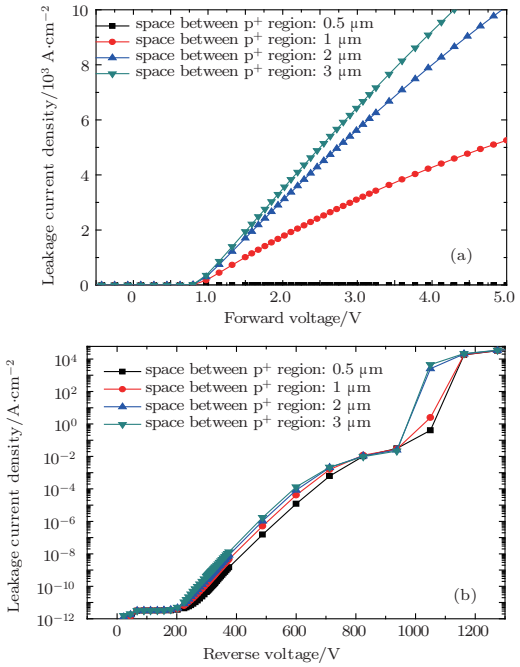


Fig. 3. (color online) Simulation results of the forward and reverse *I*–*V* characteristics of the devices with different Schottky contact widths, while the width of the p^+ region is designed to be a constant of 2 μm.

Figure 3(b) shows the simulation results of the reverse *I*–*V* characteristics of devices with different Schottky contact widths. Higher leakage current as well as lower breakdown voltage is obtained as Schottky contact width increases. The p^+ regions become closer to each other as the Schottky contact width decreases, which makes the spacing between p–n junctions better pinched-off in the blocking state, thereby shielding the surface of the devices better. Thus, lower leakage current and higher breakdown voltage can be expected.

In summary, the Schottky contact width should be selected properly as a trade-off between the forward voltage drop and the leakage current. According to these simulation results as well as the etching precision, the JBS implanted p^+ widths and the Schottky contact widths between the implanted p^+ regions are designed to be (2 μm, 2 μm), (2 μm, 3 μm) or (2 μm, 4 μm).

3. Design and fabrication

The 4H-SiC homoepilayers are grown by using a warm-wall AIX 2800G4 WW planetary reactor on 4-inch n^+ doped (0 0 0 1) 4H-SiC substrates with 4° off-axis toward (11-20) obtained from Cree Research Inc. The thickness and doping concentration of the n^- epilayer are 10.4 μm and 3.8×10^{16} cm^{-3} respectively. The implanted p^+ widths and the Schottky contact widths between the implanted p^+ regions of the SiC JBS diodes are designed to be (2 μm, 2 μm), (2 μm, 3 μm), or (2 μm, 4 μm), which are denoted as D1, D2, and D3. The spacing between HARTE-1 and HARTE-2 and the spacing between the outer edge of the Schottky contact metal and the inner edge of HARTE-2 are designed to be (5 μm, 15 μm), (4 μm, 15 μm), (5 μm, 2 μm) or (4 μm, 2 μm). The p^+ region is implanted with Al to a concentration of 1×10^{18} cm^{-3} and a depth of 0.5 μm. The area of

the active region is 2.46×10^{-3} cm^2 and that of the termination region is 1.38×10^{-3} cm^2, resulting in a total chip size of 3.84×10^{-3} cm^2.

The HARTE regions are formed simultaneously with the p^+ region through a multi-step Al implantation process. The implantation annealing is performed at 1250 °C for 4 h in Ar ambient. X-ray diffraction (XRD) and secondary ion mass spectroscopy (SIMS) are used to analyze the cure of the lattice damage caused by the implanted Al and the activation rate of the implanted Al. SiO_2 layer with a thickness of 1 μm is used as the field plate oxidation layer, which is formed by a low-pressure chemical vapor deposition (LPCVD) process. Ti is used as the Schottky contact metal while Ni is used as the Ohmic contact metal. The forward and reverse characteristic curves are measured by using an Agilent B1500A and a Tektronix 370A.

4. Results and discussion

The results of XRD and SIMS are demonstrated in Figs. 4(a)–4(d). The SiC sample shows only one peak with a full width at half maximum (FWHM) of 26.68 before it is implanted. The FWHM of the sample increases to 34.4, and another peak emerges after the sample is implanted by high-energy Al ions, which may be caused by the lattice damage. The FWHM restores to 27.8 and the damage-caused peak disappears after the sample is annealed. These results show that after the sample is annealed at 1250 °C for 4 h, the lattice damage produced by the high-energy Al implantation is almost cured. However, figure 4(d) shows that the distributions of Al do not show much difference before and after the sample is annealed. This means that there is hardly any diffusion of the implanted Al, which demonstrates most of the implanted Al ions are not activated.

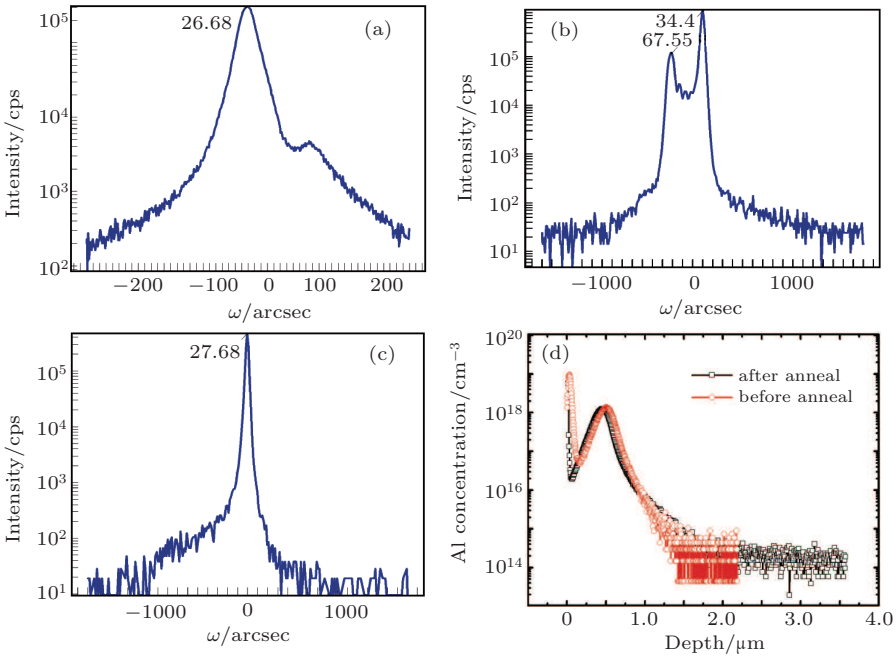


Fig. 4. (color online) Results of the XRD of the SiC sample (a) before and (b) after being implanted with Al ions and (c) after being annealed. (d) The comparison of the results of SIMS before and after the Al-implanted SiC sample is annealed.

The cross sections of the devices and a top view of a finished die are shown in Fig. 5. As illustrated in Fig. 5, *a* represents the spacing between HARTE-1 and HARTE-2, and *b* denotes the spacing between the outer edge of the Schottky contact metal and the inner edge of HARTE-2. In Fig. 5(a), *b*=2 μm, and the field plate edge is within HARTE2. In Fig. 5(b), *b*=15 μm, and the outer edge of field plate stretches beyond HARTE2. Figure 5(c) shows a top view of a finished die captured by a light microscope. The values of (*a*, *b*) are (5 μm, 15 μm), (4 μm, 15 μm), (5 μm, 2 μm), and (4 μm, 2 μm) for J1, J2, J3, and J4, respectively. The implanted p^+ widths and the Schottky contact widths between the implanted p^+ regions for J1, J2, J3, and J4 are all designed to be (2 μm, 2 μm). The reverse *I*–*V* characteristics of J1, J2, J3, and J4 are shown in Fig. 6. J1 and J2 have higher blocking voltages than J3 and J4 because their extended Schottky contact metal increases the depletion region area under high reverse voltage, as shown in Fig. 1, thus increasing the breakdown voltage.

However, the extended length should not be too long in case the HARTE regions are too far from the Schottky contact edge to prevent the electric field crowding in the blocking state. J1 has higher leakage current than J2, while J3 has higher leakage current than J4 because wider spacing between HARTE-1 and HARTE-2 may weaken the pinch-off of the spacing between HARTE-1 and HARTE-2, which would become the channel of larger leakage current. Above all, J2 with $a = 4$ μm and $b = 15$ μm has the best reverse characteristic.

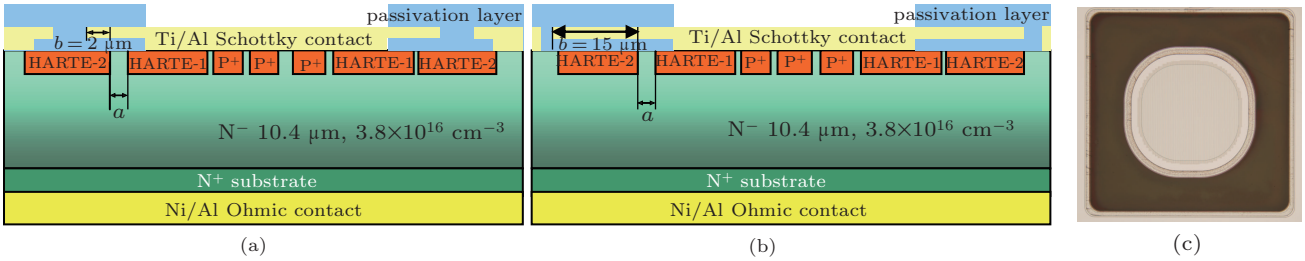


Fig. 5. (color online) (a) and (b) Cross-section illustrations of the fabricated devices with two different kinds of designs. a represents the spacing between HARTE-1 and HARTE-2, and b denotes the spacing between the outer edge of the Schottky contact metal and the inner edge of HARTE-2. The width of HARTE-2 is designed to be 5 μm. In Fig. 5(a), b=2 μm, the field plate edge is within HARTE2. In Fig. 5(b), b = 15 μm, the outer edge of field plate stretches beyond HARTE2. (c) A top view of a finished die captured by using a light microscope.

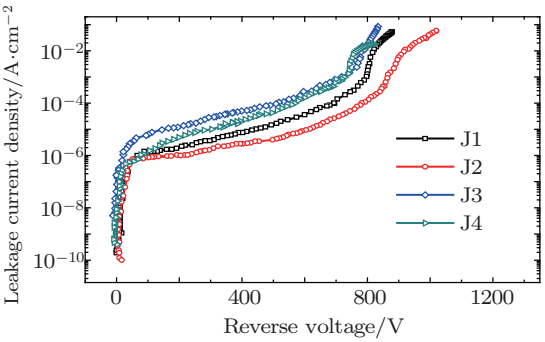


Fig. 6. (color online) Reverse $I-V$ characteristic curves of four devices with different HARTE designs, where the implanted p^+ width and the Schottky contact width between the implanted p^+ regions of the SiC JBS diodes are designed to be 2 μm and 2 μm, respectively. The spacings between HARTE-1 and HARTE-2 are 5, 4, 5, and 4 μm for J1, J2, J3, and J4, respectively. The outer edges of the Schottky contact metal exceed the inner edges of HARTE-2. They are 15, 15, 2, and 2 μm, respectively, for J1, J2, J3, and J4.

The forward and reverse characteristics of J2 are demonstrated in Fig. 7. The current density is restricted to 1×10^{-6} A/cm^2 by the measurement limit of the instrument at a forward voltage lower than 0.3 V. The forward current density achieves 180 A/cm^2 at $V_f = 1.5$ V. The leakage current densities are 5.0×10^{-3} and 3×10^{-2} A/cm^2 under high reverse voltages of 900 and 1000 V, respectively. Besides, the forward and reverse characteristics of D1, D2, and D3, whose implanted p^+ widths and Schottky contact widths between the implanted p^+ regions are designed to be (2 μm, 2 μm), (2 μm, 3 μm), and (2 μm, 4 μm), respectively, are illustrated in Fig. 8. The values of (a,b) are set to be (5 μm, 15 μm) for D1, D2, and D3. As the Schottky contact widths become larger sequentially from D1 to D3, while their implanted p^+ widths are all set to be 2 μm, the devices have higher forward current densities and higher leakage currents as well as lower breakdown voltage, as demonstrated in Fig. 8. This is because the increased Schottky contact width makes the p^+ regions separate farther from each other, which makes the pinched-off of the spacing between p–n junctions weaker in the blocking state. The same tendency is also observed in the simulation results (see Fig. 3).

The maximum breakdown voltage measured for the JBS diode is 1000 V with a leakage current of 9×10^{-5} A for chip level, as indicated in Fig. 7(b). The current density of the device with an active area of 2.46×10^{-3} cm^2 is as large as 180 A/cm^2 at $V_f = 1.5$ V, and it is 472 A/cm^2 at V_f=2.6 V, as shown in Fig. 7(a), corresponding to a differential specific on-state resistance of 3.64 mΩ·cm^2. The figure of merit (FOM), which is described as $V_B^2/R_{on,sp}$, of the device is calculated to be 275 MW/cm^2. The HARTE design of the device makes full use of the advantages of 4H-SiC.

The Schottky barrier height can be expressed as

$$\Phi_{Bn} = \frac{kT}{q}\ln\left(\frac{A^{**}T^2}{J_s}\right), \tag{1}$$

where k is Boltzmann's constant, T is the absolute temperature, A^{**} is the effective Richardson constant, and J_s is the extrapolated value of current density at zero voltage. The Φ_{Bn} is calculated to be 1.08 V by use of $q = 1.6\times10^{-19}$ C, $T = 300$ K, $k = 1.38\times10^{-23}$ J/K, and $J_s = 1.24\times10^{-11}$ A, which is acquired from Fig. 7(a).

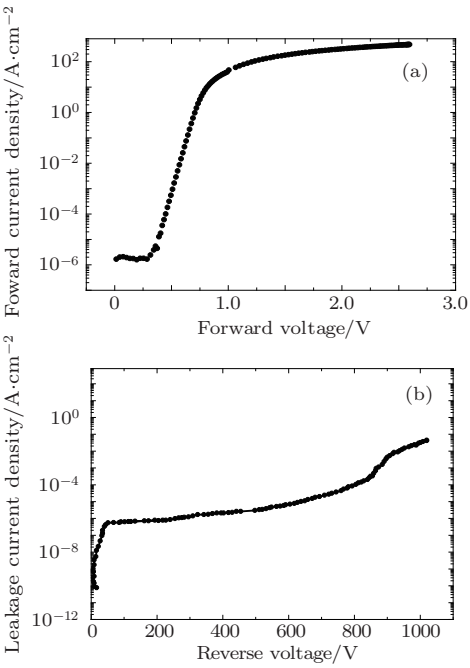


Fig. 7. (a) Forward and (b) reverse characteristics of J2. The implanted p^+ width and the Schottky contact width between the implanted p^+ regions of J2 are designed to be 2 and 2 μm, respectively. The spacing between HARTE-1 and HARTE-2 is 4 μm, and the outer edge of the Schottky contact metal exceeds the inner edge of HARTE-2, i.e., 15 μm.

Another important parameter is the ideality factor η, which can be extracted from the forward $J-V$ characteristic

curve of the device (see Fig. 7(a)) as

$$\eta \equiv \frac{q}{kT}\frac{\mathrm{d}V}{\mathrm{d}(\ln J)}. \tag{2}$$

According to Fig. 7(a), $\mathrm{d}V/\mathrm{d}(\ln J)$ should be extracted from the linear part of the curve. $\ln J = -6.53$ at $V_\mathrm{f} = 0.51$ V and $\ln J = -3.25$ at $V_\mathrm{f} = 0.6$ V. When $T = 300$ K, $\eta = 1.06$.

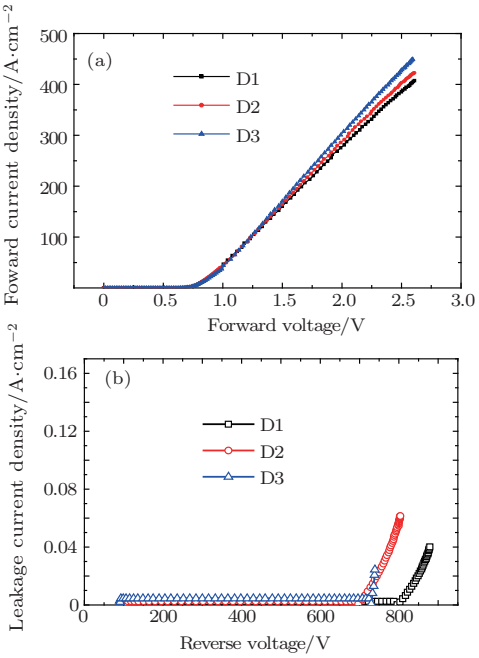


Fig. 8. (color online) Comparison of (a) the forward and (b) the reverse characteristics between D1, D2, and D3. The spacing between HARTE-1 and HARTE-2 is 5 μm and the outer edge of the Schottky contact metal exceeds the inner edge of HARTE-2, being 15 μm for D1, D2, and D3. The implanted p^+ widths and the Schottky contact widths between the implanted p^+ regions are designed to be (2 μm, 2 μm), (2 μm, 3 μm), and (2 μm, 4 μm), respectively, for D1, D2, and D3.

5. Conclusions

4H-SiC JBS diodes are fabricated and reported by using Ti as the Schottky contact metal. Simulation results show that the spacing between the p^+ regions should not be too narrow (e.g., 0.5 μm) because the depletion regions would be connected with each other in the horizontal direction, which would lead to a dramatic increase in the device onset voltage. Two HARTE rings with four different termination designs are chosen in the experiment to prevent the electric field from crowding on the edge of the device. The experimental results reveal that the extended Schottky contact metal could increase the depletion region and thus increase the breakdown voltage. However, the extended length should not be too long in case the HARTE regions are too far from the Schottky contact edge to prevent the electric field from crowding in the blocking state. Besides, the spacing between HARTE-1 and HARTE-2 should be properly designed in order to ensure that the spacing between HARTE-1 and HARTE-2 could be well pinched-off to achieve high blocking voltage and low leakage current. J2 with $a = 4$ μm and $b = 15$ μm shows the best reverse characteristic (a leakage current of 9×10^{-5} A at a reverse voltage of 1000 V). Though the implant annealing of the HARTE and p^+ regions is performed at 1250 °C instead of 1600–1800 °C, good forward and reverse characteristics are achieved.

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