Improved interface properties of HfO_2 gate dielectric GaAs MOS device by using SiN_x as interfacial passivation layer

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GaAs metal-oxide-semiconductor (MOS) capacitor with HfO_2 as gate dielectric and silicon nitride (SiN_x) as interlayer (IL) is fabricated. Experimental results show that the sample with SiN*x* as IL has an improved capacitance–voltage characteristic, lower leakage current density (0.785×10^{-6} A/cm^2 at $V_{fb} + 1$ V) and lower interface-state density (2.9×10^{12} eV^{-1}·cm^{-2}) compared with other samples with N_2– or NH_3–plasma pretreatment. The influences of post-deposition annealing temperature on electrical properties are also investigated for the samples with SiN_x IL. The sample annealed at 600 °C exhibits better electrical properties than that annealed at 500 °C, which is attributed to the suppression of native oxides as confirmed by XPS analyses.

Keywords: GaAs metal-oxide-semiconductor (MOS) devices, silicon nitride, interlayer, post-deposition annealing

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1. Introduction

Recently, III–V compound semiconductor, e.g., GaAs, has been expected as a promising channel material for future high-performance CMOS devices due to its high intrinsic electron mobility, large energy band gap, and low power consumption.[1] However, the formations of native oxides on GaAs surface, e.g., Ga oxide and As oxide, result in a high interface-state density which pins the Fermi level.[2–4] It is reported that integration of high-*k* dielectric such as HfO_2 on sulfur-treated GaAs can efficiently suppress the native oxides.[5–8] However, the direct deposition of HfO_2 on GaAs gave rise to abnormal *C*–*V* characteristics with no accumulation region.[5]In order to achieve good electrical properties, surface pretreatments, e.g., by using N_2 plasma, NH_3 plasma, and Si passivation, have been investigated by many groups. Dalapati *et al.*[9] reported that N_2–plasma pretreatment can efficiently remove the volatile element As from the surface, but the Ga–O and As–O bonds are still present. Furthermore, Yasui *et al.*[10] investigated the effects of the NH_3–plasma pretreatment on the interface properties as compared with the N_2–plasma pretreatment and found that the former can more effectively suppress the formation of the Ga–O bond than the latter. In addition, Si passivation can reach an improved *C*–*V* characteristic since the Si atoms can terminate the dangling bonds.[11] However, Si can be used as n-type dopant for GaAs substrate, causing the instability of threshold voltage. Among these passivation methods, the incorporation of N or Si is believed to be beneficial to suppress the native oxides and terminate the dangling bonds. In recent years, several researches have been performed on the use of SiN_x as gate insulator,[12] SiN_x/Si bi-layer as interface control layer,[11] and SiN_x as passivation layer on GaN substrate,[13,14] but less attention was paid to the structure of HfO_2/SiN_x/GaAs. In view of these, it is expected that good electrical properties of GaAs MOS devices could be achieved by using SiN_x as interlayer (IL). Thus, in this work, an ultrathin SiN_x is deposited by plasma enhanced chemical vapor deposition (PECVD) to use as interlayer between HfO_2 gate dielectric and GaAs substrate, and the improved electrical properties of the MOS devices are obtained compared with other passivation methods. Furthermore, the influences of post-deposition annealing (PDA) on electrical characteristics and chemical states of GaAs MOS device with SiN_x IL are also investigated.

2. Experiments

Si-doped n-type GaAs (100) wafers with a doping concentration of 5×10^{17} cm^{-3} were used as substrates. The wafers were cleaned using acetone, alcohol, and isopropanol for 5 min, sequentially, and rinsed with deionized water several times, followed by dipping in HCl solution and $(NH_4)_2S$ solution to remove native oxides.

After drying by N_2, a 2-nm SiN_x IL was deposited by the PECVD method at 250 °C, named SiN_x samples. The NH_3-to-SiH_4 gas ratio of 20:5 was used with a total pressure of 13.3 Pa. The RF power was 80 W. For comparison, the surfaces of some wafers were subjected to N_2– and NH_3–plasma pretreatment in PECVD chamber under the same conditions, called N_2 and NH_3 samples, respectively. A wafer without any surface pretreatment was used to prepare control sample. Then, all the samples were subjected to a deposition of 12-nm HfO_2 gate dielectric by an RF-sputtering method and using an Hf-target.

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The sputtering chamber was evacuated to a background pressure of 10^{-4} Pa, and then the sputtering gas of $Ar : O_2 = 26 : 4$ was filled up to an operation pressure of 2.66 Pa. Two different PDA temperatures of 500 °C and 600 °C were used for the SiN_x samples (called SiN_x 500 and SiN_x 600 samples, respectively) to investigate effects of PDA temperature on the interface properties, and only 600 °C was used for the N_2 and NH_3 samples. All anneals were carried out in N_2 for 60 s. Finally, Al was thermally evaporated and patterned into a gate electrode with an area of 7.85×10^{-5} cm^2 and also into back electrode, followed by N_2 annealing at 300 °C for 20 min to reduce contact resistances.

High-frequency (HF) *C–V* curves were measured by HP4284A precision LCR meter, and gate leakage current was measured by HP4156A precision semiconductor parameter analyzer. Physical thickness of the gate dielectric was determined by spectroscopic ellipsometry. X-ray photoelectron spectroscopy analysis was carried out by using a VG Multilab 2000 system.

3. Results and discussion

Figure 1 shows the HF (1 MHz) *C–V* curves and *I–V* characteristics of all the samples annealed at 600 °C. Obviously, the control sample without any surface pretreatment shows poor *C–V* behavior with the largest "strech-out" (see Fig. 1(a)). This is attributed to the native oxides-induced interface pining between GaAs substrate and HfO_2.[5] Although the NH_3 sample shows a *C–V* behavior as good as that in Ref. [10], the best *C–V* characteristic is obtained for the SiN_x 600 sample, with clear accumulation saturation and large slope in depletion regime (see Fig. 1(a)), indicating that the Fermi level is unpinned[15] and thus a good interface quality is achieved. The flat-band voltages (V_{fb}), gate-oxide capacitance (C_{ox}), and interface-state density (D_{it}) are extracted from the HF *C–V* curve, which are listed in Table 1. The values of V_{fb} are 2.78, 1.42, 1.06, and 0.83 V for the control sample, N_2 sample, NH_3 sample, and SiN_x 600 sample, respectively, among which the smallest value is for the SiN_x 600 sample. The D_{it} near midgap is estimated by Terman's method[16] for comparison. The samples with surface pretreatment show smaller D_{it} than the control sample, indicating that the surface pretreatment (e.g., N_2 plasma, NH_3 plasma, SiN*x* as IL) can significantly reduce the defects at/near the interface. For the N_2 sample, GaAs surface is effectively passivated according to[17]

$$\mathrm{GaAs} + \mathrm{N} \rightarrow \mathrm{GaN} + \mathrm{As(AsN)}. \quad (1)$$

The NH_3 sample has smaller D_{it} than the N_2 sample due to the additional H atoms and NH radicals,[10] which can suppress the oxygen atom diffusion towards the surface of GaAs substrate. Moreover, as shown in Fig. 1(b), the SiN_x 600 sample has almost the same leakage current density as the NH_3 sample below the gate voltage of 1.1 V, but the smaller leakage current density (e.g., 0.785×10^{-6} A/cm^2 at $V_{fb} + 1$ V) is achieved when $V_{GS} \geq 1.1$ V due to the good insulating property of SiN_xIL.[18] The smallest value of D_{it} is found for the SiN_x 600 sample due to Si atoms which can terminate defect-related surface bonds,[11,19] high density species (H atoms and NH radicals) and good desorption property of SiN_x to As and Ga atoms.[20] Thus, the SiN_x IL as surface passivation can more effectively suppress the native oxides than the other surface pretreatment methods by reducing, even eliminating, the native oxides of GaAs as confirmed by XPS analyses below, resulting in an excellent-quality interface with the smallest interface-state density (2.9×10^{12} $eV^{-1} \cdot cm^{-2}$).

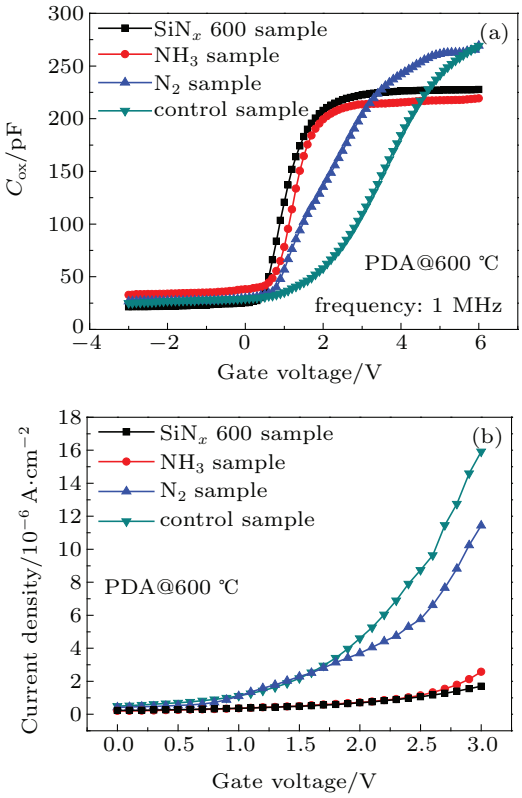


Fig. 1. (color online) (a) HF *C–V* curves and (b) *I–V* characteristics of all the samples annealed at 600 °C.

Table 1. Electrical and physical parameters of all the samples.

Sample	Control sample	N_2 sample	NH_3 sample	SiN_x 600 sample
C_{ox}/pF	269.2	269.4	219.2	227.7
V_{fb}/V	2.78	1.42	1.06	0.83
$D_{it}/eV^{-1} \cdot cm^{-2}$	1.81×10^{13}	5.4×10^{12}	3.5×10^{12}	2.9×10^{12}

In fact, effects of the SiN_x as interlayer to passivate surface of GaAs are related to PDA temperature as shown in Fig. 2. For the SiN_x sample annealed at 500 °C, it exhibits much poorer *C–V* curve and larger gate leakage current than that annealed at 600 °C. The values of V_{fb} extracted from their *C–V* curves are 2.27 V and 0.83 V for the SiN_x samples annealed at 500 °C and 600 °C, respectively. It is obvious that the SiN_x IL annealed at 600 °C can effectively diminish the formations of defects at/near the interface as compared with that annealed at 500 °C, and thus the SiN_x 600 sample shows better electrical properties than the SiN_x 500 sample.

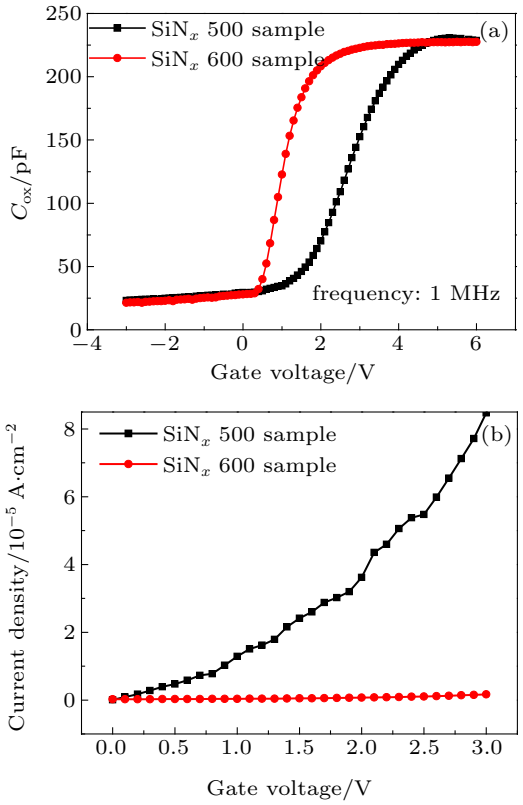


Fig. 2. (color online) (a) HF *C–V* curves and (b) *I–V* characteristics of SiN_x 500 and 600 samples.

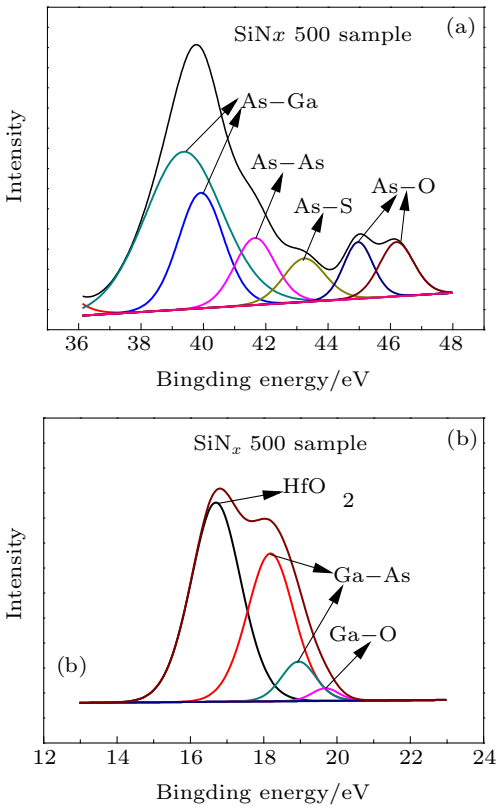


Fig. 3. (color online) XPS spectra of the As 3d and Ga 3d for the SiN_x 500 sample.

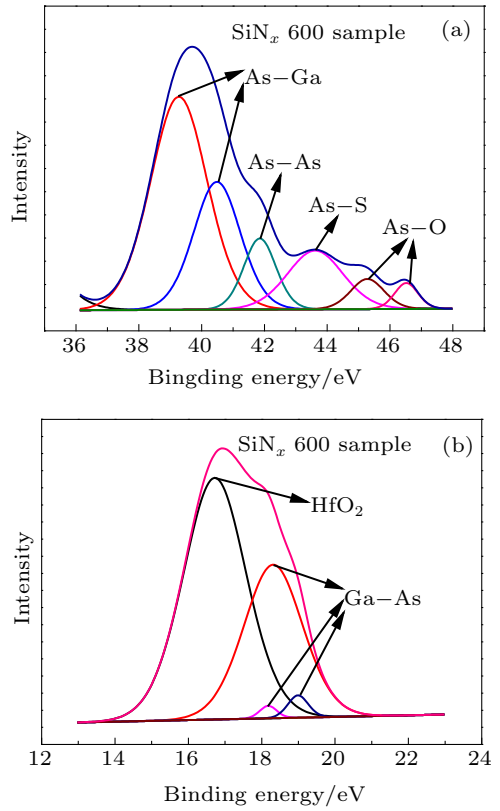


Fig. 4. (color online) XPS spectra of the As 3d and Ga 3d for the SiN_x 600 sample.

To clarify the effects of PDA temperatures on chemical states of the SiN_x sample, XPS analyses are performed for the SiN_x 500 and 600 samples. Figure 3 shows the typical XPS spectra of the As 3d and Ga 3d for the SiN_x 500 sample. From Fig. 3(a), it can be seen that As–O peaks are observed at 45.28 eV and 46.52 eV, and As–S peak and As–As peak occur at 43.62 eV and 41.85 eV, respectively. In Fig. 3(b), the peaks at 18.19 eV and 18.95 eV are from Ga–As bond, and the other two peaks at 16.7 eV and 19.68 eV correspond to $HfO_2$and Ga–O bonds, respectively. It was reported that the As–O and Ga–O bonds can act as defect states in the band gap and play a critical role in degrading electrical properties of devices.[21] For the SiN_x 600 sample, the chemical bonding states are given in Fig. 4. As can be seen from Fig. 4(a), the peak intensity of the As–O bond becomes smaller than that in Fig. 3(a), implying that the As oxides have been greatly reduced. Also from Fig. 4(b), it can be noted that the peak corresponding to the Ga–O bond is not observed, indicating that Ga oxides have been suppressed by 600 °C PDA. The weaker-intensity peaks of the native oxides for the SiN_x 600 sample also mean that the PDA at 600 °C can more effectively prevent out-diffusion of Ga and As than at 500 °C, because a densified and high-quality SiN_xIL can be formed during PDA at 600 °C.[22] These results indicate that the SiN*x* IL annealed at higher temperature (e.g., 600 °C) can effectively suppress the growth of the native oxides compared with that at lower temperature (e.g., 500 °C). This is why the SiN_x 600 sample has better quality of interface and electrical properties than the SiN_x 500 sample.

4. Summary

The GaAs MOS devices with SiN_x as IL are prepared and the improved interface properties are achieved. Com-

pared with the samples with N_2– or NH_3–plasma pretreatment, the sample with SiN_x IL exhibits an improved *C*–*V* characteristic, lower gate leakage current density (0.785×10^{-6} A/cm^2 at $V_{fb} + 1$ V) and lower interface-state density (2.9×10^{12} eV^{-1}·cm^{-2}). This indicates that the SiN_x IL as surface passivation can more effectively suppress the native oxides than the other surface pretreatment methods due to roles of the Si atoms and the high-density species (such as H atoms and NH radicals), and good desorption property of SiN_x for As and Ga atoms. Moreover, the improved extent of the interface properties is related to PDA temperature for the samples with SiN_x IL. The sample annealed at 600 °C is demonstrated to have better electrical properties than that annealed at 500 °C, and these two samples, annealed at 600 °C and 500 °C, respectively, have flat-band voltages of 0.83 V and 2.27 V, and interface-state densities of 2.9×10^{12} eV^{-1}·cm^{-2} and 6.09×10^{12} eV^{-1}·cm^{-2}. The XPS analyses confirm that the SiN_x IL annealed at higher temperature (e.g., 600 °C) can effectively suppress the growth of the native oxides compared with that at lower temperature (e.g., 500 °C).

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