The conductive mechanisms of a titanium oxide memristor with dopant drift and a tunnel barrier*

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Nano-scale titanium oxide memristors exhibit complex conductive characteristics, which have already been proved by existing research. One possible reason for this is that more than one mechanism exists, and together they codetermine the conductive behaviors of the memristor. In this paper, we first analyze the theoretical base and conductive process of a memristor, and then propose a compatible circuit model to discuss and simulate the coexistence of the dopant drift and tunnel barrier-based mechanisms. Simulation results are given and compared with the published experimental data to prove the possibility of the coexistence. This work provides a practical model and some suggestions for studying the conductive mechanisms of memristors.

Keywords: memristor, conductive mechanism, dopant drift, tunnel barrier

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1. Introduction

Since Moore's law will gradually reach its limitation as complementary metal–oxide semiconductor (CMOS) technologies are approaching maturity around 2020,[1] new techniques and devices are urgently needed for the purpose of continuing the law. The appearance and applications of nanotechnology are changing traditional electronic devices into ones with smaller geometric size, lower power dissipation and cost, faster speed, and higher performance. Thus, nano-electronics is the best option for overcoming the restrictions on microelectronics,[2] and as a new nano-scale electron device, the memristor has aroused great interest in modeling, simulation, application, and other related research. Moreover, its potential in resistive random access memory (RRAM),[3] cellular neural networks (CNNs),[4] chaotic circuit analysis,[5] digital logical operation,[6] etc, has already been proved.

Theoretically, the memristor was predicted as a basic circuit element by Chua in 1971,[7] and determined by the relation: $M(q) = \mathrm{d}\varphi(t)/\mathrm{d}q(t)$, where $\varphi(t)$ and $q(t)$ are the magnetic flux and charge, respectively. $M(q)$ is called the memristance, and has the resistance value of a memristor. Chua and Kang then extended the memristor concept to a broader memristive system.[8] In 2008, Strukov *et al.*[9] successfully fabricated a nano-scale metal/oxide/metal structure that has the characteristics of a theoretical memristor. Since then, the electrical characteristics, modeling, and applications of memristors have become hot topics in circuit academia. Biolek *et al.*[10] modeled the dopant drift process inside the memristor to simulate its characteristics in SPICE. Zhang *et al.*[11] studied the mathematical model and properties of memristors with border constraint. Bao *et al.*[12] proposed a flux-controlled memristor that is determined by a monotonically increasing cubic curve with nonlinearity, and Song *et al.*[13] studied the basic properties and applications of the memristor circuit. Jia *et al.*[14] proved that a nano dot embedded structure optimized the performance of memristors, and Bao *et al.*[15] presented a new smooth memristor oscillator, which was derived from Chua's oscillator, by replacing Chua's diode with a flux-controlled memristor and a negative conductance.

The conductive mechanism is an important research field concerned with the theoretical basis and application of titanium oxide memristors. However, it is currently still under debate, and several major theories have been proposed. Based on the physical–experimental results in Ref. [16], Strukov *et al.*[9] brought forward the dopant drift mechanism (DDM). Pickett *et al.*[17] utilized the Simmons *I–V* expression for a rectangular barrier to quantitatively describe the static transport and switching dynamics of the memristor, so this could be called the tunnel barrier mechanism (TBM). Yang *et al.*[18] gave details of the oxygen vacancies and oxygen gas formations in the process of oxide electroforming with the help of direct experimental evidence.

One possible reason explaining the complexity of the conductive behaviors of memristors is that several different mechanisms may coexist and different mechanisms can be dominant in different materials systems.[19] However, there has been no detailed research on the coexistence of DDM and TBM, which may result in the complex conductive process in a memristor. Moreover, a circuit model that is compatible with DDM and TBM is in urgent need for studying such a case.

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In the present paper, a memristor circuit model that is compatible with DDM and TBM is designed, and its accuracy and feasibility are demonstrated by simulations which are consistent with those already published. By utilizing the proposed model, the coexistence of DDM and TBM in one memristor is discussed and studied through SPICE simulations. We conclude that the coexistence case is closer to the already published physical–experimental phenomena than the case of single DDM or TBM. This work gives a practical model and some suggestions for further investigation of the conductive mechanisms of memristors.

The paper is organized as follows. In Section 2 detailed analyses of DDM and TBM are made. In Section 3 the design of the proposed compatible model and its simulation results for linear dopant drift (LDD), nonlinear dopant drift (NDD), and tunnel barrier-based cases are presented. In Section 4 the coexistence of DDM and TBM is discussed, and the possibility and rationality of the coexistence are confirmed by the simulation results. Finally, we draw some conclusions from the present studies in Section 5.

2. Conductive mechanisms of titanium oxide memristors

Voltage v, current i, charge q, and magnetic flux φ are four basic circuit variables. Theoretically, there should be six connections between them, as shown in Fig. 1. From the necessity of symmetry, Chua[7] suggested that a basic circuit element should exist. In his further research, he found the memory characteristics of the device, so it was called the memristor.

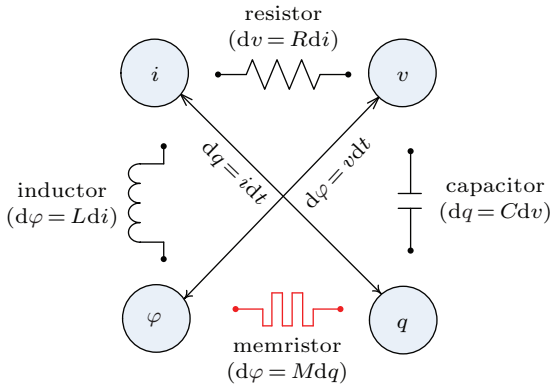


Fig. 1. (color online) The basic circuit variables and their connections.

Since the memristor relates φ to q together, the theoretical relations for charge-controlled and flux-controlled memristors are as follows:

$$\varphi = f(q), \tag{1}$$

$$q = f(\varphi). \tag{2}$$

Taking the charge-controlled memristor for example, the differential form of Eq. (1) with respect to time t shows the relation between v and i as

$$M(t) = \frac{v(t)}{i(t)} = \frac{\mathrm{d}f(q)}{\mathrm{d}q}. \tag{3}$$

Theoretically, $q(t)$ records the device history in terms of the transient resistance of a memristor, since $q(t)$ is the time integration of $i(t)$. The value of $M(t)$ depends on the charge according to Eq. (3), so memristors show the ability to remember.

One typical nano-scale titanium oxide memristor mainly consists of four parts, as shown in Fig. 2. The top and bottom electrodes are made of platinum. One layer of titanium oxide with oxygen vacancies is regarded as the doped region with dopants. Another layer of stoichiometric titanium oxide is considered as the undoped region and the ratio of oxygen to titanium is perfect, at exactly two to one.[20] The width of the doped layer is $w(t)$, and D is the whole width of the two layers. There are several techniques for forming the doped and undoped layers, such as electroforming,[18] standard contact optical lithography and sputter deposition.[21]

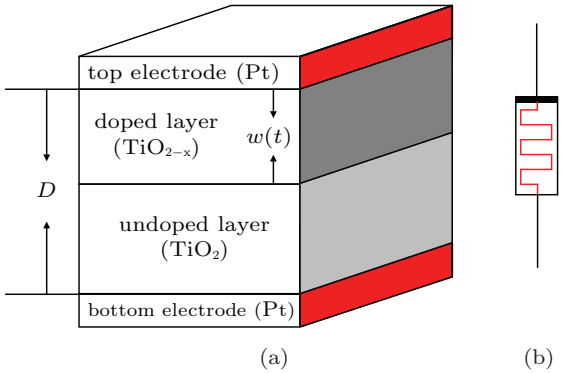


Fig. 2. (color online) The typical structure (a) and circuit symbol (b) of a titanium oxide memristor.

In nano-scale devices, small voltages can yield enormous electric fields, which in turn can produce significant nonlinearities in ionic transport[9] and result in complexity in the conductive process of titanium oxide memristors. Discussions and research around the conductive mechanisms have always been hot issues since the advent of the first memristor. DDM and TBM are two main theories that represent the conductive principles of memristors in different ways.

2.1. The dopant drift mechanism

DDM is proposed on the basis of the formation and drift of oxygen vacancies in doped titanium oxide. Suppose that both doped and undoped layers are connected in parallel, as shown in Fig. 3. There is only stoichiometric titanium oxide in the undoped layer; thus each titanium atom possesses two oxygen atoms and stable electrovalent bonds form between them, so there are hardly any chances for the oxygen atoms to move randomly. The undoped layer can therefore be regarded as an insulator with no current in it. However, the lack of a certain

percentage of oxygen results in the formation of vacancies that are not stable and could easily transfer between the adjacent titanium atoms in the doped layer. Oxygen vacancies with positive charges will move towards the negative polarity of $v(t)$, since like charges repel each other while opposite charges attract. The directional movement of charges forms current in the doped layer, and therefore, an obvious difference in conductivity exists between the two layers.

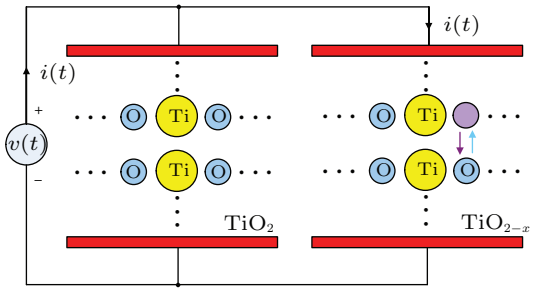


Fig. 3. (color online) The difference in conductive behavior between the doped and undoped layers.

The resistance R of a given material depends on the length l, average cross-sectional area s, and its electrical resistivity ρ, expressed as

$$R = \rho \frac{l}{s}. \tag{4}$$

It is obvious that the doped and undoped layers could be regarded as two variable resistors connected in series. The resistance of each layer is proportional to its length, since the two layers share the same cross-sectional area

$$R_{\text{doped}} = R_{\text{ON}} \frac{w(t)}{D}, \tag{5}$$

$$R_{\text{undoped}} = R_{\text{OFF}} \left(1 - \frac{w(t)}{D}\right), \tag{6}$$

$$v(t) = (R_{\text{doped}} + R_{\text{undoped}}) i(t), \tag{7}$$

where R_{ON} and R_{OFF} are the memristances of the memristor when $w(t) = D$ and $w(t) = 0$, respectively. $i(t)$ is the current that flows through the memristor, and $v(t)$ drives the oxygen vacancies in the doped layer towards the undoped one, so the width of each layer changes. For the simplest case of Ohmic electronic conduction and linear ionic drift in a uniform field with average ion mobility μ_{v}, it is found that[9]

$$\frac{\mathrm{d}w(t)}{\mathrm{d}t} = \mu_{\text{v}} \frac{R_{\text{ON}}}{D} i(t). \tag{8}$$

The combination of Eqs. (5)–(8) leads to an analytical relation between $q(t)$ and $M(t)$ as follows:

$$M(q) = M_0 - \frac{q(t)}{Q_0}(R_{\text{OFF}} - R_{\text{ON}}), \tag{9}$$

where M_0 is the initial memristance and $Q_0 = D^2/(\mu_{\text{v}} R_{\text{ON}})$ is a constant. Equation (9) is consistent with the theoretical definition of the memristor, which is expressed in Eq. (3) and demonstrates how the memristor remembers the device history in terms of memristance.

The LDD gives a basic and ideal description of the conductive behaviors of the memristor, but excludes the boundary conditions. In many existing physical experiments, the boundary movement is suppressed when the value of $w(t)$ approaches 0 or D, and it remains a constant until the voltage reverses the polarity.[9] The LDD could be improved to NDD by adding a window function $F(w)$, such as Eq. (10) to Eq. (8), since $F(w)$ acts as a coefficient that depends on the value of $w(t)$. The LDD could also be regarded as one of the special cases of NDD when $F(w) = 1$.

$$F(w) = \frac{w(D-w)}{D^2}, \tag{10}$$

$$\frac{\mathrm{d}w(t)}{\mathrm{d}t} = F(w)\mu_{\text{v}} \frac{R_{\text{ON}}}{D} i(t). \tag{11}$$

The simulation results of NDD in Ref. [9] are approximate with respect to the physical experimental data in Ref. [16]. We conclude that the formation and drift of oxygen vacancies in titanium oxide are the critical factors of DDM.

2.2. The tunnel barrier mechanism

Pickett *et al.*[17] gave details of the electroforming process and proposed TBM to describe the conductive behaviors of titanium oxide memristors.

The device in Ref. [17] is a thin film of stoichiometric titanium oxide that is sandwiched between two platinum electrodes, as shown in the upper part of Fig. 4. It is then electroformed by applying a voltage sweep from 0 to 6 V over 5 ms. At the same time, oxygen vacancies are formed, which result in a highly conductive channel and shunt most of the oxide film except for a narrow tunnel gap. The gap was modeled by an electron tunnel barrier. The tunnel barrier width $\delta(t)$ can be modulated by applying a voltage across the memristor, and the highly conductive channel can be regarded as a resistor R_{S}. Therefore, after the process of electroforming, the device is equivalent to an Ohmic resistor and a tunnel barrier connected in series.

Based on the Simmons I–V expression for a rectangular barrier with image forces,[22] the supplementary material of Ref. [17] gave the function form of the static transport model of titanium oxide memristors by Eqs. (12)–(20). The current that flows through the device is modeled by utilizing a tunneling junction, and its function form is given as follows:

$$i = \frac{j_0 A}{\Delta\delta^2} \left\{ \phi_{\text{I}} \mathrm{e}^{-B\sqrt{\phi_{\text{I}}}} - (\phi_{\text{I}} + e|v_{\text{g}}| \mathrm{e}^{-B\sqrt{\phi_{\text{I}} + e|v_{\text{g}}|}}) \right\}, \tag{12}$$

where

$$v_{\text{g}} = v - \mathrm{i}R_{\text{S}}, \tag{13}$$

$$j_0 = \frac{e}{2\pi h}, \tag{14}$$

$$\delta_1 = \frac{1.2\lambda\delta}{\phi_0}, \tag{15}$$

$$\Delta\delta = \delta_2 - \delta_1 \tag{16}$$

$$\phi_I = \phi_0 - e|v_g|\left(\frac{\delta_1+\delta_2}{\delta}\right) - \left(\frac{1.15\lambda\delta}{\Delta\delta}\right)\ln\left(\frac{\delta_2(\delta-\delta_1)}{\delta_1(\delta-\delta_2)}\right), \tag{17}$$

$$B = \frac{4\pi\Delta\delta\sqrt{2m}}{h}, \tag{18}$$

$$\delta_2 = \delta_1 + \delta\left(1 - \frac{9.2\lambda}{(3\phi_0 + 4\lambda - 2e|v_g|)}\right), \tag{19}$$

$$\lambda = \frac{e^2\ln(2)}{8\pi k\varepsilon_0\delta}, \tag{20}$$

where k is the dielectric constant, h is Planck's constant, m the mass of the electron, A the channel area of the memristor, e the electron charge, v the voltage applied to the tunnel barrier and highly conductive channel, v_g the voltage across the tunnel barrier, ϕ_0 the barrier height in electron volts, and ε_0 the vacuum permittivity.

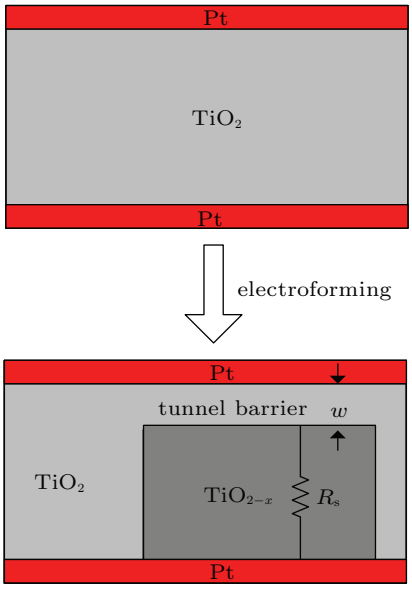


Fig. 4. (color online) Schematic diagram of a memristor after the electroforming process.

The tunnel barrier width δ is time-varying and could be modeled according to the exponential dependence of the switching time on the device current.[17]

In the case of $i(t) > 0$,

$$\frac{d\delta}{dt} = f_{off}\sinh\left(\frac{i}{i_{off}}\right) \times \exp\left[-\exp\left(\frac{\delta - a_{off}}{\delta_c} - \frac{|i|}{b}\right) - \frac{\delta}{\delta_c}\right]; \tag{21}$$

in the case of $i(t) < 0$,

$$\frac{d\delta}{dt} = f_{on}\sinh\left(\frac{i}{i_{on}}\right) \times \exp\left[-\exp\left(-\frac{\delta - a_{on}}{\delta_c} - \frac{|i|}{b}\right) - \frac{\delta}{\delta_c}\right], \tag{22}$$

where f_{off}, i_{off}, a_{off}, b, δ_c, f_{on}, i_{on}, and a_{on} are all constants. Equations (12)–(22) are the basis for modeling and simulating memristor conductive behaviors determined by TBM.

3. The compatible circuit model in SPICE

A significant challenge to the widespread adoption of memristive oxide switches by circuit designers has been the lack of a predictive compact model that can be integrated into a time domain simulation package like SPICE.[17] However, there has been no detailed realization of a circuit model that simulates both the DDM and TBM of a memristor and the interrelations between them. For the purpose of solving such a problem, a compatible circuit model of memristors is proposed, and its feasibility and accuracy are proved by simulations in SPICE.

3.1. The circuit model structure

The proposed model is shown in Fig. 5, and the main nodes are indicated by arrows. Nodes 'pos' and 'neg' represent the two terminals of a memristor, and 'interface' denotes the node between the active areas of a memristor and the electrodes. The proposed model mainly consists of two parts. In the first part, G_{mem} is a current-controlled current source. R_1, R_2, and R_E are three resistors. G_{mem} and R_1 are connected in series between nodes pos and interface. R_E is between nodes interface and neg, and represents the resistance of two electrodes. In the second part, E_{mem} is a current-controlled voltage source, and L is an inductor with a negligible internal resistance R_2. The first part represents the main body of a memristor and the second is used for dealing with the differential relations between the state variable and memristor current as expressed in Eqs. (11), (21), and (22). The voltage between nodes pos and interface is defined to be $v_{mem}(t)$, which is the voltage of the main part except the electrodes in a memristor.

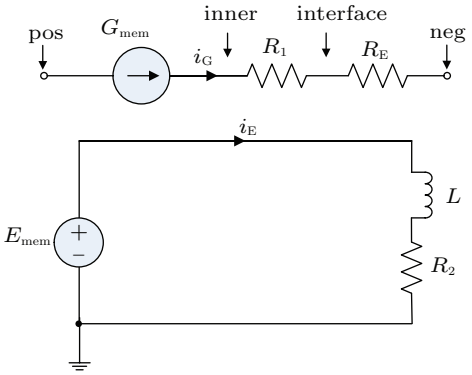


Fig. 5. The proposed circuit model of the titanium oxide memristor.

The relation between i and φ of an inductor with inductance L is given as follows:

$$L = \frac{\mathrm{d}\varphi}{\mathrm{d}i}. \tag{23}$$

Numerically, the value of i is the time integration of the voltage when $L = 1$ H, since φ is the time integration of the voltage across the inductor. Therefore, the second part of the circuit model acts as an integrating circuit, which is indispensable for simulating both dopant drift and tunnel barrier-based cases. Each memristor has an initial state, which is represented by the initial current i_0 in the inductor.

Compared with the already published models, our model is compatible with DDM and TBM. In the case of DDM, G_{mem} represents two variable resistors (doped and undoped layers) which are connected in series. The resistances of R_1 and R_2 are both set to be a negligible value. i_{E} and i_{G} represent the doped layer width and the current that flows through the device, respectively. The second part of the circuit model simulates the differential relation between $w(t)$ and i_{G} according to Eq. (11). E_{mem} and G_{mem} are expressed as follows:

$$E_{\mathrm{mem}} = F(i_{\mathrm{E}})\frac{\mu_{\mathrm{v}} R_{\mathrm{ON}}}{D} i_{\mathrm{G}}, \tag{24}$$

$$G_{\mathrm{mem}} = \frac{v(\mathrm{pos},\mathrm{neg}) - i_{\mathrm{G}} R_{\mathrm{E}}}{i_{\mathrm{E}} R_{\mathrm{ON}}/D + (1 - i_{\mathrm{E}}/D) R_{\mathrm{OFF}}}, \tag{25}$$

where v(pos,neg) is the voltage between nodes pos and neg. In the case of TBM, G_{mem} and R_1 represent the tunnel barrier and highly conductive channel, respectively. The second part of the circuit model simulates the differential relations between $\delta(t)$ and i_{G} according to Eqs. (21) and (22). i_{E} represents $\delta(t)$, and E_{mem} and G_{mem} are expressed as follows:

$$E_{\mathrm{mem}} = \frac{1}{2}\left\{ [\mathrm{sgn}(v_{\mathrm{g}}) + 1] \left.\frac{\mathrm{d}\delta}{\mathrm{d}t}\right|_{i(t)>0} + [-\mathrm{sgn}(v_{\mathrm{g}}) + 1] \left.\frac{\mathrm{d}\delta}{\mathrm{d}t}\right|_{i(t)<0} \right\}, \tag{26}$$

$$G_{\mathrm{mem}} = \frac{j_0 A}{\Delta\delta^2}\left\{ \phi_{\mathrm{I}} \mathrm{e}^{-B\sqrt{\phi_{\mathrm{I}}}} - \left(\phi_{\mathrm{I}} + e|v_{\mathrm{g}}| \mathrm{e}^{-B\sqrt{\phi_{\mathrm{I}} + e|v_{\mathrm{g}}|}} \right) \right\}, \tag{27}$$

where v_{g} is the voltage between nodes pos and inner, and the value of i_{E} equals the value of $\delta(t)$. sgn(x) is the sign function, which is defined by the following relation:

$$\mathrm{sgn}(x) = \begin{cases} 1, & x > 0, \\ 0, & x = 0, \\ -1, & x < 0. \end{cases} \tag{28}$$

The adoption of sgn(x) guarantees the unified form of Eqs. (21) and (22) and is a necessary condition for the simulations.

3.2. Simulation results

DDM and TBM are simulated in SPICE and the results are compared with the published simulations to prove the feasibility and accuracy of the proposed model. The circuit for simulations consists of a voltage bias $v(t)$ and a memristor, as shown in Fig. 6. The version of our SPICE software is PSpice 10.5, which is a widely used version.

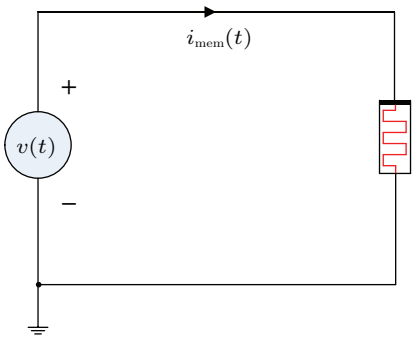


Fig. 6. (color online) The circuit structure for the simulation.

The case of LDD is simulated first and the results are given in Fig. 7. Key parameters adopted in the simulation are cited from Ref. [9]: $\mu_{\mathrm{v}} = 10^{-14}\cdot\mathrm{m}^2\cdot\mathrm{V}^{-1}\cdot\mathrm{S}^{-1}$, $D = 10$ nm, $R_{\mathrm{ON}} = 100\ \Omega$, $R_{\mathrm{OFF}} = 5$ kΩ, and the initial value of the doped layer width $w_0 = 1.0$ nm, $L = 1$ H. The values of R_{E}, R_1, and R_2 are all equal to 1 mΩ, and thus $v_{\mathrm{mem}}(t)$ could be approximately regarded as being equal to $v(t)$, as shown in Figs. 7(a) and 7(b). $v(t) = v_0 \sin(\omega t)$, $v_0 = 0.65$ V, and $\omega = 2\pi$. The simulation time span $T = 3$ s and time step $\Delta t = 0.1$ ms. $vntol = 10^{-7}$ and $abstol = 1$ are the absolute voltage and current tolerance, respectively. The V–I curve of LDD in Ref. [9] is shown in the illustration of Fig. 7.

By contrast, the case of NDD is simulated and the results are given in Fig. 8. $v(t) = v_0 \sin(\omega t)$, $v_0 = 4.0$ V, and the other parameters are the same as those adopted in the case of LDD. The function given in Eq. (10) is selected as the window function. The experimental V–I curve of a memristor device in Ref. [16] is given in the illustration of Fig. 8(d), which indicates that NDD is closer to the physical experiment data than LDD.

The case of NDD with an asymmetric input voltage is then simulated and the results are given in Fig. 9. The asymmetric input voltage has a triangular waveform, and its positive and negative peak values are 0.7 V and −0.65 V, respectively. The simulation time span $T = 18$ s and time step $\Delta t = 1$ ms. The other parameters remain unchanged.

The case of TBM is simulated and the results are given in Fig. 10. The key parameters are as follows: $\phi_0 = 0.95$ eV, $e^2 \ln(2)/(8K\varepsilon_0) = 0.0998$, $\delta_1 = 0.1261$ nm, $f_{\mathrm{off}} = 3.5$ μs, $i_{\mathrm{off}} = 115$ μA, $a_{\mathrm{off}} = 1.2$ nm, $f_{\mathrm{on}} = 40$ μs, $i_{\mathrm{on}} = 8.9$ μA, $a_{\mathrm{on}} = 1.8$ nm, $b = 500$ μA, $\delta_{\mathrm{c}} = 0.107$ nm, $\delta_0 = 1.1$ nm, L is set to 1 nH to take into account that δ is in nm, $R_1 = 215\ \Omega$ and $R_{\mathrm{E}} = 2.4$ kΩ, $R_2 = 1$ mΩ. The key parameters and input voltage adopted in the simulation are consistent with those in Ref. [23]. The voltage bias applied to the memristor model has an asymmetric triangular waveform, and is shown in

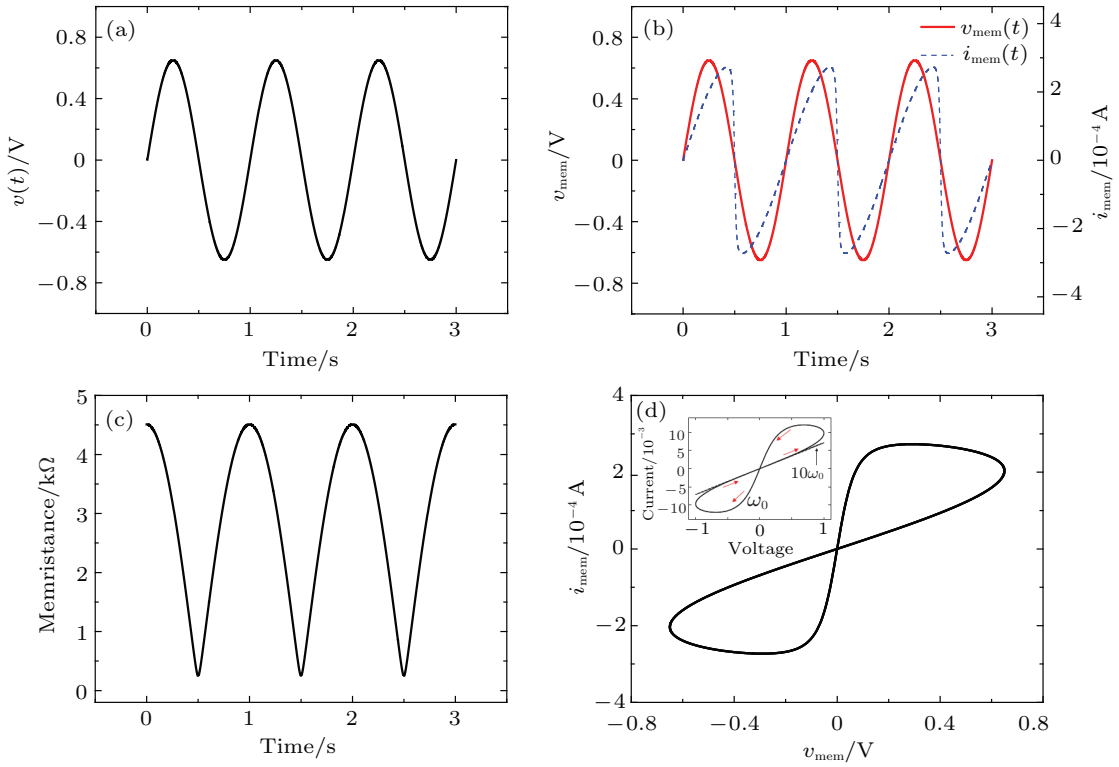


Fig. 7. (color online) The simulation results of the proposed model in the case of LDD.

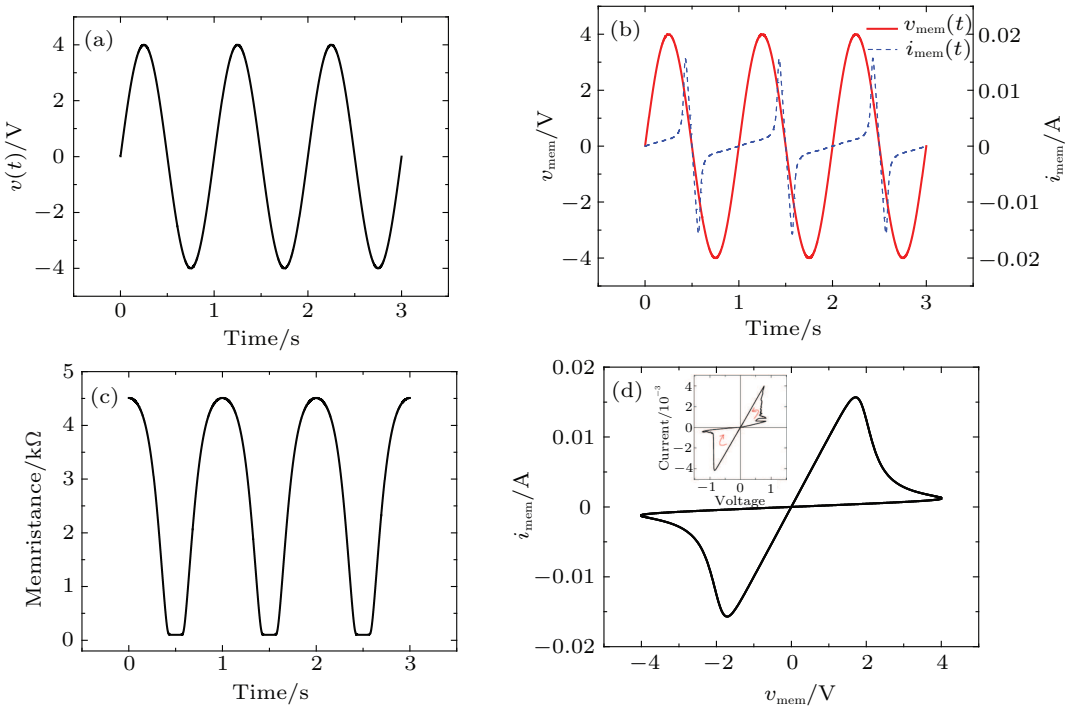


Fig. 8. (color online) The simulation results of the proposed model in the case of NDD with a symmetric input voltage.

Fig. 10(a). The simulation time span $T = 18$ s and time step $\Delta t = 1$ ms. The illustration of Fig. 10(d) shows the simulation (solid line) and experimental results (black dots) of the memristor with a tunnel barrier in Ref. [23].

The simulations shown in Figs. 7, 8, and 10 are consistent with the results already published in Refs. [9] and [23]. Therefore, the feasibility and compatibility of our model are proved. As shown in Fig. 9, DDM-based conductive behavior exhibits changeable V–I features when the input bias has an asymmetric waveform, since the value of the initial doped

layer width changes at the beginning of each outer bias cycle. On the contrary, TBM-based conductive behavior exhibits stable V–I features with a similar input voltage waveform, as shown in Fig. 10.

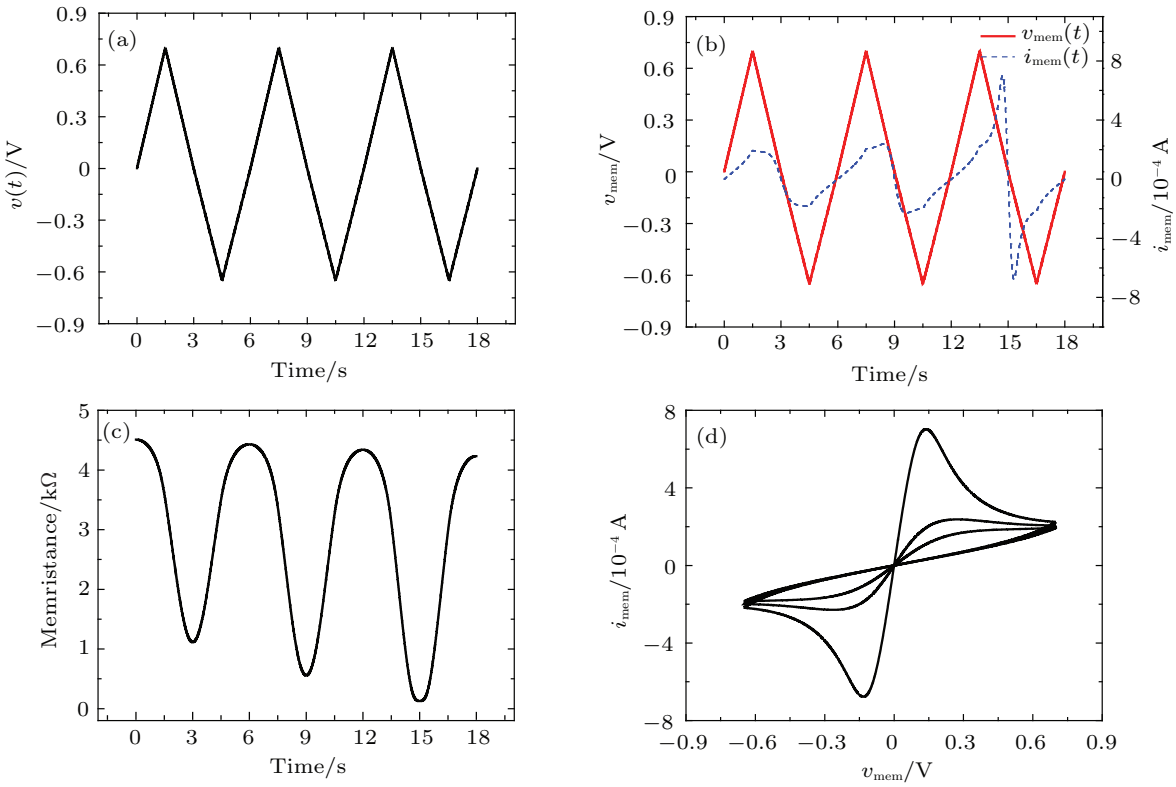


Fig. 9. (color online) The simulation results of the proposed model in the case of NDD with an asymmetric input voltage.

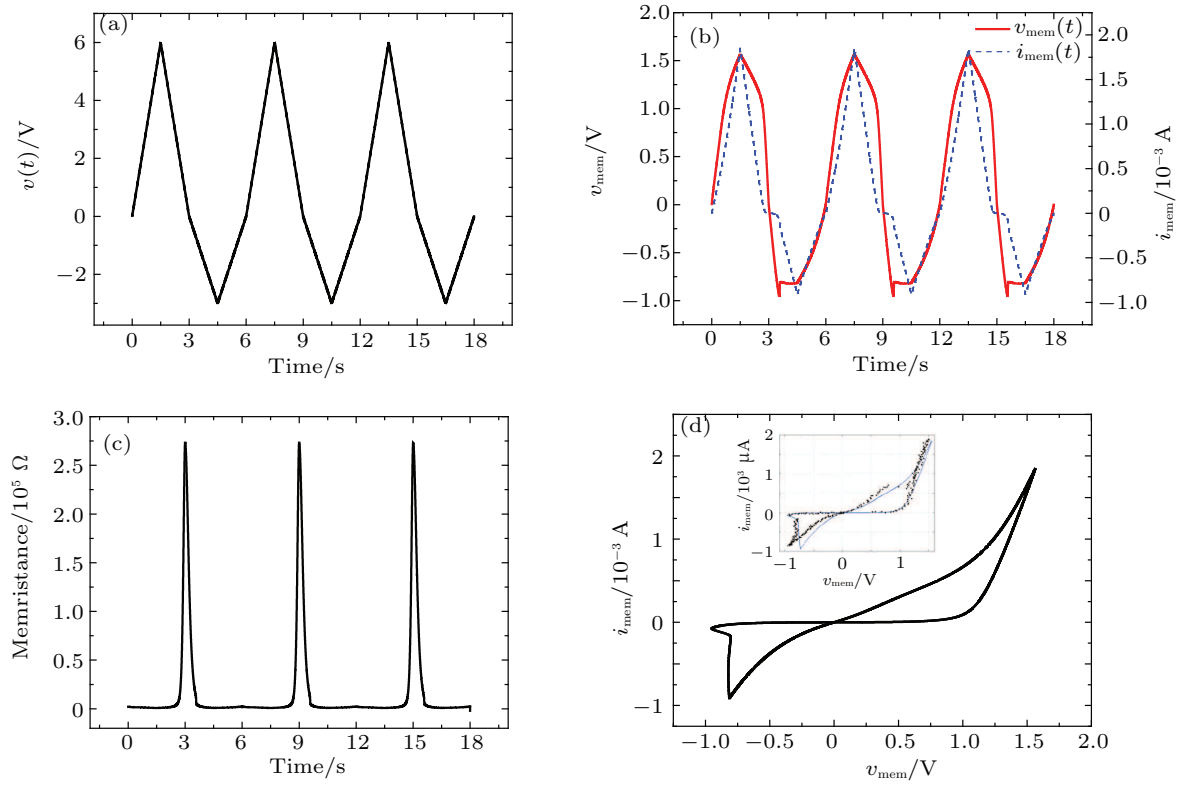


Fig. 10. (color online) The simulation results of the proposed model in the case of TBM.

4. The coexistence of DDM and TBM

There is a special phenomenon in many of the existing physical experimental results, such as the data shown in Fig. 1(b) in Ref. [18], and in Fig. 1(c) in Ref. [19], and also in memristor V–I curves that within several identical outer bias cycles do not coincide with each other. A possible explanation is that different mechanisms may coexist compared with the major mechanism, with the minor one possibly regarded as an interference.

DDM and TBM are totally different from each other. The former occurs in the inner part of titanium oxide and has a certain connection with the formation and transfer of oxygen vacancies. The latter occurs at the interface between the titanium oxide and electrodes, so it is associated with the formation of a tunnel barrier. If we suppose that they coexist in one memristor, then its conductive behavior will probably be special and different from neither pure DDM nor pure TBM-based behaviors.

Since the tunnel barrier and its series-connected highly conductive channel occupy only part of the titanium oxide and share the same electrodes with the remaining part in a memristor, as shown in Fig. 4, it is a reasonable deduction that two parts are connected in parallel. Though the remaining part mainly consists of stoichiometric titanium oxide, it could be regarded as a mixture of doped and undoped titanium oxide with an ultra-low value of initial doped layer width.

Theoretically, there are three cases of coexistence. In the first two cases, DDM or TBM plays a major role. In the third case, the conductive behavior is a half-and-half mixture of them.

The proposed circuit model is modified to simulate the case of coexistence, and is shown in Fig. 11.

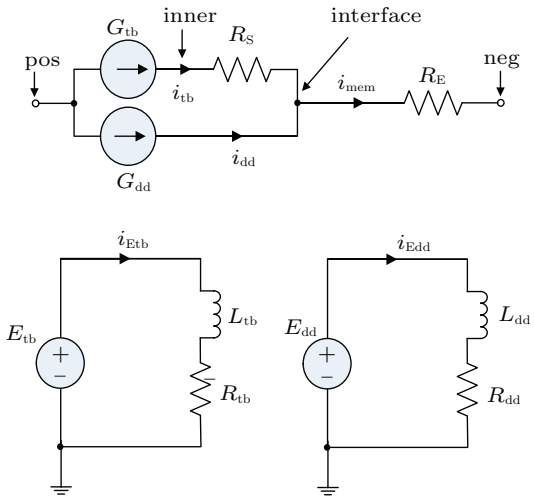


Fig. 11. A modified circuit model for simulating the coexistence of DDM and TBM.

In the modified model, G_{tb} and G_{dd} are two current-controlled current sources that represent the tunnel barrier and titanium oxide, respectively. The titanium oxide contains two layers in accordance with the typical structure shown in Fig. 2. E_{tb} and E_{dd} are two current-controlled voltage sources. The subcircuit, which is in the lower left corner of Fig. 11, contains E_{tb}, L_{tb}, and R_{tb}, and acts as an integrating circuit for simulating the differential relation between the tunnel barrier width and the current of the memristor. The other subcircuit with the same structure is used to simulate the differential relation between the doped layer width and the current of the memristor. The main nodes are indicated by arrows. The circuit structure and outer voltage bias used for simulation are shown in Figs. 6 and 10(a), respectively.

It is possible that a memristor with both TBM and DDM has changeable V–I curves with the asymmetric input voltage, since the titanium oxide shows such a changeability, while the tunnel barrier exhibits stability. In this case, the titanium oxide is equivalent to a variable resistor with a changeable initial resistance value.

The simulation results shown in Fig. 12 confirm our guess and prove the possibility of the coexistence of two mechanisms in one memristor. In Figs. 12(c) and 12(d), R_{TB} and R_{DD} represent the transient resistances of the tunnel barrier with its series-connected high conductive channel and the titanium oxide, respectively. The key parameters are as follows: w_0 is set to be 10^{-4} nm to take into account that the undoped layer width has an ultra-low initial value. Compared with $R_{ON} = 100\ \Omega$ and $R_{OFF} = 5\ \text{k}\Omega$ in the simulations shown in Figs. 7–9, R_{ON} and R_{OFF} are set to be 200 Ω and 10 kΩ, respectively, since the cross-sectional area of the titanium oxide decreases after the electroforming process, on the assumption that the new value is half the original one. The other parameters remain the same.

As shown in Fig. 12(a), $v_{mem}(t)$ has a smaller amplitude than $v(t)$, since the electrodes act as a voltage divider. In Figs. 12(b)–12(e), the tunnel barrier and its series-connected highly conductive channel exhibit relatively stable features, which are consistent with the simulation results shown in Fig. 10. However, the titanium oxide shows changeable features, since the asymmetric $v_{mem}(t)$ results in an increment of the initially doped layer width in each voltage cycle, and this has been proved by the simulation results shown in Fig. 9. The V–I curve given in Fig. 12(f) exhibits the mixed effect produced by DDM and TBM in one memristor. Compared with the V–I curve, which is shown in Fig. 10(d), the V–I curve of the memristor with the coexistence of DDM and TBM exhibits changeable features that are closer to the already published physical–experimental phenomena than the case of single DDM or TBM.

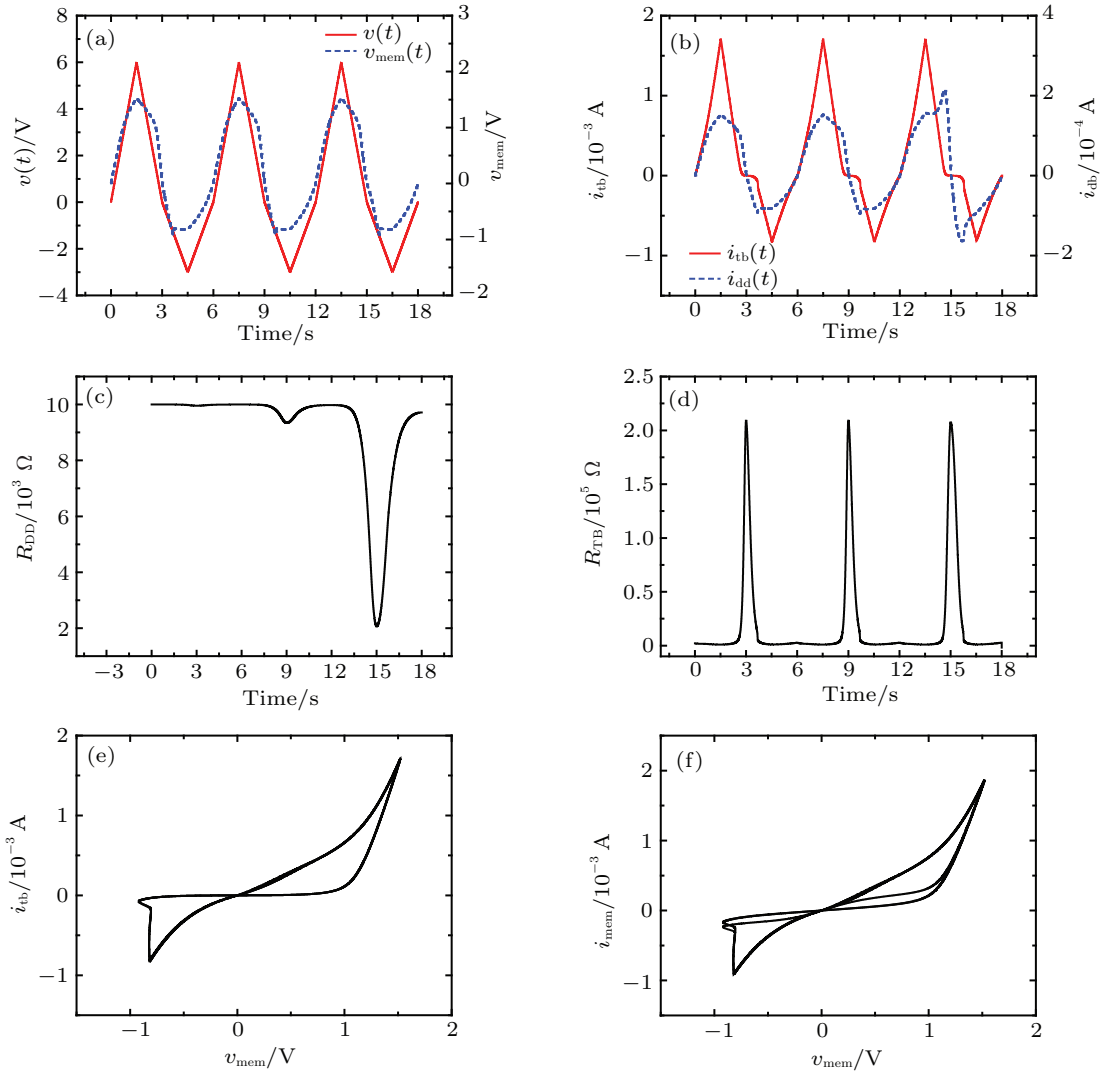


Fig. 12. (color online) The simulation results of the modified circuit model with asymmetric input voltage.

5. Conclusions

A circuit model of a memristor that is compatible with DDM and TBM is proposed in this paper and simulated in SPICE. By utilizing the proposed circuit model, the coexistence of DDM and TBM in one memristor is simulated and discussed. The simulation results prove the possibility of the coexistence. With the proposed circuit model and simulation results, researchers can further study the coexistence of conductive mechanisms in different cases, which is also our future work.

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