SPICE modeling of flux-controlled unipolar memristive devices*

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Unipolar memristive devices are an important kind of resistive switching devices. However, few circuit models of them have been proposed. In this paper, we propose the SPICE modeling of flux-controlled unipolar memristive devices based on the memristance versus state map. Using our model, the flux thresholds, ON and OFF resistance, and compliance current can easily be set as model parameters. We simulate the model in HSPICE using model parameters abstracted from real devices, and the simulation results show that the proposed model caters to the real device data very well, thus demonstrating that the model is correct. Using the same modeling methodology, the SPICE model of charge-controlled unipolar memristive devices could also be developed. The proposed model could be used to model resistive memory cells, logical gates as well as synapses in artificial neural networks.

Keywords: unipolar memristive devices, memristive, SPICE model

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1. Introduction

The concepts of memristors[1] and memristive systems[2] were proposed by Chua as early as in the 1970s. However, relevant research has remained dormant ever since because of the absence of their physical implementations. In 2008, the missing memristor was found by researchers from Hewlett-Packard (HP).[3] Since then, studies related to memristors and memristive devices have been thriving throughout the world. Memristive devices have lower power consumption, excellent scalability, simple cell structure, complementary metal oxide semiconductor (CMOS) process compatibility, and especially, a nonvolatile state-holding capability,[4–10] which make them one of the most promising next-generation memory technologies. Moreover, memristive devices are also being studied for many other applications, such as building stateful logic gates,[11–13] modeling synapses in neuromorphic systems,[10,14,15] and processing analog signals.[16–19]

Generally, a memristive device can store one bit of information in a high-resistance state (HRS, or the OFF state) and a low-resistance state (LRS, or the ON state) and its state can be switched by an external voltage or current. Memristive devices are divided into unipolar devices and bipolar devices based on their switching behavior. For unipolar devices, the switching procedure does not depend on the polarities of the voltage and the current signals, while for bipolar devices, the set to an ON state occurs at one voltage/current polarity and the reset to the OFF state occurs on the reversed voltage/current polarity.[4,5] Compared with bipolar memristors, unipolar materials are more suitable for building memories. Firstly, the polarity-independent switching characteristic of unipolar devices simplifies the peripheral circuit design of the resistive memory. Secondly, unipolar devices usually feature a larger switching ratio and a better linear I–V correlation in their LRSs than their bipolar counterparts.[20,21]

Nano-circuit researchers have proposed many circuit models for bipolar memristors.[22–30] However, few studies have been done for developing an efficient circuit model of unipolar memristive devices. To the best of our knowledge, there are only two such SPICE models available. One was proposed by Lee *et al.*.[31] They developed an HSPICE macromodel of unipolar resistive random access memories (RAMs), which showed good agreement with experimental results but did not consider the compliance current issue (the compliance current is imposed on a memristive device to protect the device from dielectric breakdown during the SET process), and is not applicable to very-large-scale circuit-level simulations since it incorporated many nonlinear circuit elements, such as RS flip flops and operational amplifiers. The other was proposed by Akou *et al.*[32] They also developed a behavioral model of unipolar resistive RAMs. Their model was in accordance with the experimental results. However, the modeling method is rather complex, e.g., using the double-well potential function, and manually setting the compliance current according to the applied voltage pulse, the implementation of which is of low efficiency.

In this paper, we propose the SPICE modeling of flux-controlled unipolar memristive devices. We build the model based on the memristance versus state map proposed by

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Chua.[33] The memristance versus state map reveals the intrinsic switching characteristic of a memristive device (here, the state refers to the flux or the charge, and throughout the paper, we will use memristance and resistance interchangeably since they are of the same unit Ω). The map can be used to navigate resistance switching of memristive devices precisely. The advantage of our method is that it can be applied to all of the unipolar memristive devices, rather than be just limited to some specific devices with particular switching mechanisms. Since most real device data are presented in the voltage sweep form, we choose the flux as the state variable to demonstrate our modeling methodology, which could also be used to build the SPICE model for charge-controlled unipolar memristive devices.

The most significant contributions of this work are as follows: (i) we develop the SPICE model for flux-controlled unipolar memristive devices, which has not been proposed before. In our model, the flux thresholds, ON and OFF resistance, compliance current can easily be set as model parameters. (ii) we build the model on the memristance versus flux map, which captures the intrinsic feature of unipolar memristive devices, and has not been used to model unipolar memristive devices before. (iii) we simulate the SPICE model in HSPICE using the model parameters abstracted from real-device data, which validates the functionality of the proposed model. The model can be used to model resistive memory cells, logical gates as well as synapses in artificial neural networks.

The rest of the paper is organized as follows: Section 2 discusses the memristance versus state map and the state equation for unipolar memristive devices, which are the theoretical bases for building the SPICE models. Section 3 presents the circuit structures and the simulation program for integrated circuits emphasis (SPICE) implementation of the model. Section 4 presents the simulation verification of the model. In Section 5, we discuss the benefits and shortcomings of the proposed model. Section 6 concludes the paper.

2. Memristance versus state map and state equation

The memristor[1] is the fourth fundamental two-terminal circuit element characterized by a constitutive relation between charge q and flux φ, which are the time integrals of current $i(t)$ and voltage $v(t)$ through the element, respectively. A memristor is flux-controlled if its constitutive relation can be expressed by

$$q = q(\varphi), \tag{1}$$

where $q(\varphi)$ is the continuous and piecewise-differentiable function with bounded slopes. Note that in the same way, the charge-controlled memristor can also be defined (i.e., in the form of $\varphi = \varphi(q)$).

Differentiating Eq. (1) with respect to time t, we obtain

$$i = \frac{\mathrm{d}q}{\mathrm{d}t} = \frac{\mathrm{d}q(\varphi)}{\mathrm{d}\varphi}\frac{\mathrm{d}\varphi}{\mathrm{d}t} = G(\varphi)v, \tag{2}$$

where

$$G(\varphi) = \frac{\mathrm{d}q(\varphi)}{\mathrm{d}\varphi} \tag{3}$$

is called the memductance at φ in unit of Siemens (S). Furthermore, to present Eq. (3) in the memristance versus flux form, we obtain

$$R(\varphi) \equiv \frac{1}{G(\varphi)}, \tag{4}$$

where $R(\varphi)$ is the memristance at φ, and has the unit of Ohms (Ω).

The curve of $R(\varphi)$ is called the memristance versus state (flux) map, the concept of which was first proposed by Chua.[33] When a memristive device is fabricated, its $R(\varphi)$ feature is determined, which means that the memristance versus state map depicts the intrinsic resistance switching characteristic of a memristive device, and can be used to guide the resistance tuning of the device. The state is flux or charge. Hence, there are memristance versus flux maps for flux-controlled unipolar memristive devices, and memristance versus charge maps for charge-controlled unipolar memristive devices. For instance, the memristance versus flux maps of a memristive device is shown in Fig. 1. To change its memristance from R_0 to R_1, one only needs to apply a voltage pulse whose time integral is equal to $\Delta\varphi$, as shown in the inset of Fig. 1. In fact, any voltage stimulation which infuses $\Delta\varphi$ flux into the memristor will yield the same memristance switching effect.

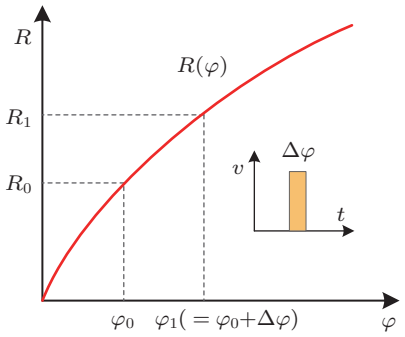


Fig. 1. (color online) Memristance versus charge map of a memristive device. The inset shows the generation of $\Delta\varphi$ flux by a voltage pulse.

With the help of the memristance versus state map of a memristive device, we can tune its memristance in a predicable way, namely, applying the voltage/current pulse to change the flux/charge state of the device, and then the memristance. Hence, it is of crucial importance to derive the memristance versus state map for the modeled device. In the paper, we choose the flux as the state variable since most of the real device data are presented in the voltage sweep form. Inspired

by the memristance versus state map for binary memristors in Ref. [33], we propose the equation of the memristance versus flux map for unipolar memristive devices as follows:

$$R(\varphi) = \frac{1}{2}\{(R_{\rm off}+R_{\rm on})-(R_{\rm off}-R_{\rm on}) \times [\mathrm{sgn}(|\varphi|-B_1)\times \mathrm{sgn}(|\varphi|-B_2)]\}, \quad (5)$$

where $R_{\rm on}$ and $R_{\rm off}$ are the ON and OFF resistance of the unipolar device, and B_1 and B_2 are the flux thresholds, i.e., the flux breaking points in Fig. 2. $\mathrm{sgn}(x)$ is the sign function, which returns -1 if x is less than 0, 0 if x is equal to 0, and 1 if x is greater than 0.[34] The sign function can readily be found in SPICE dialects such as HSPICE. The curve of the memristance versus flux map is shown in Fig. 2.

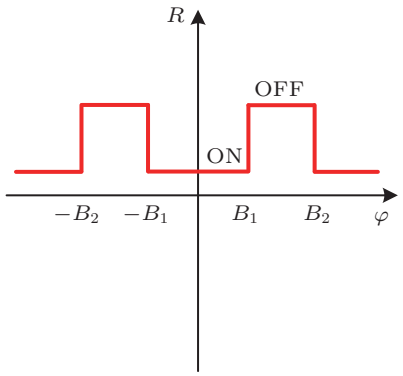


Fig. 2. (color online) Memristance versus flux map of unipolar memristive devices. B_1 and B_2 are the RESET and SET flux thresholds, while ON and OFF denote the low and high-resistance states.

In the positive flux branch, when the flux is in the range of $[0, B_1)$, the device holds the ON state; when the flux passes the RESET flux threshold B_1, the memristance is abruptly switched to the OFF state (the RESET process) and keeps constant in the range of $[B_1,\ B_2)$; when the flux exceeds the SET flux threshold B_2, the memristance is switched to the ON state again (the SET process). Such resistance switching processes are in accordance with the voltage polarity independence feature of unipolar memristive devices. Meanwhile, the memristance switching behavior is symmetrical in the negative flux branch. Note that the memristance versus state map of a memristive device also obeys Ohm's Law, except that the memristance R is not a constant. In the proposed model, the dynamical variable determining the memristance is flux, which evolves according to the voltage integral equation, called the state equation. A unipolar memristive device is therefore defined by the flux-dependent Ohm's law

$$i_{\rm M} = \frac{v_{\rm M}}{R(\varphi)} \quad (6)$$

and the memristive state equation

$$\varphi = \int_0^t v_{\rm M}\mathrm{d}t, \quad (7)$$

where $v_{\rm M}$ is the applied voltage, and $i_{\rm M}$ is the current through the memristive device.

3. SPICE implementation

Based on the port equation (flux-dependent Ohm's law) and the state equation proposed above, we can build the SPICE model. The unipolar memristive device is modeled by a two-terminal (pos,neg) circuit block, which is shown in Fig. 3. The sub-circuit in Fig. 3(a) implements the port equation by the voltage-controlled current source GM. The sub-circuit in Fig. 3(b) implements the state equation by connecting the voltage-controlled current source GF with the capacitor CF. The external voltage is integrated on CF and the flux is equal to the voltage of point x. The resistor RG provides a DC path from x to ground for the simulator to calculate the initial DC operating point. RG will not affect simulation results since it is endowed with a huge resistance. The sub-circuit in Fig. 3(c) calculates the memristance of the model by connecting the voltage-controlled voltage source ER with the resistor RM. The memristance of the model is equal to the voltage of point y.

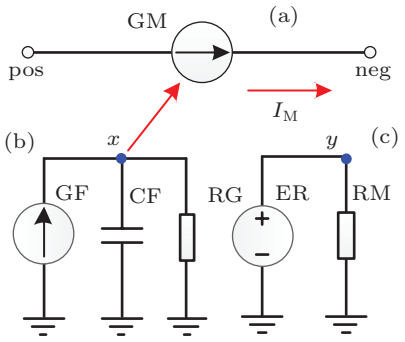


Fig. 3. (color online) SPICE circuit of the proposed model: (a) sub-circuit for the port equation, (b) sub-circuit for the state equation, and (c) sub-circuit for calculating memristance.

The core SPICE code for implementing the circuit in Fig. 3 is shown in Fig. 4. Note that the SPICE code can be implemented in any SPICE-compatible simulator. Code line 1 is the parameter function for the memristance versus flux map. Code line 2 corresponds to the sub-circuit in Fig. 3(a). In the expression of GM, $I_{\rm cc}$ is the compliance current, and the ternary function is used to impose the compliance current limitation. Notice that a ternary function is defined in the form of $a\ ?\ b : c$, which means IF a, THEN b, ELSE c.[34] The IF clause of the ternary function has two conditions: the former checks whether the port current is larger than the compliance current and the latter makes the compliance current limitation only be imposed on the SET process. The applied voltage in GM is wrapped by the abs( ) function to make sure that the switching behavior is symmetrical in the negative voltage branch. Note that abs(x) returns the absolute value of x : $|x|$.[34] Code lines 3, 4, and 5 correspond to the sub-circuit in Fig. 3(b). Code lines 6 and 7 correspond to the sub-circuit in Fig. 3(c). In line 6, *scale* is the parameter for better model stability.

```
*-------------Memrsitance vs. Flux map----------------
1 .PARAM g(t)='((Roff+Ron)-
  +(sgn(abs(t)-B1)*sgn(abs(t)-B2))*(Roff-Ron))/2'
*---------------Resistive Port Equation-----------------
2 GM pos neg value='(abs(V(pos,neg)/g(V(x)))>Icc
  +&&(abs(V(x))>B2)) ? Icc*sgn(V(pos,neg)) :
  +V(pos,neg)/g(V(x))'
*---------------------State Equation---------------------
3 GF 0 x value='V(pos,neg)'
4 CF x 0 1
5 RG x 0 1T
*---------------------Memristance------------------------
6 ER y 0 value='g(V(pos,neg))/scale'
7 RM y 0 1
*--------------------------------------------------------
```

Fig. 4. (color online) Core SPICE code of the proposed model: code line 1 is the parameter function for the memristance versus flux map; code line 2, code lines 3, 4 and 5, and code lines 6 and 7 correspond to the sub-circuits in Figs. 3(a), 3(b), and 3(c), respectively.

4. Simulation

To validate the functionality of the proposed model, we implement the model in HSPICE. In the following simulation, the parameters are abstracted from real devices in Ref. [13]. The R_{on} and R_{off} resistance are set to 35 Ω and 10 kΩ, the RESET flux threshold (B_1) and SET flux threshold (B_2) are chosen as 1.125 mWb and 8 mWb. The compliance current (I_{cc}) is set to ±10 mA, and the scale parameter (*scale*) is set to 1000. The model is initially in the ON state when the input flux is zero (the initial state is determined by the memristance versus flux map). Firstly, to demonstrate the hysteresis *I*–*V* characteristics of the unipolar memristive device, we apply a sinusoid-like piecewise linear voltage source to the model with zero net input flux, as shown in the inset of Fig. 5. In the positive branch of the *I*–*V* curve in Fig. 5, the voltage increases from 0 V to 6 V and then decreases to 0. In this process, when the voltage increases to 1.5 V, the input flux reaches the RESET flux threshold (1.125 mWb), and the RESET process occurs; while the voltage increases to 4 V, the input flux reaches the SET flux threshold (8 mWb), and the SET process occurs. The current compliance keeps the current from rising above 10 mA in the SET process. When the voltage decreases to 0, a closed *I*–*V* curve appears. The symmetrical process happens in the negative voltage branch, and the curve is symmetrical about the origin. The path of the curve is denoted by the arrows with the sequence numbers. The *I*–*V* curve shown in Fig. 5 is the most significant symbol of unipolar memristive devices, which means our model correctly models the hysteresis behavior of the unipolar device. In addition, the *I*–*V* curve shows good agreements with the *I*–*V* curve in Ref. [13], which demonstrates the precision of the model.

To further validate the model, we present the memristance versus flux map of the model. The stimulating voltage is shown in Fig. 6(a), and the memristance versus flux map is shown in the lower part of Fig. 6(b). The voltage sweep from 0 to 24 ms is responsible for generating the negative input flux, thus producing the left part of the memristance versus flux map, while the voltage sweep from 24 ms to 48 ms is responsible for generating the positive input flux, thus producing the right part of the memristance versus flux map. As can be seen from the figure, the memristance versus flux map of the modeled device is in accordance with the theoretical memristance versus flux map of unipolar memristive device proposed in Fig. 2.

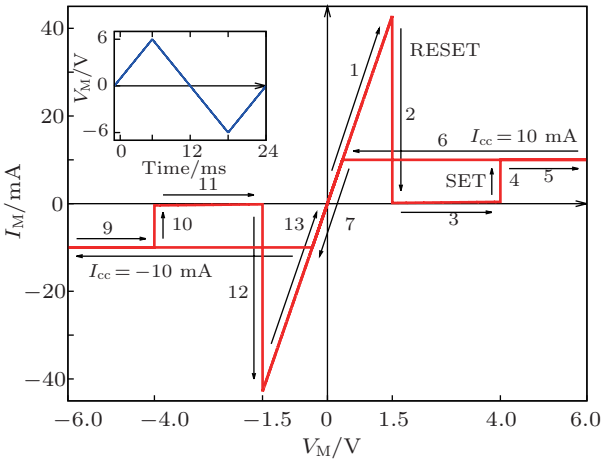


Fig. 5. (color online) *I*–*V* characteristics of the modeled device. The inset shows the stimulating voltage curve with zero net input flux. The red curve shows the hysteresis relation of voltage and current, which is symmetrical about the origin. The curve path is denoted by the numbered arrows. The RESET and SET processes happen when their corresponding flux thresholds are met, that is, when the voltage is equal to 1.5 V and 4 V with the applied voltage curve. I_{cc} is the compliance current and is equal to ±10 mA.

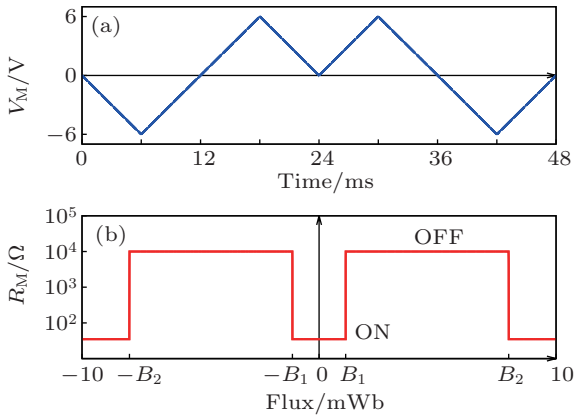


Fig. 6. (color online) Memristance versus flux map of the proposed model. (a) shows the stimulating voltage curve, and (b) is the real map, which is in accordance with the theoretical map proposed in Fig. 2.

Furthermore, figure 7 gives the five-segment piecewise-linear charge versus flux curve of the model with the same stimulating voltage in Fig. 6. Here, three parallel red segments with a steep slope ($= 1/R_{on}$) are in the low-resistance state, whereas two parallel blue segments with a much larger slope ($= 1/R_{off}$) are in the high-resistance state. Note that the compliance current constraint is temporally relieved in order to obtain the correct charge amount in the SET process. The curve

in Fig. 7 fits well with the unipolar switching characteristics detailed by Chua in Ref. [33], which further demonstrates the correctness of the model.

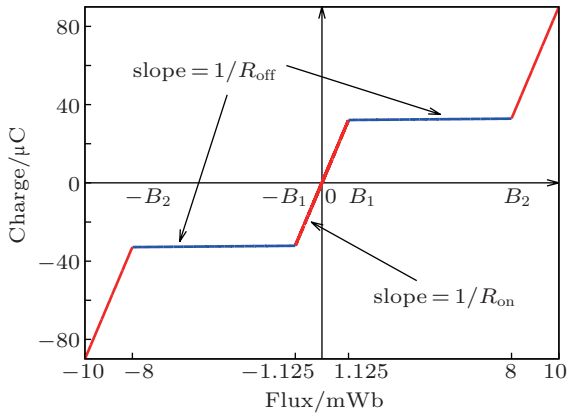


Fig. 7. (color online) Five-segment "staircase-like" charge versus flux relationship of the proposed model. The red segments are in the low-resistance state (R_{on}) and the blue segments are in the-high-resistance state (R_{off}).

To demonstrate the feasibility of the model for modeling memory cells, we show the voltage pulse responses of the model. The pulse width is set as 1 ms, and the pulse amplitudes are ±3 V for RESET and ±6 V for SET. The voltage pulses are shown in Fig. 8(a), while the memristance switching responses are shown in Fig. 8(b). The model is initially in the ON resistance state ($= R_{on}$). When a positive RESET pulse is applied to the model, the memristance is switched to the OFF resistance state ($= R_{off}$), and when a positive SET pulse is applied, the memristance is switched to the ON resistance state ($= R_{on}$) again. The same switching processes occur when the negative RESET and SET voltage pulses are applied to the model. This model behavior is in accordance with the theory of unipolar memristors which mentions that the memristance of unipolar memristors can be switched by the voltage pulses of the same polarity, or in other words, their switching behavior is polarity-independent.[33]

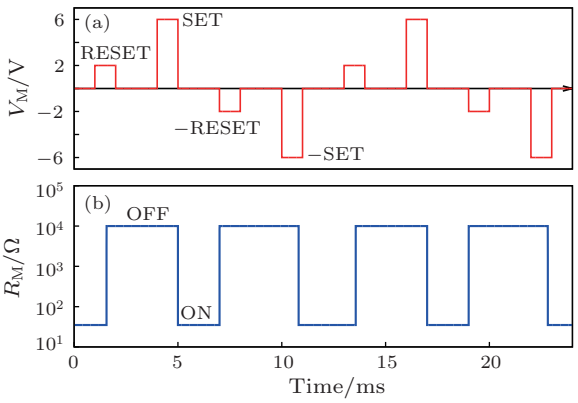


Fig. 8. (color online) Voltage pulse responses of the model with pulse width 1 ms and pulse amplitudes ±3 V for RESET and ±6 V for SET. The upper part (a) shows the simulating voltage pulses and the lower part (b) shows the corresponding resistance switching.

Based on the simulation results above, we can conclude that the proposed model of flux-controlled unipolar memristive devices is correct.

5. Discussion

When building the model, we use the memristance versus flux map, which is an intrinsic and common characteristic for unipolar memristive devices, rather than on the *I*–*V* feature of any specific unipolar device. The benefit of this approach is that it makes the model mechanism-independent and widely applicable to all kinds of unipolar memristive devices. Moreover, the model for charge-controlled unipolar memristive devices could also be built in the same way by using the memristance versus charge map.

Although built mechanism-independently, the proposed model is in accordance with the filament theory. According to the filament theory, the resistance switching is caused by the formation and rupture of conductive filaments under electric field biases or thermal effects, namely, filament formation for the SET process and filament rupture for the RESET process.[4,5,7,10] In our model, voltage is integrated as flux, and flux is correlated to the ability to rupture filaments in the RESET process and to form filaments in the SET process. However, our model only behaviorally describes those abilities because the analytical relation for those correlation is unknown, due to the fact that the detailed resistance switching mechanisms of unipolar memristive devices have not yet been thoroughly understood. Moreover, the dependence of set-state resistance and reset current on the compliance current can also attributed to the formation mechanism of conductive filaments, which means this dependence could also be correlated to flux, and be potentially reflected by the model.

In the proposed model, however, the memristance will eventually be switched as long as the net flux passes the flux thresholds, no matter how small the applied voltage is. This discrepancy with some voltage threshold memristor models is due to using flux as the resistance switching threshold rather than voltage. Nevertheless, the model better explains the phenomenon that a larger voltage bias switches a device faster than a small voltage bias, since a larger voltage integrates flux faster. Using the model, if the wave form of the applied voltage is known, the time of the resistance switching event can be predicted. Last but not least, the proposed model is a general model for all of the unipolar memristive devices, and could be implemented in any SPICE-compatible circuit simulators, such HSPICE and PSPICE.

6. Conclusion

In this paper, we have proposed an SPICE model for the flux-controlled unipolar memristive devices. We build the

model on the memristance versus flux map, thus making the model mechanism-independent and widely applicable to the unipolar memristive devices. By setting various model parameters, our model can model real unipolar devices easily yet precisely. The functionality of the model is validated by actual experimental data, which proves that the model is correct. Although we only present the model of flux-controlled devices in the paper, the model of charge-controlled devices could also be developed by the same modeling approach based on the memristance versus charge map. The proposed model can be applied in various areas such as modeling resistive memory cells, logical gates, and neural synaptic weights.

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