Lead zirconate titanate behaviors in an LDMOS*

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The behaviors of lead zirconate titanate (PZT) deposited as the dielectric for high-voltage devices are investigated experimentally and theoretically. The devices demonstrate not only high breakdown voltages above 350 V, but also excellent memory behaviors. A drain current–gate voltage (I_D–V_G) memory window of about 2.2 V is obtained at the sweep voltages of ±10 V for the 350-V laterally diffused metal oxide semiconductor (LDMOS). The retention time of about 270 s is recorded for the LDMOS through a controlled I_D–V_G measurement. The LDMOS with memory behaviors has potential to be applied in future power conversion circuits to boost the performance of the energy conversion system.

Keywords: laterally diffused metal oxide semiconductor (LDMOS), lead zirconate titanate, memory behavior, retention

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1. Introduction

Lead zirconate titanate ($Pb(Zr,Ti)O_3$, PZT) has been widely investigated and integrated in ferroelectric random access memories and ferroelectric field effect transistors due to large remnant polarization and high permittivity.[1–7] In these applications, the PZT has mainly been used in low-voltage device fields.[8–14] Recently, high-permittivity dielectrics for power electronic applications have been extensively applied to realize high breakdown voltages and low on-resistance (R_{on}). However, most of these studies still remain at the simulation and theoretical analysis stages.[15–19]

In our previous work,[20] we have successfully fabricated a laterally diffused metal oxide semiconductor (LDMOS) covered by the PZT with high dielectric constants. The breakdown voltage is about 350 V, which is three times larger than that for the LDMOS covered by SiO_2, suggesting that the PZT is a potential candidate for future power applications. However, the behaviors of PZT in power applications have rarely been reported, thus making it an interesting and necessary research task.

Our experimental results show that the PZT LDMOS also has a memory characterization, which has not been reported. With the memory behavior, the LDMOS allows impulse driving instead of switching driving, which can be potentially used to design novel DC–DC circuit and improve the performance of the energy conversion system. The present work focuses mainly on the analysis of its memory performance.

2. Device structure and fabrication

Figure 1 shows the schematic cross section of the LDMOS, where a 600-nm PZT film covers a 20-nm SiO_2 insulator layer. The gate is also the field plate for the device. The channel length and width are 2 μm and 6000 μm, respectively. The N^- drift region is 80 μm. The n-channel LDMOS device was fabricated on a p-type Si (100) substrate. After the ion implantation into N^+ drain and source regions, the SiO_2 insulator layer was thermally grown. Then, the PZT film was deposited using radio-frequency magnetron sputtering. Subsequently, the PZT film was etched and contact windows were opened. Finally, the aluminum was deposited and patterned. We also fabricated counterparts with a SiO_2 dielectric for comparing with the novel devices. The current–voltage characteristics of the LDMOS were measured with an Agilent 4155B semiconductor parameter analyzer.

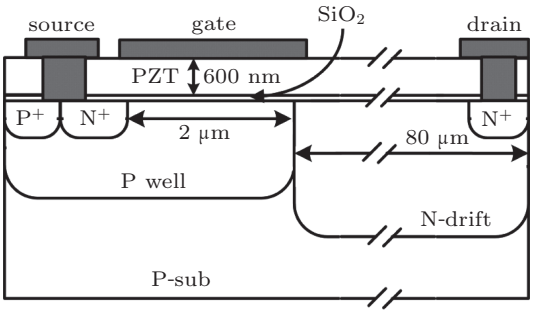


Fig. 1. Schematic cross section of the LDMOS with PZT.

3. Results and discussion

Figure 2(a) shows the drain current–gate voltage (I_D–V_G) characteristics of the LDMOS with PZT. The gate voltages

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were scanned from −10 to 10 V, and the counterclockwise hysteresis loops were observed. At the same time, we tested the SiO_2 counterpart and no hysteresis loop was observed (Fig. 2(b)). We suggest that the polarization charges formed in the PZT ferroelectric material are the main reason. Figure 3 shows the relationship of the gate voltage and the states of ferroelectric films. As shown in Fig. 3(a), the gate is driven to a positive voltage and the PZT is polarized, as shown in Fig. 3(e). The polarization induces charges and the Si surface approaches the inversion state, which can be regarded as writing "1". After the positive voltage is removed (Figs. 3(b) and 3(f)), the remnant polarization of the ferroelectric film is equivalent to adding a positive gate bias on the semiconductor. The effective gate voltage (V_{Geff}) can be expressed as

$$V_{\mathrm{Geff}} = V_{\mathrm{G}} + \frac{d_{\mathrm{Fe}}}{\varepsilon_0 \varepsilon_{\mathrm{Fe}}} P_{\mathrm{Fe}}, \tag{1}$$

where P_{Fe} is the remnant polarization, d_{Fe} and $\varepsilon_{\mathrm{Fe}}$ are the thickness and the dielectric constant of the ferroelectric film. Similarly, after writing "0", as shown in Figs. 3(c) and 3(d), the sign in formula (1) is minus.

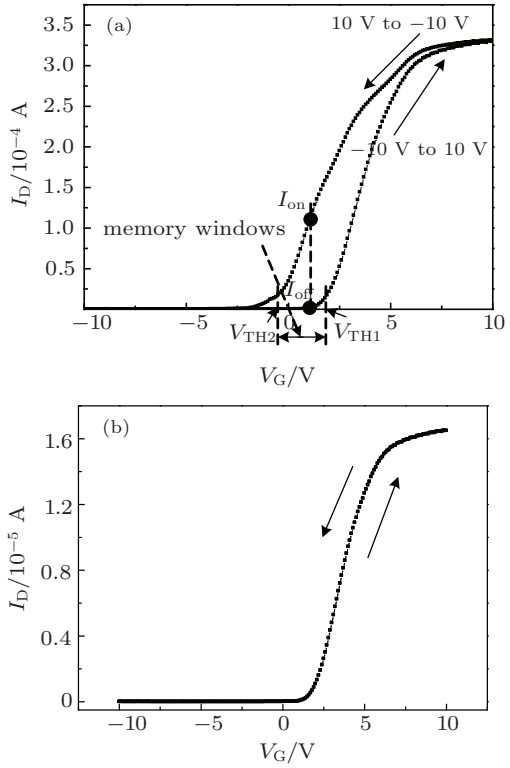


Fig. 2. Drain current–gate voltage (I_{D}–V_{G}) curves of (a) the fabricated n-channel LDMOS with PZT, and (b) the SiO_2 counterpart.

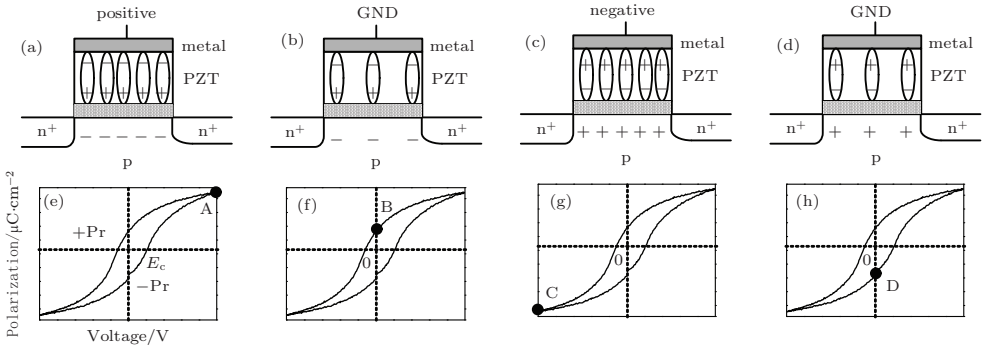


Fig. 3. The remnant polarization of ferroelectric films shifts the threshold of the LDMOS. (a) Under a positive voltage, (b) the positive voltage is off, (c) a negative bias, and (d) the negative bias is off. Panels (e)–(h) show the states of the ferroelectric films under corresponding gate voltages, respectively.

In the gradual-channel approximation, after "1" or "0" is written, the drain current of n-channel LDMOS in the linear regime is expressed as[21]

$$I_{\mathrm{D}} = \frac{W}{L} \mu_{\mathrm{n}} C_{\mathrm{stack}} (V_{\mathrm{Geff}} - V_{\mathrm{TH}}^0) V_{\mathrm{D}}, \tag{2}$$

where V_{TH}^0 is the threshold voltage independent of polarization, W and L are the channel width and length, μ_{n} is the electron mobility, and C_{Stack} is the gate stack capacitance given by $C_{\mathrm{Stack}} = C_{\mathrm{Fe}} C_{\mathrm{OX}} / (C_{\mathrm{Fe}} + C_{\mathrm{OX}})$, with C_{Fe} being the ferroelectric capacitance and $C_{\mathrm{OX}}$the oxide layer capacitance.

From Eqs. (1) and (2), we can see that even at the same V_{G}, the drain currents are different under different states, and therefore the polarization of the gate can be sensed by monitoring the drain current ratio of $I_{\mathrm{on}}/I_{\mathrm{off}}$. The experimental results show that the ratio $I_{\mathrm{on}}/I_{\mathrm{off}}$ of this LDMOS exceeds 10^3 at the gate bias voltage of 1.2 V.

Based on the foregoing discussion, the LDMOS can be used as a memory, which especially can be applicative in the high-voltage field. Generally, the memory window[22–24] is defined as the difference of the threshold voltage ($V_{\mathrm{TH1}} - V_{\mathrm{TH2}}$), as shown in Fig. 2(a). The memory window measured from the I_{D}–V_{G} characteristics of the LDMOS is about 2.2 V as V_{G} sweeps between −10 V and 10 V. Figure 4 shows that the memory window varies with the scanning voltage. We can see that the memory windows increase with increasing scanning voltage.

Furthermore, the retention characteristic has also been tested. To measure the retention characteristics in the on state and the off state, the voltages were applied from ±10 to 0 V

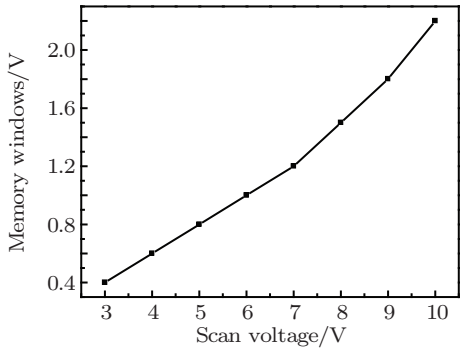


Fig. 4. Memory windows of the LDMOS with different scan voltages.

with a sweep rate of 5 V per point. In every point, voltage is hold for 0.1 s and delayed for a period of time, and then the subsequent points were tested. The drain current–gate voltage curves with delays of 60, 180, and 300 s were shown in Fig. 5(a). It can be seen that the memory windows are reduced with the increase in delay time. Figure 5(b) shows the variation of the drain currents as a function of the retention time for the fabricated LDMOS devices. The drain current on/off ratios gradually decrease by about one order of magnitude after 270 s. This means that the drain current difference can still be detected after 270 s.

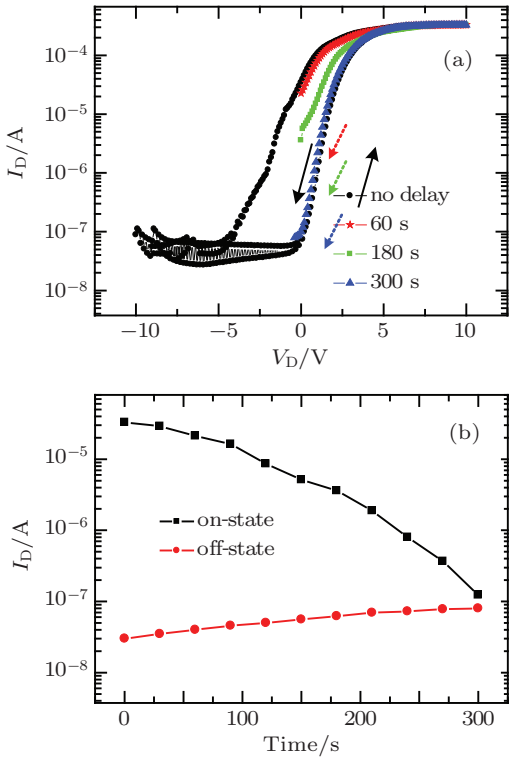


Fig. 5. (color online) (a) Drain current–gate voltage curves with delay times of 0, 60, 180, and 300 s. (b) The retention characteristics of the LDMOS at room temperature.

Figures 6(a) and 6(b) show the breakdown voltage characteristics of the LDMOS devices with PZT and SiO_2, respectively. The results show that the breakdown voltages have been improved two times by using the PZT films. As pointed out by Chen,[15] thin films of dielectric materials with high permittivity, which cover the semiconductor surface, can transmit electric flux into or extract flux from the semiconductor surface. Hence, the high permittivity of PZT can be used to prevent the occurrence of strong electric fields produced at the edges of some doped regions, thus improving the breakdown voltage of a lateral semiconductor device.

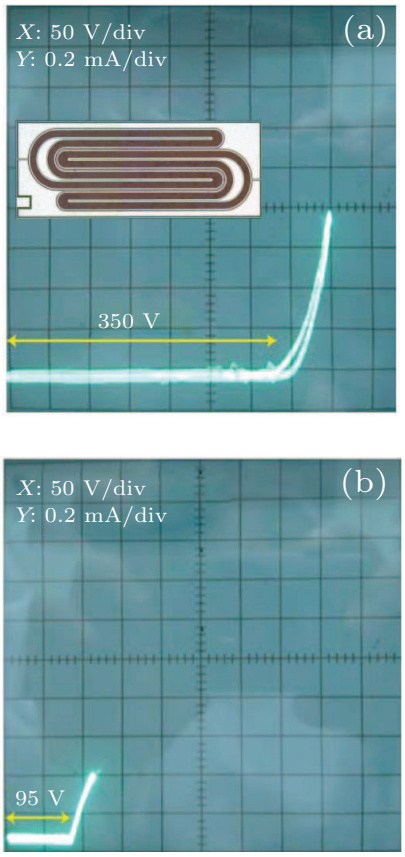


Fig. 6. (color online) Breakdown voltage characteristics of (a) the LDMOS with PZT. The inset shows the photo of the LDMOS. (b) The LDMOS with SiO_2.

4. Conclusion

We have proposed a ferroelectric material ($Pb(Zr_{0.53}, Ti_{0.47})$) as a novel substitution for high-k dielectric in conventional high-voltage LDMOS. Based on the high permittivity and the remnant polarization of the PZT films, the LDMOS devices not only have improved breakdown voltage, but also have a memory characteristic. The I–V memory window of about 2.2 V was obtained at a sweep voltage of $\pm$10 V for the 350-V LDMOS. The retention time of the LDMOS is about 270 s. These results pave a new way for the optimum design of high-performance LDMOS and extend new applications of the PZT. Taking advantage of such hysteresis behaviors of the PZT dielectric LDMOS, impulse driving for the LDMOS is available, and novel DC-DC circuit architectures are potential to be proposed to improve the performance of the power conversion systems.

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