A dual-gate and dielectric-inserted lateral trench insulated gate bipolar transistor on a silicon-on-insulator substrate*

Fu Qiang(付 强)†, Zhang Bo(张 波), Luo Xiao-Rong(罗小蓉), and Li Zhao-Ji(李肇基)

State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu 610054, *China*

(Received 18 January 2013; revised manuscript received 27 February 2013)

In this paper, a novel dual-gate and dielectric-inserted lateral trench insulated gate bipolar transistor (DGDI LTIGBT) structure, which features a double extended trench gate and a dielectric inserted in the drift region, is proposed and discussed. The device can not only decrease the specific on-resistance $R_{on,sp}$, but also simultaneously improve the temperature performance. Simulation results show that the proposed LTIGBT achieves an ultra-low on-state voltage drop of 1.31 V at 700 A·cm^{-2} with a small half-cell pitch of 10.5 μm, a specific on-resistance $R_{on,sp}$ of 187 mΩ·mm^2, and a high breakdown voltage of 250 V. The on-state voltage drop of the DGDI LTIGBT is 18% less than that of the DI LTIGBT and 30.3% less than that of the conventional LTIGBT. The proposed LTIGBT exhibits a good positive temperature coefficient for safety paralleling to handling larger currents and enhances the short-circuit capability while maintaining a low self-heating effect. Furthermore, it also shows a better tradeoff between the specific on-resistance and the turnoff loss, although it has a longer turnoff delay time.

Keywords: lateral trench insulated gate bipolar transistor, specific on-resistance, positive temperature coefficient, turnoff characteristic

PACS: 73.40.Ty, 85.30.De, 85.30.Pq **DOI:** 10.1088/1674-1056/22/7/077309

1. Introduction

Lateral insulated gate bipolar transistors (LIGBTs) have attractive features such as a low on-state voltage drop, high-current controllability, and easy integration. Silicon-on-insulator (SOI) technology provides many superior advantages,[1–3] such as high speed, superior isolation, and strong immunity to latch-up compared with bulk silicon. LIGBTs on SOI substrates have been widely used in power electronic applications because of the above features, especially in plasma display panel (PDP) driver integrated circuits (ICs). In PDP scan driver IC applications, a high current handling capability in the scan mode and a high current density with a low on-state voltage drop for the light emission discharge in the sustain mode are both necessary in LIGBTs.[4–7]

However, the supply voltage should be increased to improve the luminous efficacy of PDPs with a higher Xe concentration in discharge gas, leading to a larger device area and a higher cost.[8] So many efforts have been widely made to develop LIGBTs of small size, low cost, and high reliability. Trench gate technology was first introduced to IGBTs (LTIGBTs) to reduce the saturation voltage drops of the planar structures,[9–11] which was invented for the higher integration due to smaller cell pitches. By using a trench filled with oxide in the drift region of the device, the characteristics of the breakdown voltage and the specific on-resistance of reduced surface field (RESURF) laterally diffused metal oxide semiconductors (LDMOS) and LIGBT transistors based on SOI can be improved.[12–16]

The aim of this paper is to present a novel dual-gate and dielectric-inserted LTIGBT (DGDI LTIGBT) structure, which combines the merits of the dielectric trench and SOI technologies. Numerical simulations with MEDICI are performed to analyze the proposed DGDI LTIGBT in terms of the on-state characteristics and the temperature performance. We also compare the turnoff loss with that of the DI LTIGBT and the conventional LTIGBT.

2. Device structure and operation

The schematic cross-sectional view of the proposed DGDI LTIGBT structure on an SOI substrate is shown in Fig. 1(a). The DGDI LTIGBT features double trench gates and is dielectric-inserted: a deep oxide trench in the drift region, a buried trench gate inserted in the oxide trench, and another trench gate extended to the buried oxide layer. Figure 1(b) is the equivalent circuit. Here, T_{SOI}, T_{OX}, and B_{OX} are the thicknesses of the top silicon layer, the deep oxide trench, and the buried oxide layer, respectively; D_2 is the depth of gate 2; and N_D and P_{SUB} are the doping concentrations of the N-drift region and the P-substrate region, respectively. The device parameters listed in Table 1 and at room temperature are used.

*Project supported by the Major Program of the National Natural Science Foundation of China (Grant No. 2009ZX02305-006) and the National Natural Science Foundation of China (Grant No. 61076082).

†Corresponding author. E-mail: fuqiang17@gmail.com

© 2013 Chinese Physical Society and IOP Publishing Ltd

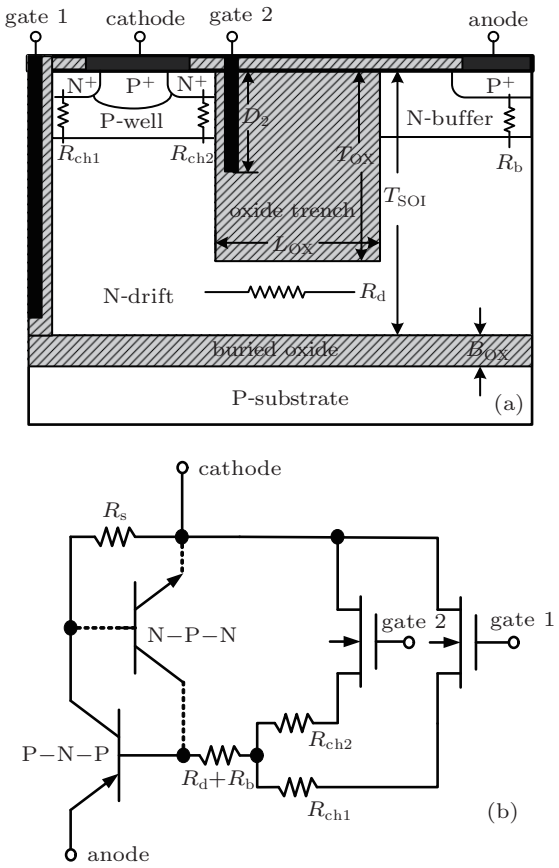


Fig. 1. (a) Schematic cross-sectional view of the proposed DGDI LTIGBT, and (b) its equivalent circuit. The DI LTIGBT structure is that without the gate 2 electrode.

Table 1. The key parameters in the device simulations.

Parameter	DGDI LTIGBT
Cell width W_{cell}/μm	10.5
SOI layer thickness T_{SOI}/μm	10
Buried oxide thickness B_{OX}/μm	1
N-drift doping N_D/cm^{-3}	2.5×10^{15}
Oxide trench depth T_{OX}/μm	7
Oxide trench length L_{OX}/μm	4
P-substrate doping P_{SUB}/cm^{-3}	6×10^{14}
P-well doping N_{PW}/cm^{-3}	3×10^{17}
N-buffer doping N_{NB}/cm^{-3}	1.5×10^{17}

As we know, the ratio of the maximum electric field occurring inside the silicon, E_{si}, to that in the insulator inside the trench, E_{ox}, is the inverse of their permittivities: $E_m/E_{ox} = \varepsilon_{ox}/\varepsilon_{si}$. The lateral critical electric field strength is increased due to the lower permittivity of the oxide ($\varepsilon_{ox} = 3.9$) than that of Si ($\varepsilon_{si} = 11.9$), as shown in Fig. 2. The oxide trench, therefore, leads to electric field reshaping, and an enhanced RESURF effect, which results in a much smaller cell pitch compared to that of the conventional LTIGBT structure for maintaining nearly the same breakdown voltage $V_{B,off}$. The extended double trench gates can widen the conduction area, enhance the electron injection efficiency, and make the current flow line distribution on the cathode side uniform. They will also decrease the on-state resistance and improve the temperature performance of the proposed DGDI LTIGBT structure.

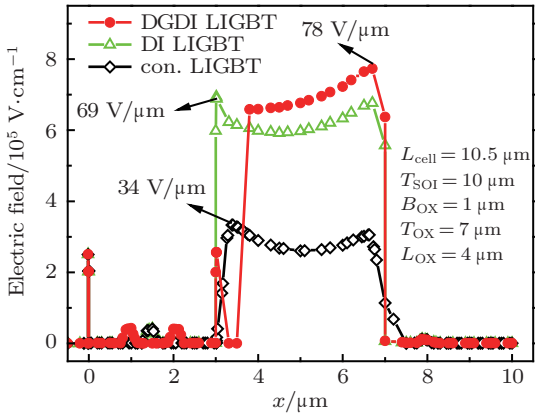


Fig. 2. Electric field distributions in the x direction at the surface for the same cell pitch devices.

The on-state characteristics of the IGBT structure can be obtained using the MOSFET/PNP model. The on-state resistance of an LTIGBT transistor can be written as the sum of a channel component and a drift-region component (shown in Fig. 1(b))

$$R_{total} = R_{ch} + R_d + R_b. \tag{1}$$

For the proposed DGDI LTIGBT structure, the channel component can be written as

$$R_{ch} = R_{ch1} \| R_{ch2} = \left(\frac{1}{R_{ch1}} + \frac{1}{R_{ch2}} \right)^{-1}. \tag{2}$$

Generally, there are two main modes in IGBT device operation: the bipolar portion at low current densities, and the mobility portion at high current densities, which dictate the temperature behavior. Differentiating the expression of the anode current density J_A with respect to temperature yields

$$\frac{1}{J_A}\frac{\partial J_A}{\partial T} = \frac{1}{\mu_{ni}}\frac{\partial \mu_{ni}}{\partial T} + \frac{1}{\beta_{pnp}}\frac{\partial \beta_{pnp}}{\partial T}, \tag{3}$$

where C_{ox} is the capacitance per unit area; μ_{ni} is the average electron mobility; and β_{pnp} is the common-emitter current gain of the P-N-P transistor. These two effects counter each other, so at a low current density, the voltage drop across the junction and the reduction in the drift resistance due to a higher PNP gain β_{pnp} will dominate and result in a negative temperature coefficient of the on-state voltage drop; while at a higher current density, the degradation of the mobility will dominate and result in a positive temperature coefficient of the on-state voltage drop.

3. Results and discussion

3.1. On-state and turnoff characteristics

Figure 3 shows the on-state I–V characteristics of the conventional LTIGBT (con. LTIGBT), the DI LTIGBT, and the

proposed DGDI LTIGBT. It indicates that the proposed DGDI LTIGBT has lower on-state voltage drop and higher transconductance than the conventional LTIGBT and the DI LTIGBT due to the higher doping concentration in the N-drift region and the widened effective conduction area caused by the extended trench gate and gate 2. This would result in the enhancement of the electron injection efficiency and the corresponding conductivity modulation effect. The N-drift doping concentration of the DI LTIGBT and the DGDI LTIGBT is 2.5×10^{15} cm^{-3}, while that of the conventional structure is 1.2×10^{15} cm^{-3}. The on-state voltage drop V_{on} at J_A =700 A· cm^{-2}, 300 K of the DGDI LTIGBT (shown in the inset of Fig. 3) is 1.31 V, while those of the DI LTIGBT and the conventional LTIGBT are 1.59 V and 1.88 V, respectively. The on-state voltage drop of the DGDI LTIGBT is 18% less than that of the DI LTIGBT and 30.3% less than that of the conventional LTIGBT. The ultra-low on-state voltage drop suggests that the DGDI LTIGBT can significantly reduce the energy loss during on-state operation.

Figure 4 shows the tradeoff relation between the specific on-resistance $R_{on,sp}$ and the breakdown voltage $V_{B,off}$ of the DGDI LTIGBT structure and different state-of-the-art technologies.[16–22] The experimental and simulated data reported previously are shown in Fig. 4 and Table 2. It can be seen that the DGDI LTIGBT has the lowest $R_{on,sp}$ in the 250 V-class LTIGBTs, which shows that the performance is the best in power applications. The results of the state-of-the-art devices show that for the DI LIGBT structure, the $R_{on,sp}$ is 330 mΩ·mm^2, and $V_{B,off}$ is 210 V;[16] for the DI LDMOS structure, the $R_{on,sp}$ is 700 mΩ·mm^2, and $V_{B,off}$ is 250 V;[20] and for the multi-emitter LIGBT structure, the $R_{on,sp}$ is 237 mΩ·mm^2, and $V_{B,off}$ is 270 V.[22] Whereas in the proposed DGDI LTIGBT, the current density is improved to 700 A·cm^{-2} at V_{on} = 1.31 V, the $R_{on,sp}$ is 187 mΩ·mm^2, and the half-cell width is reduced to 10.5 μm with a breakdown voltage of 250 V by using double trench gates and the dielectric-inserted technology.

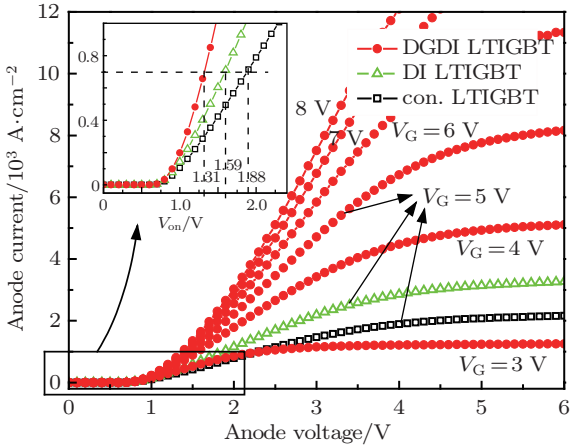


Fig. 3. (color online) The on-state $I-V$ characteristics of the conventional LTIGBT, the DI LTIGBT, and the proposed DGDI LTIGBT, where $V_{G1} = V_{G2}$ = 3–8 V. The inset shows the on-state voltage drop characteristics at J_A = 700 A·cm^{-2}, $V_{G1} = V_{G2}$ = 5 V, 300 K.

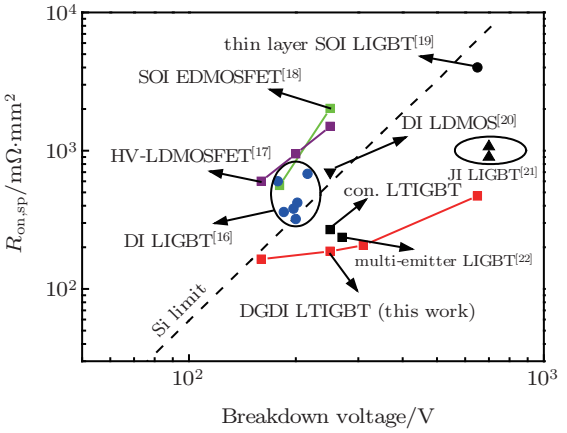


Fig. 4. (color online) The tradeoff relation of the specific on-resistance $R_{on,sp}$ at J_A = 700 A/cm^2 with the breakdown voltage $V_{B,off}$.

Table 2. Comparison of the experimental and simulated data reported, and the data of this work.

Device structure	Half-cell pitch/μm	$V_{B,off}$ /V	$R_{on,sp}$/mΩ·mm^2	T_{max}/K
DGDI LTIGBT	10.5	250	187	346
DI LTIGBT	10.5	250	227	382
Con. LTIGBT	10.5/18	105/250	193/268	344.5/386
DI LTIGBT[16]	13.5	210	330	–
Multi-emitter LIGBT[22]	35	270	237	–

Figure 5 shows the influences of the gate 2 depth (D_2) on the specific on-resistance and the turnoff loss for the DGDI LTIGBT. The increase in D_2 makes the proposed DGDI LTIGBT show a lower on-state voltage drop and specific on-resistance, while the turnoff loss of the DGDI LTIGBT is kept unchanged. The tradeoff between the specific on-resistance and the turnoff loss obtained by varying the doping concentrations of the P-anode is comparatively illustrated in Fig. 6. The proposed DGDI LTIGBT shows greatly superior tradeoff characteristics than the other two. It is also worth mentioning that the turnoff delay time t_d of the DGDI LTIGBT is longer than that of the DI LTIGBT due to a larger gate parasitic capacitance for the DGDI LTIGBT.

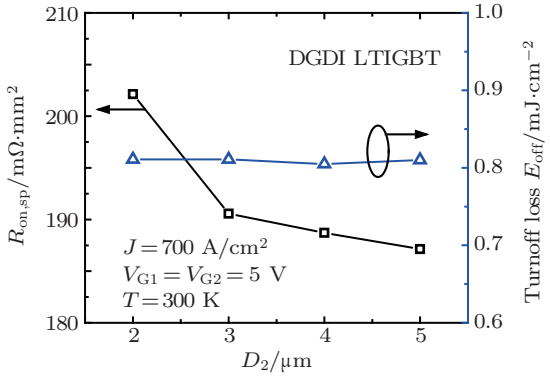


Fig. 5. (color online) The dependence of the specific on-resistance and the turnoff loss on the gate 2 depth.

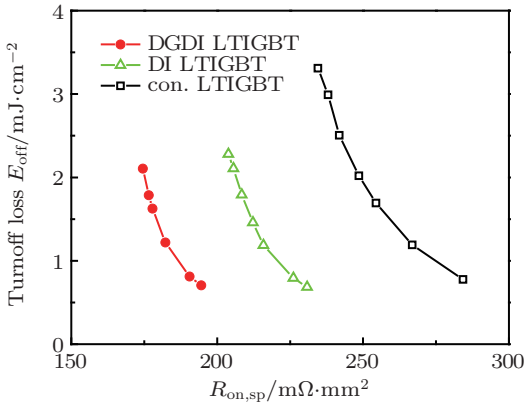


Fig. 6. (color online) The tradeoff between the specific on-resistance and the turnoff loss.

3.2. Temperature performance

The dependence on temperature and the on-state voltage drop of the DGDI LTIGBT are shown in Fig. 7. Similarly to the DI LTIGBT and the conventional LTIGBT, the DGDI LTIGBT has a negative temperature coefficient at operating current density $J_A = 700$ A·cm^{-2} and low gate voltage $V_{G1} = V_{G2} = 5$ V, because the bipolar conduction mode in the DGDI LTIGBT dominates at high temperature. However, it should be noted that the zero thermal coefficient (ZTC) of the DGDI LTIGBT is at $J_A = 3000$ A·cm^{-2}. Above the ZTC, the temperature coefficient becomes positive and causes

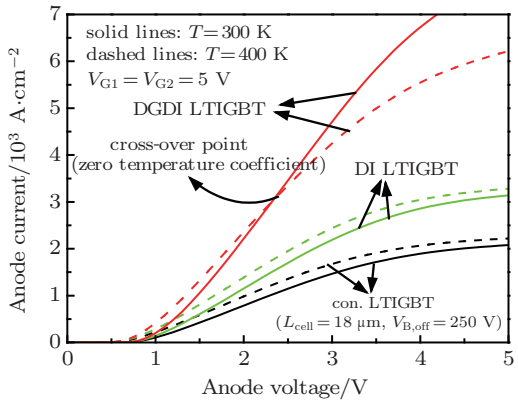


Fig. 7. (color online) Comparison of the on-state characteristics at various temperatures.

the mobility degradation, which is shown by the decrease in the anode saturation current (shown in Fig. 7). Due to the ultra-low on-state voltage of the DGDI LTIGBT, it is likely to increase the operating current density to a higher level (> 3000 A·cm^{-2}) to achieve a positive temperature coefficient. This therefore suggests that the on-state characteristics of the chips exhibit a good positive temperature coefficient for safety paralleling to handling larger currents.

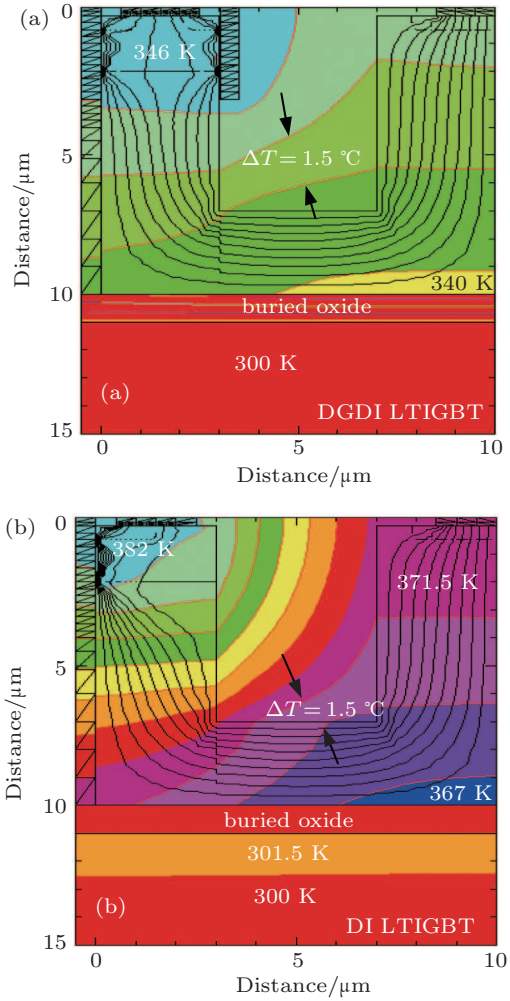


Fig. 8. (color online) The 2D distributions of the temperature and current of (a) the proposed DGDI LTIGBT, and (b) the DI LTIGBT.

Figures 8(a) and 8(b) show the two-dimensional (2D) temperature distributions and the current distributions of the DI LTIGBT and the proposed DGDI LTIGBT. The vertical temperature comparison of the above structures in the cathode region is shown in Fig. 9. The substrate temperature is fixed at 300 K, and V_{G1} and V_{G2} are 5 V. The temperature is extracted at a current of 2×10^{-4} A·μm^{-1}. The heat is mainly dissipated through the heat sink attached to the substrate; the temperature thus decreases from the surface to the substrate. The maximum temperatures, T_{max}, in these devices are also given in Table 2. The temperature of the DGDI LTIGBT is the lowest of the above structures with the 250V-class $V_{B,off}$, but that of the conventional LTIGBT is the highest in Fig. 9. That

is because of the widened effective conduction area caused by the double trench gates and the uniform current distribution on the cathode side (shown in Fig. 8). It can be concluded that DGDI LTIGBT devices can enhance the short-circuit capability and achieve a larger maximum dissipation power, while maintaining a low self-heating effect (SHE).

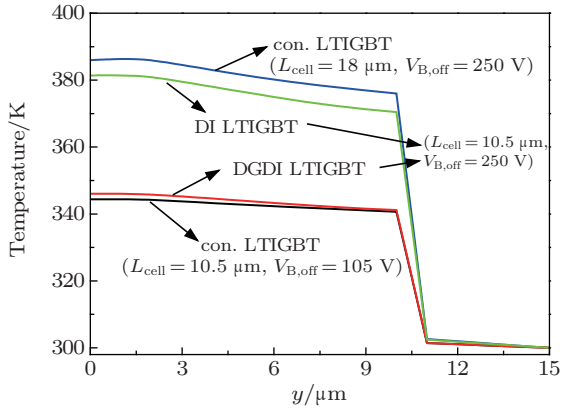


Fig. 9. (color online) The vertical temperature distributions in the cathode region.

4. Conclusion

In summary, we have proposed a novel dual-gate and dielectric-inserted LTIGBT with an ultra-low on-state voltage drop of 1.31 V at 700 A·cm^{-2}. The half-cell pitch of the IGBT is reduced to 10.5 μm and the specific on-resistance $R_{on,sp}$ is decreased to 187 mΩ·mm^2 with a breakdown voltage of 250 V by using double trench gates and the dielectric-inserted technology. It also shows a better tradeoff between the specific on-resistance and the turnoff loss. Furthermore, the on-state characteristics of the proposed LTIGBT exhibit a good positive temperature coefficient and maintain a low SHE for safety paralleling to handling larger currents.

References

[1] Schwantes S, Florian T, Stephan T, Graf M and Dudek V 2005 *IEEE Trans. Electron Dev.* **52** 1649
[2] Qiao M, Zhuang X, Wu L J, Zhang W T, Wen H J, Zhang B and Li Z J 2012 *Chin. Phys. B* **21** 108502
[3] Vanhoenacker-Janvier D, El Kaamouchi M and Si Moussa M 2008 *IET Circuits Devices Syst.* **2** 151
[4] Sumida H, Maiguma T, Shimizu N and Kobayashi H 2007 *Proc. IEEE ISPSD* p. 229
[5] Wu L J, Hu S D, Zhang B, Luo X R and Li Z J 2011 *Chin. Phys. B* **20** 087101
[6] Lu D H, Mizushima T, Kitamura A, Iwamuro N and Fujishima N 2008 *Proc. IEEE ISPSD* p. 32
[7] Kim J, Roh T M, Kim S G, Song Q S, Lee D W, Koo J G, Cho K I and Ma D S 2001 *IEEE Trans. Electron Dev.* **48** 1256
[8] Uchida G, Uchida S, Akiyama T, Kajiyama H and Shinoda T 2010 *J. Appl. Phys.* **107** 103311
[9] Chang H R, Baliga B J, Kretchmer J W and Piacente P A 1987 *Proc. IEDM Tech. Dig.* p. 674
[10] Cai J, Sin J K O, Mok P K T, Ng W T and Lai P P T 1999 *IEEE Trans. Electron Dev.* **46** 1788
[11] Khanna V K 2003 *The Insulated Gate Bipolar Transistor (IGBT): Theory and Design* (New York: IEEE Press) p. 517
[12] Luo X R, Yao G L, Chen X, Wang Q, Ge R and Udrea F 2011 *Chin. Phys. B* **20** 028501
[13] Hu X R, Zhang B, Luo X R, Wang Y G, Lei T F and Li Z J 2012 *Chin. Phys. B* **21** 078502
[14] Xiao H, Zhang L J, Huang R, Song F, Wu D, Liao H L, Wong W S and Wang Y Y 2009 *IEEE Electron Device Lett.* **30** 386
[15] Luo X R, Fan J, Wang Y, Lei T, Qiao M, Zhang B and Udrea F 2011 *IEEE Electron Device Lett.* **32** 185
[16] Lu D H, Jimbo S and Fujishima N 2005 *Proc. IEEE IEDM Tech. Dig.* p. 381
[17] Kobayashi K, Yanagigawa H, Mori K, Yamanaka S and Fujiwara A 1998 *Proc. IEEE ISPSD* p. 141
[18] Lee M R, Oh-Kyong Kwon, Lee S S, Lee I H, Yang I S, Paek J H, Hwang L Y, Ju J I, Lee B H and Lee C J 1999 *Proc. IEEE ISPSD* p. 285
[19] Letavic T, Petruzzello J, ClaeS J, Eggenkamp P, Janssen E and van der WaI A 2006 *Proc. IEEE ISPSD* p. 1
[20] Varadarajan K R, Chow T P and Wang J 2007 *Proc. IEEE ISPSD* p. 233
[21] Terashima T and Moritani J 2007 *Proc. IEEE ISPSD* p. 225
[22] Sakano J, Shirakawa S, Hara K, Yabuki S, Wada S, Noguchi J and Wada M 2010 *Proc. IEEE ISPSD* p. 83