Effect of the Si-doped $In_{0.49}Ga_{0.51}P$ barrier layer on the device performance of $In_{0.4}Ga_{0.6}As$ MOSFETs grown on semi-insulating GaAs substrates*

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(Received 18 December 2012; revised manuscript received 5 February 2013)

$In_{0.4}Ga_{0.6}As$ channel metal–oxide–semiconductor field-effect transistors (MOSFETs) with and without an Si-doped $In_{0.49}Ga_{0.51}P$ barrier layer grown on semi-insulating GaAs substrates have been investigated for the first time. Compared with the $In_{0.4}Ga_{0.6}As$ MOSFETs without an $In_{0.49}Ga_{0.51}P$ barrier layer, $In_{0.4}Ga_{0.6}As$ MOSFETs with an $In_{0.49}Ga_{0.51}P$ barrier layer show higher drive current, higher transconductance, lower gate leakage current, lower subthreshold swing, and higher effective channel mobility. These $In_{0.4}Ga_{0.6}As$ MOSFETs (gate length 2 μm) with an $In_{0.49}Ga_{0.51}P$ barrier layer exhibit a high drive current of 117 mA/mm, a high transconductance of 71.9 mS/mm, and a maximum effective channel mobility of 1266 $cm^2/(V{\cdot}s)$.

Keywords: metal–oxide–semiconductor field-effect transistor, InGaAs, InGaP, Al_2O_3

PACS: 73.40.Qv, 71.55.Eq, 77.55.D– **DOI:** 10.1088/1674-1056/22/7/077306

1. Introduction

As Si complementary metal–oxide–semiconductor (CMOS) scaling comes to its fundamental physical limits, continuous device scaling and performance improvements are faced with a great challenge. In order to maintain Moore's law, tremendous efforts have been made to look into alternative channel materials beyond Si, such as germanium, InGaSb, and InGaAs.[1–3] One solution is to integrate high-performance, high electron mobility InGaAs channel NMOS with high performance, high hole mobility Ge channel PMOS for next-generation CMOS technology. Recently, high crystalline quality Ge thin film on a lattice matched GaAs substrate has been obtained,[4] which makes it possible to integrate Ge PMOS and InGaAs NMOS on the GaAs substrate, and excellent performance Ge PMOS using $HfO_2/Al_2O_3/GeO_x$ as the gate oxide has been reported.[3] However, InGaAs channel NMOSFETs grown on semi-insulating GaAs substrates still need to be further studied. The main obstacle for the InGaAs metal–oxide–semiconductor field-effect transistor (MOSFET) is the lack of high-quality thermo-dynamically stable gate dielectrics. Recently, surface channel InGaAs MOSFETs with atomic layer deposited (ALD) Al_2O_3,[2] HfO_2,[5] ZrO_2[6] have shown improved interface passivation and stability, however, the effective channel mobility is still relatively low compared to that of the bulk InGaAs. The buried channel InGaAs NMOSFET is considered as one of the most promising NMOSFETs for next-generation CMOS technology as it combines a high electron mobility channel and thermal stable MOS interface, which will exhibit excellent output and transfer characteristics.

A buried channel $In_xGa_{1-x}As$ ($x < 0.25$) MOSFET with 3.5 nm InAlP native oxide as the gate dielectric[7] exhibits promising radio-frequency performance, however, the drain current density is only 165 mA/mm at $V_{ds} = 2$ V, which might be due to the low indium composition and the high energy barrier at the source/drain region. For the $In_{0.49}Ga_{0.51}P/In_xGa_{1-x}As$ high-electron-mobility transistor (HEMT) structure, the $In_xGa_{1-x}As$ electron mobility increases as the indium composition increases, but the sheet resistance also increases owing to the increase in the conduction band gap offset between $In_{0.49}Ga_{0.51}P$ and $In_xGa_{1-x}As$.[8] Moreover, although the effective channel mobility of the buried channel InGaAs MOSFETs with molecular beam epitaxy (MBE) InP/InAlAs and an InP barrier layer[9,10] is larger than that of the surface channel MOSFETs, the undoped barrier layer increases the source and drain resistance and degrades the on-state performance.[11] In this work, buried channel $In_{0.4}Ga_{0.6}As$ MOSFETs on GaAs substrates with and without an Si-doped $In_{0.49}Ga_{0.51}P$ barrier layer are proposed and investigated for the first time. An $In_{0.4}Ga_{0.6}As$ MOSFET (gate length $L_g = 2$ μm) with a 5 nm Si-doped $In_{0.49}Ga_{0.51}P$ barrier layer and 10 nm ALD Al_2O_3 dielectric exhibits high performance, showing a higher drive current, transconductance, effective channel mobility and lower gate leakage current than

*Project supported by the National Basic Research Program of China (Grant Nos. 2011CBA00605 and 2010CB327501), the National Natural Science Foundation of China (Grant No. 61106095), and the National Science and Technology Major Project of the Ministry of Science and Technology of China (Grant No. 2011ZX02708-003).

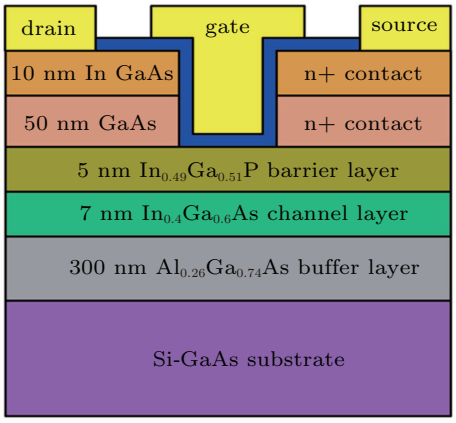
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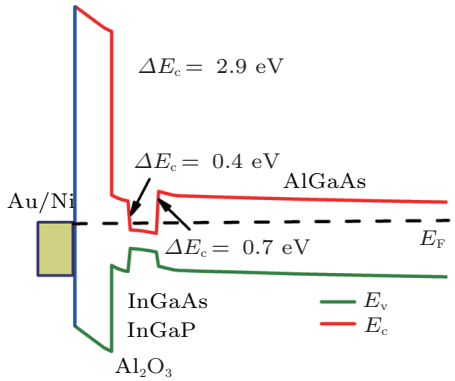
$In_{0.4}Ga_{0.6}As$ MOSFETs without a doped $In_{0.49}Ga_{0.51}P$ barrier layer.

2. Device fabrication

Figure 1(a) shows the cross section of the $In_{0.4}Ga_{0.6}As$ MOSFET structure. The layer structure was grown on a semi-insulating GaAs substrate by metal–organic chemical vapor deposition (MOCVD) and consisted of a 300 nm $Al_{0.26}Ga_{0.74}As$ buffer layer (with Si planar doping at 3 nm below the InGaAs channel), a 7 nm $In_{0.4}Ga_{0.6}As$ strained quantum well channel layer, a 5 nm $In_{0.49}Ga_{0.51}P$ barrier layer, and an n^+ contact layer including a 50 nm GaAs cap layer and a 10 nm $In_{0.54}Ga_{0.46}As$ cap layer. The sheet resistance was 100 Ω/□, and the room-temperature Hall mobility was larger than 8000 $cm^2/(V{\cdot}s)$. The n^+ contact layer was selectively removed by phosphate acid solution (H_3PO_4:H_2O_2:H_2O=3:1:50). The $In_{0.49}Ga_{0.51}P$ barrier layer was removed by hydrochloric acid solution (HCl: H_3PO_4=1:4). After a recess, the wafers were pretreated by diluted hydrochloric acid solution and ammonia-based solution. Then, 10 nm Al_2O_3 was deposited by ALD as the gate dielectric, followed by 400 °C post-deposition annealing in an N_2 ambient. The Ni/Au gate metal, Ni/Ge/Au/Ge/Ni/Au source, and drain Ohmic contacts were then deposited by e-beam evaporation, respectively, after selectively etching Al_2O_3 using a buffered oxide etch (BOE). Finally, a rapid thermal annealing (RTA) process at 270 °C for 3 min in an N_2 ambient was carried out. The sheet resistance and the contact resistance of the source and drain regions were determined to be only 100 Ω/□ and 0.1 Ω·mm, respectively, using the transmission line method, which were much smaller than those of the InGaAs channel MOSHEMTs[12,13] and MOSFETs[7,14] with an undoped $In_{0.49}Ga_{0.51}P$ barrier layer. The reason for this may be that the thick $In_{0.54}Ga_{0.46}As$ cap layer and the Si-doped $In_{0.49}Ga_{0.51}P$ barrier layer significantly lowers the barrier height at the source and drain. Figure 1(b) shows the energy band diagram for $In_{0.4}Ga_{0.6}As$ channel MOSFETs with an $In_{0.49}Ga_{0.51}P$ barrier layer.



(a)



(b)

Fig. 1. (color online) (a) Cross-section view of the substrate structure, and (b) the energy band diagram for $In_{0.4}Ga_{0.6}As$ MOSFETs with an $In_{0.49}Ga_{0.51}P$ barrier layer.

3. Results and discussion

The transfer and output characteristics of $In_{0.4}Ga_{0.6}As$ MOSFETs ($L_g = 2$ μm) with and without an $In_{0.49}Ga_{0.51}P$ barrier layer are investigated. As shown in Figs. 2(a) and 2(b), the threshold voltage V_{th} of the $In_{0.54}Ga_{0.46}As$ MOSFET without an $In_{0.49}Ga_{0.51}P$ barrier layer is –0.1 V, while it is –0.6 V for the MOSFET with an $In_{0.49}Ga_{0.51}P$ barrier layer, indicating that the doped $In_{0.49}Ga_{0.51}P$ barrier reduces the gate control over the channel. The threshold voltage shift is believed to be due to the positive charge in the Si-doped $In_{0.49}Ga_{0.51}P$ barrier layer as it is depleted. The energy band diagram of the $In_{0.4}Ga_{0.6}As$ MOSFETs with $In_{0.49}Ga_{0.51}P$ barrier layer is shown in Fig. 1(b). It is also observed that the peak transconductance g_m of the $In_{0.4}Ga_{0.6}As$ MOSFETs with an $In_{0.49}Ga_{0.51}P$ barrier layer is 71.9 mS/mm, which is five times larger than that (14.2 mS/mm) of the $In_{0.4}Ga_{0.6}As$ MOSFETs without an $In_{0.49}Ga_{0.51}P$ barrier layer. As shown in Figs. 2(c) and 2(d), the maximum drive current of the devices with an $In_{0.49}Ga_{0.51}P$ barrier layer is 117 mA/mm, which is three times higher than that of the devices without an $In_{0.49}Ga_{0.51}P$ barrier layer. The drain current I_d versus drain bias V_d curves of $In_{0.4}Ga_{0.6}As$ MOSFETs with an Si-doped $In_{0.49}Ga_{0.51}P$ barrier layer show cross-over characteristics, which result from the fact that some channel electrons spill over into the lower mobility $In_{0.49}Ga_{0.51}P$ layer when the gate bias V_g is high (≥ 3 V).[10]

Figure 3(a) shows the the drain current I_d versus gate bias V_g curves at a drain bias V_{ds} of 50 mV for the MOSFETs with and without an $In_{0.49}Ga_{0.51}P$ barrier layer. The off current density of the $In_{0.4}Ga_{0.6}As$ MOSFETs with an $In_{0.49}Ga_{0.51}P$ barrier layer is 3×10^{-4} mA/mm at $V_g - V_{th} = -0.9$ V, while that of the $In_{0.4}Ga_{0.6}As$ MOSFETs without an $In_{0.49}Ga_{0.51}P$ barrier layer is 3×10^{-3} mA/mm at $V_g - V_{th} = -0.9$ V, indicating that the $In_{0.49}Ga_{0.51}P$ barrier layer results in a reduction of the off current by an order of magnitude. Moreover, the $In_{0.49}Ga_{0.51}P$ barrier layer also helps the MOSFETs achieve a lower gate

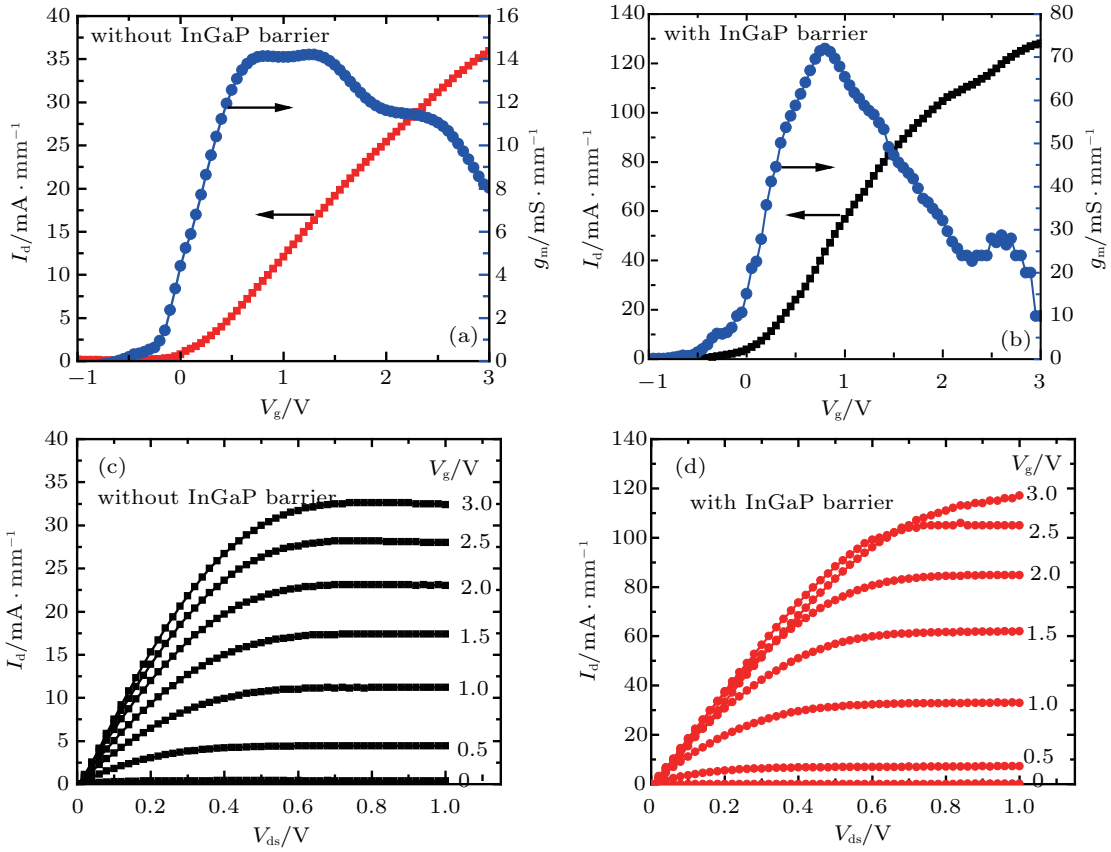


Fig. 2. (color online) Panels (a) and (b) show the transfer characteristics of InGaAs MOSFETs without and with a doped $In_{0.49}Ga_{0.51}P$ barrier layer. The gate length is 2 μm. Panels (c) and (d) show I_d–V_d at V_g from 0 to 3 V with a step of 0.5 V for InGaAs MOSFETs without and with a doped $In_{0.49}Ga_{0.51}P$ barrier.

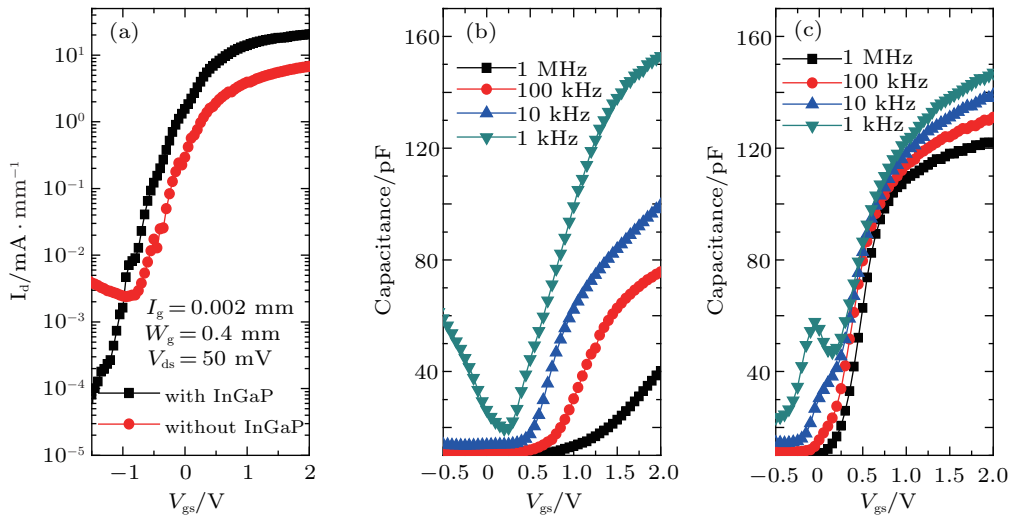


Fig. 3. (color online) (a) The I_d–V_g at $V_{ds} = 50$ mV for InGaAs MOSFETs with and without a doped $In_{0.49}Ga_{0.51}P$ barrier. Panels (b) and (c) show the split C–V of InGaAs MOSFETs without and with a doped $In_{0.49}Ga_{0.51}P$.

leakage current density compared with the device without the $In_{0.49}Ga_{0.51}P$ barrier layer (not shown here). As shown in Figs. 3(b) and 3(c), the frequency dispersion of the split C–V curves of $In_{0.4}Ga_{0.6}As$ MOSFETs with an $In_{0.49}Ga_{0.51}P$ layer is much smaller than that without it. This phenomenon may result from two facts. One is that the MBE $In_{0.49}Ga_{0.51}P/In_{0.4}Ga_{0.6}As$ interface is superior to the $Al_2O_3/In_{0.4}Ga_{0.6}As$ obtained by the ALD technology. The other is that the doped $In_{0.49}Ga_{0.51}P$ layer makes the $In_{0.4}Ga_{0.6}As$ channel move away from the $Al_2O_3/In_{0.49}Ga_{0.51}P$ interface, resulting in the effective interface state density of $In_{0.4}Ga_{0.6}As$ MOSFETs with an $In_{0.49}Ga_{0.51}P$ barrier layer being much lower than that without the $In_{0.49}Ga_{0.51}P$ barrier layer.

Figure 4 shows the effective channel mobility of the $In_{0.4}Ga_{0.6}As$ buried channel MOSFETs with a 4 nm $In_{0.49}Ga_{0.51}P$ barrier layer, the $In_{0.6}Ga_{0.4}As$ surface channel MOSFETs,[15] and the $In_{0.7}Ga_{0.3}As$ buried channel MOSFET with a 4 nm InP barrier layer.[16] All measurements are performed with the split *C*–*V* method by using the devices with a gate length of 20 μm. Although it is well known that a higher indium content results in higher electron mobility, it is observed that the peak effective channel mobility of $In_{0.4}Ga_{0.6}As$ MOSFETs with an $In_{0.49}Ga_{0.51}P$ barrier layer is 1266 $cm^2/(V{\cdot}s)$, which is much larger than that of the higher indium composition $In_{0.53}Ga_{0.47}As$ surface channel MOSFETs, while it is smaller than that of the $In_{0.7}Ga_{0.3}As$ buried MOSFETs with an InP barrier layer due to the much lower indium composition.

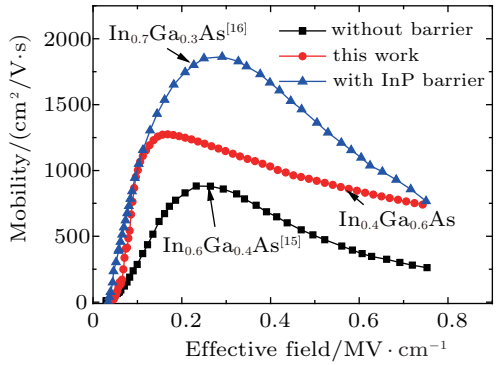


Fig. 4. (color online) Effective channel mobility as a function of the effective field for different indium composition $In_xGa_{1-x}As$ MOSFETs.

4. Conclusion

High-performance $In_{0.4}Ga_{0.6}As$ MOSFETs with and without an $In_{0.49}Ga_{0.51}P$ barrier layer on a GaAs substrate were fabricated and investigated. The Si-doped $In_{0.49}Ga_{0.51}P$ barrier layer exhibits its excellent passivation effect on the interface to increase the effective channel mobility of the $In_{0.4}Ga_{0.6}As$ MOSFETs with an $In_{0.49}Ga_{0.51}P$ barrier layer. The $In_{0.4}Ga_{0.6}As$ MOSFETs with an $In_{0.49}Ga_{0.51}P$ barrier layer show higher drive current, higher transconductance, lower gate leakage current, lower subthreshold swing, and higher effective channel mobility than those without an $In_{0.49}Ga_{0.51}P$ barrier layer. These $In_{0.4}Ga_{0.6}As$ MOSFETs ($L_g = 2$ μm) with an $In_{0.49}Ga_{0.51}P$ barrier layer exhibit a high drive current of 117 mA/mm, a high transconductance of 71.9 mS/mm, and a maximum effective channel mobility of 1266 $cm^2/(V{\cdot}s)$.

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