Interfacial characteristics of Al/Al_2O_3/ZnO/n-GaAs MOS capacitor*

Liu Chen(刘 琛)†, Zhang Yu-Ming(张玉明), Zhang Yi-Men(张义门), and Lü Hong-Liang(吕红亮)

School of Microelectronics, Key Laboratory of Wide Band-Gap Semiconductor Materials and Devices, Xidian University, Xi'an 710071, *China*

(Received 27 August 2012; revised manuscript received 12 March 2013)

The interfacial characteristics of Al/Al_2O_3/ZnO/n-GaAs metal–oxide–semiconductor (MOS) capacitor are investigated. The results measured by X-ray photoelectron spectroscopy (XPS) and high-resolution transmission electron microscopy (HRTEM) show that the presence of ZnO can effectively suppress the formations of oxides at the interface between the GaAs and gate dielectric and gain smooth interface. The ZnO-passivated GaAs MOS capacitor exhibits a very small hysteresis and frequency dispersion. Using the Terman method, the interface trap density is extracted from *C*–*V* curves. It is found that the ZnO layer can effectively improve the interface quality.

Keywords: gate dielectric, Terman method, interface trap density

PACS: 67.30.hp, 68.37.–d, 61.72.uj **DOI:** 10.1088/1674-1056/22/7/076701

1. Introduction

The metal–oxide–semiconductor field-effect transistor (MOSFET) has been the workhorse of the semiconductor technology for a couple of decades. Following the Moore's law, Si-based MOSFET is approaching to the dimension limits. III–V compound materials, such as GaAs, are receiving special attention as future channel materials due to their high electron mobilities, large energy band gaps, and high critical breakdown fields compared with Si. However, a major problem is the lack of high quality and thermodynamically stable dielectric that can be used to fabricate high quality GaAs MOSFET.[1] High interface trap density[2] can lower the channel electron mobility, thus leading to the degradation of device electrical properties. For GaAs MOS devices, the values of interface trap density reported by different authors were between 5×10^{11} $cm^{-2}\cdot eV^{-1}$–6.9×10^{12} $cm^{-2}\cdot eV^{-1}$,[3] but for Si/SiO_2 MOS, it is 10^{10} $cm^{-2}\cdot eV^{-1}$. In order to effectively reduce the interface trap density, lots of efforts have been devoted to high *k* dielectrics[4] and the passivation layer. It was found that high *k* materials, such as HfO_2,[5] Ga_2O_3,[6] and TiO_2 deposited by atomic layer deposition (ALD) or molecular beam epitaxy (MBE), together with Ge[7] or TN[8] as the passivation layer, can lead to the reduction of the interface trap density to some extent. In this paper, the interfacial properties of Al/Al_2O_3/ZnO/n-GaAs MOS capacitors are investigated.

2. Experiment

The GaAs wafers used in this paper were single-polished, n-type (100) oriented, Si-doped with a doping concentration of 4×10^{17} cm^{-3}–5×10^{17} cm^{-3}. Prior to deposition, the samples were first chemically degreased using acetone, cleaned in HCl for 1 min for native oxide removal, and then dipped in NH_4OH for 1 min to remove elemental As, and dried in N_2. The ALD technique was used to deposit a thin ZnO interface passivation layer (IPL) of 2 nm, and followed by Al_2O_3 deposition with a thickness of 9 nm. Post deposition annealing (PDA) was carried out in an N_2 ambient at 500 °C for 1 min by rapid thermal annealing. Al metal deposited by sputtering was used to form the gate electrode with an area of 5.8×10^{-3} cm^2, and low resistance Ohmic contact on the back side of the wafers. XPS was performed to analyze the interface on the GaAs surface, in which the XPS data were collected using K-Alpha (made by VG, UK). HRTEM was adopted to investigate the interfacial structure of Al_2O_3/ZnO/n-GaAs. The capacitance–voltage (*C*–*V*) measurements were carried out using Keithley 590.

3. Results and discussion

Figure 1 shows the high-resolution transmission electron microscopy (HRTEM) image of Al_2O_3/ZnO gate stack on n-GaAs. It can be found clearly that the interface on n-GaAs is smooth and the thickness of ZnO layer is 2 nm measured by HRTEM and ellipsometry.

Figure 2 shows the *C*–*V* characteristics of Al/Al_2O_3/n-GaAs and Al/Al_2O_3/ZnO/ n-GaAs MOS capacitors measured at a frequency of 100 kHz. It can be observed that the accumulation capacitance for the Al_2O_3/ZnO gate stack is higher than that for single Al_2O_3, though the physical thickness for Al_2O_3/ZnO gate stack is thicker than that for the directly de-

*Project supported by the National Basic Research Program of China (Grant No. 2010CB327505), the National Defense Advance Research Foundation, China (Grant No. 9140A08030511DZ111), and the National Defense Advance Research Project, China (Grant No. 51308030306).

†Corresponding author. E-mail: lcxd710071@126.com

© 2013 Chinese Physical Society and IOP Publishing Ltd

posited Al_2O_3. The result is likely to be explained by the fact that the presence of ZnO on n-GaAs can suppress the low-k interfacial layer growth on n-GaAs surface and cause higher equivalent dielectric constant of the dielectric stack, thus leading to higher accumulation capacitance. The hysteresis was determined by sweeping the gate voltage from inversion to accumulation and then sweeping back to obtain the difference between flatband voltages. The reduced hysteresis for n-GaAs MOS capacitor with the deposition of ZnO prior to Al_2O_3 may be attributed to the decrease of interface trap density and the improvement on dielectric quality.

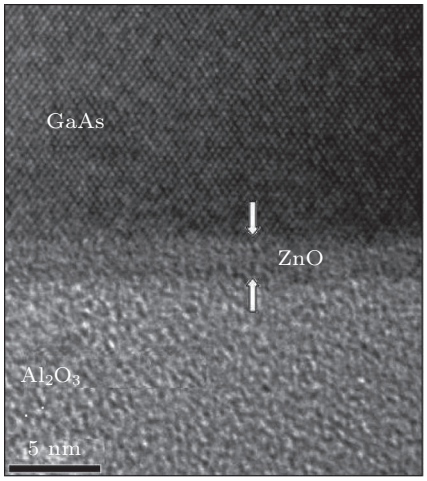


Fig. 1. The HRTEM image of the Al_2O_3/ZnO gate stack on n-GaAs.

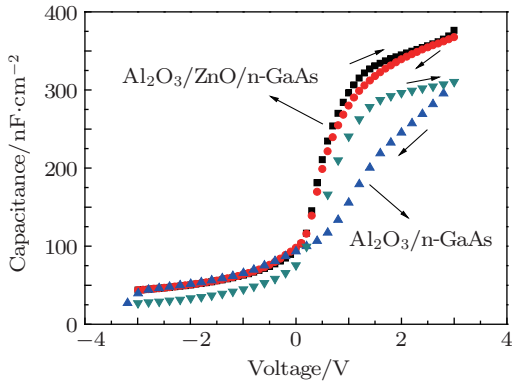


Fig. 2. (color online) The C–V characteristics of GaAs MOS capacitor with and without ZnO as the passivation layer measured at 100 kHz.

Figure 3 shows the frequency variation of the C–V characteristics for GaAs MOS capacitors with and without ZnO. The frequency dispersion could be possibly attributed to the interface trap density. Compared with the Al/Al_2O_3/n-GaAs capacitors, the Al/Al_2O_3/ZnO/ n-GaAs capacitors have very small frequency dispersion, thus suggesting a lower interface trap density, ultimately a better interface quality.

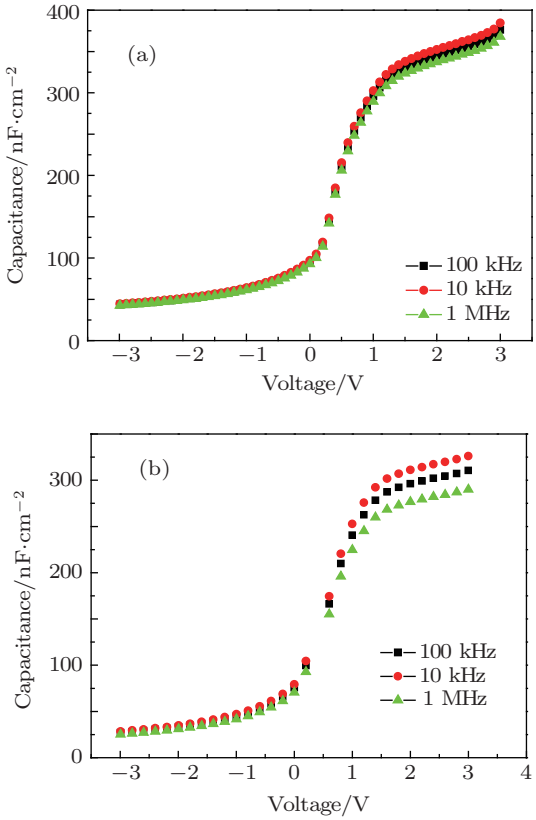


Fig. 3. (color online) (a) The C–V characteristics of ZnO passivated GaAs MOS capacitor measured in a frequency range from 10 kHz to 1 MHz, and (b) the C–V characteristics of GaAs MOS capacitor without ZnO measured at different frequencies.

In order to analyze the interface trap density on the GaAs surface, D_{it} can be extracted from capacitance–voltage curves using the Terman method as follows:

$$C(\psi_s) = \frac{1}{1/C_{ox} + 1/C_s(\psi_s)}, \tag{1}$$

$$\psi_s = \frac{\varepsilon_s q N}{2C_s^2}, \tag{2}$$

$$C_{it}(\psi_s) = C_{ox}\left[\left(\frac{d\psi_s}{dV_g}\right)^{-1} - 1\right] - C_s(\psi_s), \tag{3}$$

$$D_{it}(\psi_s) = \frac{C_{it}(\psi_s)}{q}, \tag{4}$$

$$E_t - E_i = q\phi_B - q\psi_s, \tag{5}$$

where C_{ox} is the insulator capacitance, ψ_s the surface potential of GaAs, V_g the gate voltage, C_s the substrate capacitance, ε_s the relative dielectric constant of the substrate, E_t the energy level of the interface trap state, E_i the intrinsic Fermi level, $q\phi_B$ the doping-induced Fermi level in the bulk GaAs, q the unit charge, and N the doping concentration of the substrate. Based on the experimental C–V curves, we can extract the values of C_s using Eq. (1). Then the relationship between ψ_s and V_g can be extracted from Eq. (2). Fitting the experimental data by Matlab, an approximate functional relationship between ψ_s and V_g can be developed. According to Eqs. (3), (4), and (5),

we can obtain the curves of D_{it} versus $E_t - E_i$ as presented in Fig. 4.

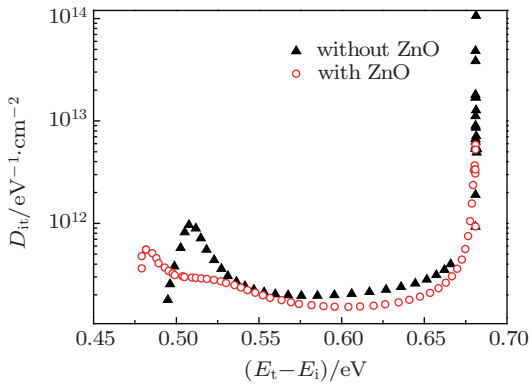


Fig. 4. (color online) Curves of the D_{it} versus $E_t - E_i$ for the cases with and without ZnO.

It can be obviously seen that the interface trap density for Al/Al_2O_3/ZnO/n-GaAs MOS capacitor is lower than that without ZnO, which means that the presence of a thin layer of ZnO can effectively reduce the interface trap density, thus improving the interfacial properties on the GaAs surface. The midgap D_{it} for our MOS capacitor is 2.6×10^{11} $cm^{-2}\cdot eV^{-1}$, while the values of D_{it} for Zr_O2/Si/p-GaAs and HfAlO/SiO_2/p-GaAs are 3×10^{12} $cm^{-2}\cdot eV^{-1}$ and 5×10^{11} $cm^{-2}\cdot eV^{-1}$, respectively.

Figures 5(a) and 5(b) show the Ga 3d spectra for Al_2O_3 films deposited for the samples without and with ZnO passivation. The peak at 19.2 eV is due to Ga–As bond, while the peak at 21 eV is due to Ga–O bond. From Fig. 5(a), it can be seen clearly that large amounts of Ga–O are observed for n-GaAs MOS without ZnO passivation. However, the amount of Ga–O decreases dramatically for ZnO IPL-passivated n-GaAs MOS capacitor. From Figs. 5(c) and 5(d), it can also be seen that the amount of As–O[9] (the peak at 44.50 eV) has an obvious reduction as a thin ZnO layer is inserted between GaAs and Al_2O_3. The presented results show that Ga–O and As–O that are related to the interface states can significantly degrade the interfacial properties. However, the ZnO interface passivation layer can act as the oxygen reaction barrier and the presence of ZnO on n-GaAs effectively reduces the Ga and As oxides and suppresses the formation of low k interfacial layer on the GaAs surface,[10] thus improving the interface quality. It could be the reason why the interface trap density is reduced after the deposition of ZnO in Fig. 4 and why the presence of ZnO can lead to higher accumulation capacitance in Fig. 2.

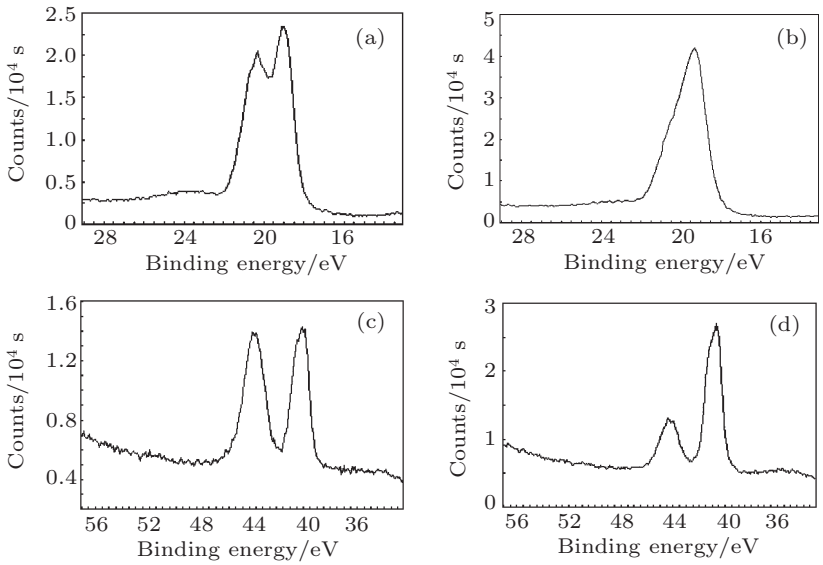


Fig. 5. XPS spectra for Al_2O_3/n-GaAs and Al_2O_3/ZnO/n-GaAs: (a) Ga 3d XPS spectra without ZnO, (b) Ga 3d XPS spectra with ZnO, (c) As 3d XPS spectra without ZnO, (d) As 3d XPS spectra with ZnO.

Looking into this issue, it is tightly related to the crystalline structure of ZnO, where each zinc atom is surrounded by four oxygen atoms at the corners of a tetrahedron, and *vice versa*. The structure is a well-knit one, which has notable properties including large bond strength indicated by the large cohesive energy (−7.692, −7.679, and −7.455 eV for ZnO with wurtzite, zinc-blende, and rocksalt phases, respectively) and high melting point (1975 °C) as well as extreme stability of exciton indicated by the large exciton binding energy (60 meV). Owing to its superior structure stability, the structure of ZnO remains the same during the deposition of Al_2O_3, which makes ZnO a strong barrier between Al_2O_3 and GaAs,

effectively reducing the chance of the contact of Ga and As on the surface of GaAs with the oxygen atoms in Al_2O_3. On the other hand, ZnO has such a high exciton binding energy that the Zn–O bonds cannot be easily destroyed, which means that it is almost impossible for ZnO to react with Ga and As at the interface, though there exist oxygen atoms in ZnO.

4. Conclusions

In this paper, the studies on the *C–V* characteristics of Al/Al_2O_3/n-GaAs and Al/Al_2O_3/ZnO/n-GaAs MOS capacitors have been presented with extracting the interface trap density using the Terman method. It can be seen that a thin layer of ZnO (2 nm) can effectively lower D_{it}. XPS results show that the amounts of Ga–O and As–O bonds reduce dramatically due to inserting the ZnO layer between Al_2O_3 and n-GaAs. XPS data may explain the reduction of D_{it} and the increase of accumulation capacitance. The incorporation of ZnO interface passivation layer provides improved *C–V* characteristics with low hysteresis and frequency dispersion. In general, a ZnO layer between GaAs and high *k* dielectric provides a good way to passivate the GaAs surface and improve the interface quality for future application in MOS devices.

Acknowledgment

We acknowledge Fudan Microelectronics Institute for the deposition of ZnO and Al_2O_3, also we are thankful to 204 Research Institution for providing XPS test and HRTEM measurement.

References

[1] Li C, Zhuang Y Q, Zhang L and Bao J L 2012 *Chin. Phys. B* **21** 048501

[2] Chen Y T, Huang P, Jimmy L, Patrick S and Veksler D 2012 *International Symposium on VLSI Technology, Systems, and Applications* (VLSI-TSA), April 23–25, 2012, Hsinchu, Taiwan, p. 1

[3] Shahrjerdi D, Tutuc E and Banerjee S K 2007 *Appl. Phys. Lett.* **91** 3503

[4] Guo D F, Geng W G, Lan W, Huang C M and Wang Y Y 2005 *Acta Phys. Sin.* **54** 5901 (in Chinese)

[5] Xu J P, Chen W B, Lai P T, Li Y P and Chan C L 2007 *Chin. Phys.* **16** 529

[6] Passlack M, Medendorp N, Gregory R and Braddock D 2003 *Appl. Phys. Lett.* **83** 5262

[7] Shahrjerdi D, Oye M M, Holmes A L Jr and Banerjee S K 2006 *Appl. Phys. Lett.* **89** 3501

[8] Gao F, Lee S J, Chi D Z, Balakumar S and Kwong D L 2007 *Appl. Phys. Lett.* **90** 2904

[9] Dalapati G K, Sridhara A, Wong A S W, Chia C K, Lee S J and Chi D 2007 *Appl. Phys. Lett.* **91** 2101

[10] Brennan B, Zhernokletov D M, Dong H, Hinkle C L, Kim J and Wallace R M 2012 *Appl. Phys. Lett.* **100** 1603