High-voltage super-junction lateral double-diffused metal–oxide semiconductor with a partial lightly doped pillar*

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A novel super-junction lateral double-diffused metal–oxide semiconductor (SJ-LDMOS) with a partial lightly doped P pillar (PD) is proposed. Firstly, the reduction in the partial P pillar charges ensures the charge balance and suppresses the substrate-assisted depletion effect. Secondly, the new electric field peak produced by the P/P$^-$ junction modulates the surface electric field distribution. Both of these result in a high breakdown voltage (BV). In addition, due to the same conduction paths, the specific on-resistance ($R_{on,sp}$) of the PD SJ-LDMOS is approximately identical to the conventional SJ-LDMOS. Simulation results indicate that the average value of the surface lateral electric field of the PD SJ-LDMOS reaches 20 V/μm at a 15 μm drift length, resulting in a BV of 300 V.

Keywords: super-junction, lateral double-diffused metal–oxide semiconductor, partial lightly doped pillar, electric field modulation, breakdown voltage

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1. Introduction

With the development of smart power-integrated circuits (SPICs), the demand for power devices that can be easily integrated into SPICs has been increasing more and more. For a commonly used integrated device, the lateral double-diffusion metal–oxide semiconductor field-effect transistor (MOSFET)/(LDMOS) acts as an important constituent in power electronics applications. The super-junction (SJ) concept[1] used in the LDMOS[2,3] improves the tradeoff characteristics between the breakdown voltage and the specific on-resistance ($R_{on,sp}$). Unfortunately, the N pillars of the conventional SJ-LDMOST are depleted by neighboring P pillars as well as by the P substrate, while the P pillars are depleted by neighboring N pillars only. This is called the substrate-assisted depletion effect. This effect causes a charge imbalance and results in the decrease of the breakdown voltage (BV). To eliminate it, several new structures have been reported.[4–13]

In this paper, an SJ-LDMOS with partial lightly doped P pillar (PD) is proposed to suppress the substrate-assisted depletion effect. Owing to the decrease in the charges in the P pillar, the charge balance is achieved and the new peak appearing at the P/P$^-$ junction modulates the surface electric field distribution. Thus, a higher BV is obtained according to the simulation results.

2. Device structure and mechanism

The proposed PD SJ-LDMOS is illustrated in Fig. 1. The key feature of the device is that the P pillar in the SJ region is split into two distinct parts. The first one is the heavily doped P pillar, of which the doping concentration is equal to that of the N pillar. The second is the lightly doped P pillar with a doping concentration of N_P and a length L_P. The cross section along the AA' plane is shown in Fig. 2. On the one hand, the use of the lightly doped P pillar causes a reduction in the p-type charge density, thereby ensuring the charge balance among the N pillar, the P pillar, and the P substrate. The substrate-assisted depletion effect therefore can be suppressed. On the other hand, the electric field peak which occurs at the P/P$^-$ junction modulates the electric field distribution in the N pillar, which causes a uniform distribution of the surface electric field.

Three-dimensional (3D) device simulations are carried out by Sentaurus[14] in order to demonstrate the performance of the PD SJ-LDMOS. The PD SJ-LDMOS is compared with the conventional SJ-LDMOS, and the relevant device parameters are listed in Table 1.

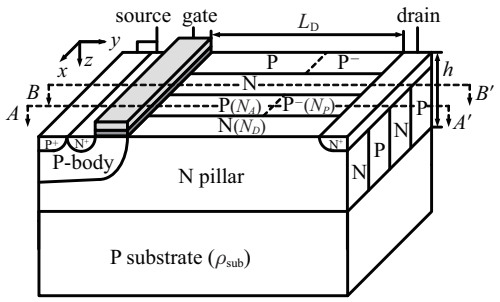


Fig. 1. Three-dimensional (3D) view of the PD SJ-LDMOS.

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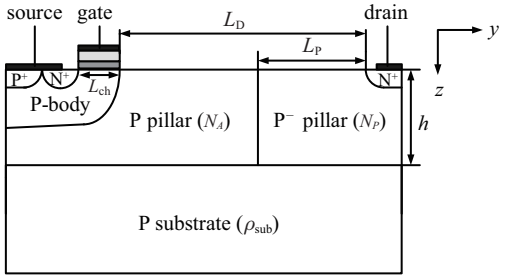


Fig. 2. Cross section along the AA' plane in Fig. 1.

Figures 3(a) and 3(b) show the potential distributions of the PD SJ-LDMOS and conventional SJ-LDMOS at the same drift length of 15 μm, respectively. For the conventional SJ-LDMOS, the potential contours concentrate at the drain and the breakdown voltage deteriorate sharply. However, for the PD SJ-LDMOS, part of the potential contours are pulled out toward the source due to the charge balance caused by the lightly doped P pillar, and the curvature effect of the drain is alleviated. It is clear that the equipotential contours of the PD SJ-LDMOS are evenly spaced and the depletion area is extended into the source region in comparison with the conventional SJ-LDMOS. The BV of the PD SJ-LDMOS reaches 300 V compared with 100 V for the conventional SJ-LDMOS, which increases about 300%. Figures 3(c) and 3(d) show the lateral electric field profiles at the silicon surface and vertical electric field, respectively. Another electric field peak P_K appears at the P/P$^-$ junction in the P pillar. Due to the modulation effect of this new electric field P_K, the lateral electric field distribution of the PD SJ-LDMOS is more uniform than that of the conventional SJ-LDMOS, which concentrates at the drain. The electric field of the PD SJ-LDMOS also increases strongly around the source ($E_1 > E_2$) and reduces around the drain ($E_4 < E_3$). The depletion area of the PD SJ-LDMOS is then further extended into the substrate. Thus the substrate sustains a higher blocking voltage and the BV can be improved.

Table 1. Device specifications.

Parameter	PD SJ-LDMOS	Conventional SJ-LDMOS
Drift length, L_D/μm	15	15
Pillar width, $W_N = W_P$/μm	1	1
Pillar height, h/μm	1, 2, 4	1, 2, 4
Substrate resistivity, $\rho_{sub}/\Omega \cdot$ cm	65	65
Pillar doping, $N_D = N_A/10^{16}$ cm^{-3}	2	2
Effective channel length, L_{ch}/μm	2	2
Lightly doped P pillar length, L_P/μm	1 to 14	–
Lightly doped P pillar doping, $N_P/10^{16}$ cm^{-3}	0.8 to 1.2	–

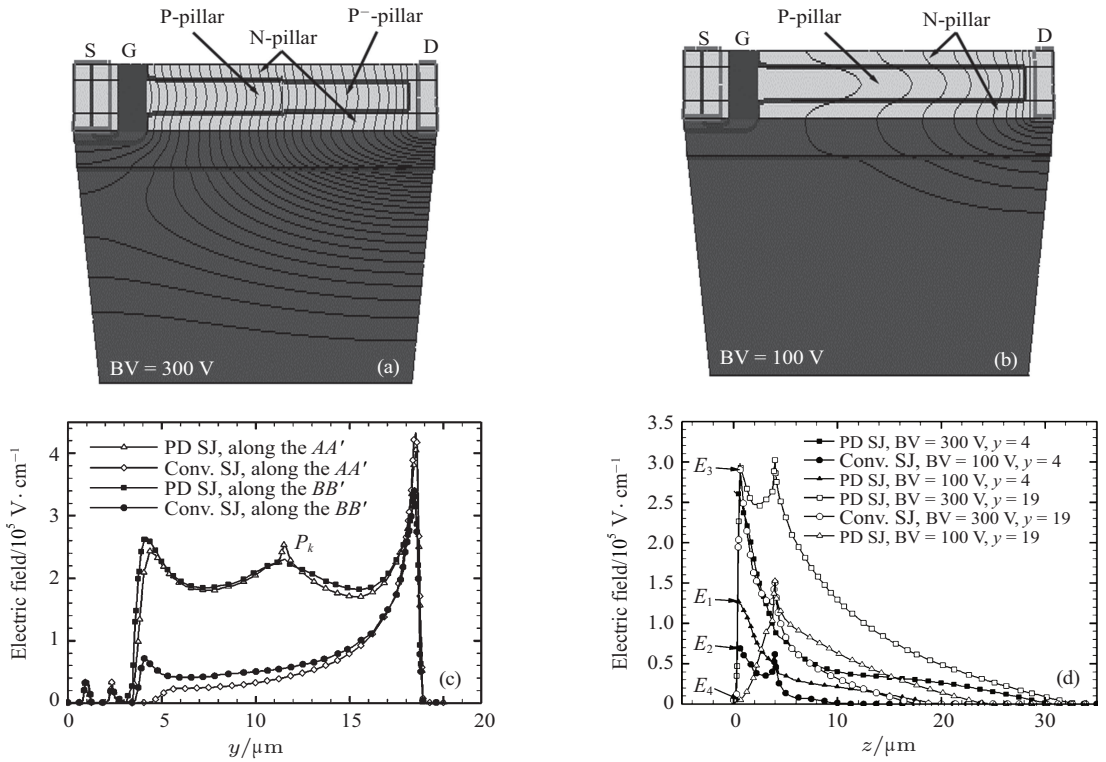


Fig. 3. Equipotential contour distributions for the (a) PD SJ-LDMOS, and (b) conventional SJ-LDMOS (10 V/contour). (c) Lateral electronic field distribution along the AA' and BB' plane. (d) Vertical electronic field distribution around the drain ($y = 19$ μm) and the source ($y = 4$ μm). In panel (d), E_1 and E_4 are the electronic field peaks of the PD SJ-LDMOS around the source and the drain, respectively, and E_2 and E_3 are the electronic field peaks of the conventional SJ-LDMOS around the source and the drain, respectively, when the drain voltage is 100 V. PD SJ-LDMOS: $L_P = 7.5$ μm, $N_P = 1 \times 10^{16}$ cm^{-3}, $h = 4$ μm; conventional SJ-LDMOS: $h = 4$ μm.

3. Results and discussion

The doping concentration N_P and the length L_P of the lightly doped P pillar are important parameters in the design of the PD SJ-LDMOS that must ensure the charge balance among the P pillar, the N pillar, the P^- pillar, and the P substrate. This requires these key parameters to satisfy the reduced surface field (RESURF) principle,[15,16] that is,

$$N_{\text{eff}} \cdot h = \left(N_D - N_A + \frac{L_p}{L_D} \Delta N \right) \cdot h \approx \text{const}, \tag{1}$$

where $\Delta N = N_A - N_P$. If $N_D = N_A$, it can be obtained that

$$\alpha \Delta N \cdot h \approx C, \tag{2}$$

where $\alpha = L_P / L_D$, C is a constant. This means that the reduced dose of the P pillar ensures the charge balance and suppresses the substrate-assisted depletion effect.

The relationships between the BV and the L_P at different N_P for the PD SJ-LDMOS are shown in Fig. 4(a). It can be observed that for the PD SJ-LDMOS, the maximum BV occurs when $\alpha = 1/2$. Hence, in the discussion below, the L_P is adopted to be 1/2 L_D. The BVs of the PD SJ-LDMOS as a function of N_P at different values of height h are shown in Fig. 4(b). It is obvious that the maximum BV of the PD SJ-LDMOS increases as the height increases, and the optimal values of N_P are 1×10^{16} cm^{-3} for the case of $h = 4$ μm, 0.5×10^{16} cm^{-3} for the case of $h = 2$ μm, and -0.6×10^{16} cm^{-3} for the case of $h = 1$ μm. It is worth noting that the N_P is negative when $h = 1$ μm. This can be explained by the fact that from Eq. (2), N_P is given by

$$N_P \approx N_A - \frac{C}{\alpha \cdot h}. \tag{3}$$

Under the condition of $N_A < C/(\alpha \cdot h)$, $N_P < 0$, which means that the lightly doped P pillar is changed into the N pillar. Moreover, the values of the dose $\alpha \Delta N \cdot h$ that correspond to N_P are 2×10^{12} cm^{-2} ($h = 4$ μm), 1.5×10^{12} cm^{-2} ($h = 2$ μm), 1.3×10^{12} cm^{-2} ($h = 1$ μm), respectively. A larger $\alpha \Delta N \cdot h$ is needed to ensure the charge balance due to the further extension of the depletion area in the substrate at the higher maximum BV.

In order to demonstrate the influence of the charge imbalance of the SJ region on the BV, the charge imbalance factor is defined as

$$\eta = \frac{N_A - N_D}{N_D}. \tag{4}$$

In Fig. 4(c), the BV of the PD SJ-LDMOS and conventional SJ-LDMOS at the different charge imbalance factors are compared. The PD SJ-LDMOS achieves a charge balance between the pillars and the P substrate to ensure the suppression of the substrate-assisted depletion effect at maximum BV, while the conventional SJ-LDMOS shows a charge imbalance factor of 15%. The maximum BV increases ΔV ($\Delta V = 85$ V in this case) compared with that of the conventional SJ-LDMOS. The dependences of the BV on ΔN with N_{eff} remain constant for the cases of different heights, and are shown in Fig. 4(d). The fixed N_{eff} (i.e. N_D and $N_A + N_P$ are kept unchanged in this case) ensures

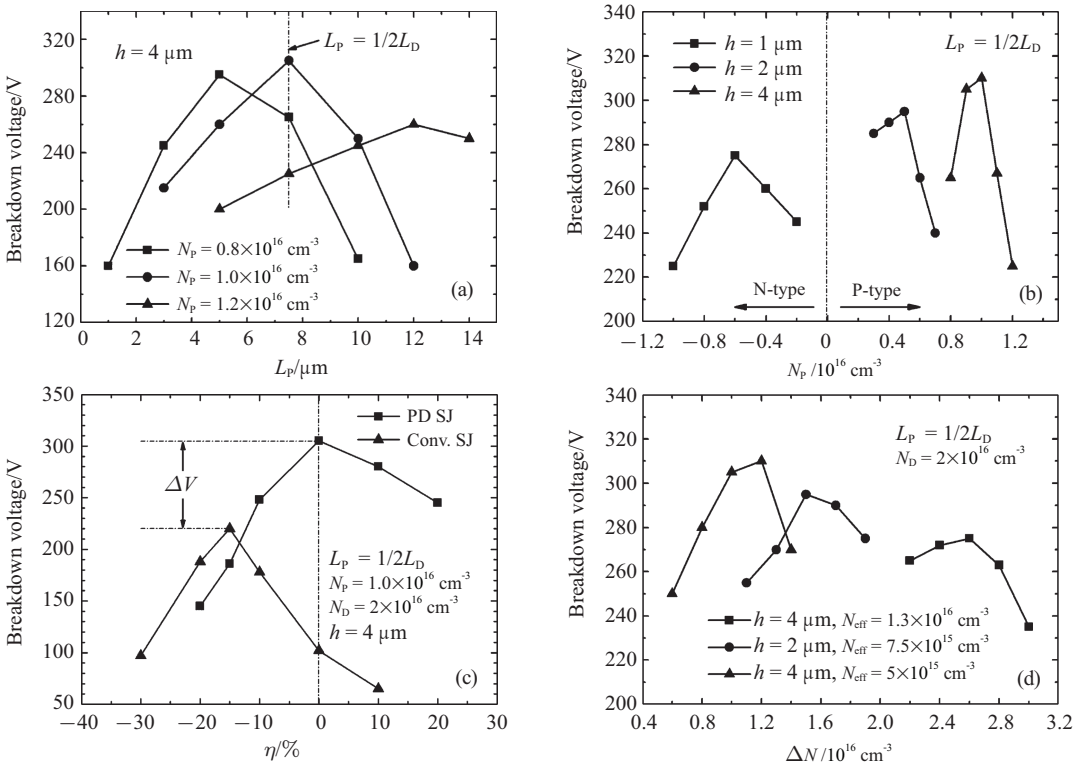


Fig. 4. (color online) The BVs of the PD SJ-LDMOS versus (a) drift length L_P, (b) the concentration of the P^- pillar N_P, (c) the charge imbalance factor η, and (d) the concentration difference ΔN between the P pillar and the P^- pillar.

the charge balance. It is found that the difference in the ΔN concentration between the P pillar and the P^- pillar has an optimal value. If ΔN is too high, then the BV of the PD SJ-LDMOS can be reduced due to the premature breakdown of the P/P^- junction. However, if ΔN is too low, then the BV also deteriorates because the modulation effect of the electric field peak at the P/P^- junction is very poor. So a well-designed ΔN must make the modulation effect obvious, but prevent the premature breakdown of the P/P^- junction.

Figure 5 shows the dependences of the $R_{on,sp}$ and BV on the height h. As height h increases, the value of $R_{on,sp}$ decreases due to the increase in the N-type doping dose, and the BV increases because of the improvement in the vertical BV. For the $R_{on,sp}$ case, the values of the $R_{on,sp}$ of the PD SJ-LDMOS are approximately the same as those of the conventional SJ-LDMOS at $h = 2$ μm and $h = 4$ μm, owing to the similarity of their conduction paths. Moreover, under the condition of $h = 1$ μm it can be obtained from Fig. 4(b) that the lightly doped P pillar is changed into the N pillar, leading to the increase in the N-type doping dose. The $R_{on,sp}$ of the PD SJ-LDMOS is therefore smaller than that of the conventional SJ-LDMOS at $h = 1$ μm.

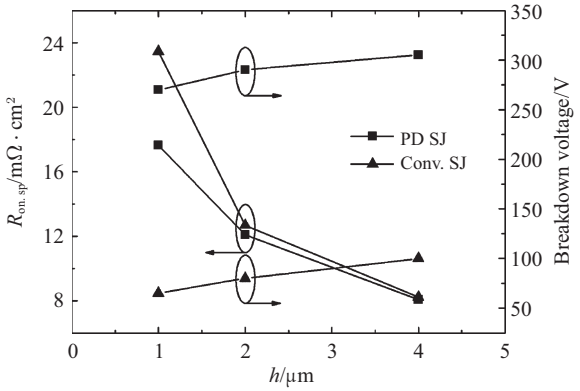


Fig. 5. Dependences of $R_{on,sp}$ and BV on height h with $\alpha = 1/2$ and $N_A = N_D = 2 \times 10^{16}$ cm^{-3}.

For the proposed structure, the fabrication of the lightly doped P pillar is the key process. A flow chart of the process is illustrated in Fig. 6. An additional ion implantation needs to be added right after the phosphorus ions have been implanted in the N pillar to form the lightly doped P pillar. The other process flow of the PD SJ-LDMOS is identical to the conventional SJ-LDMOS process.

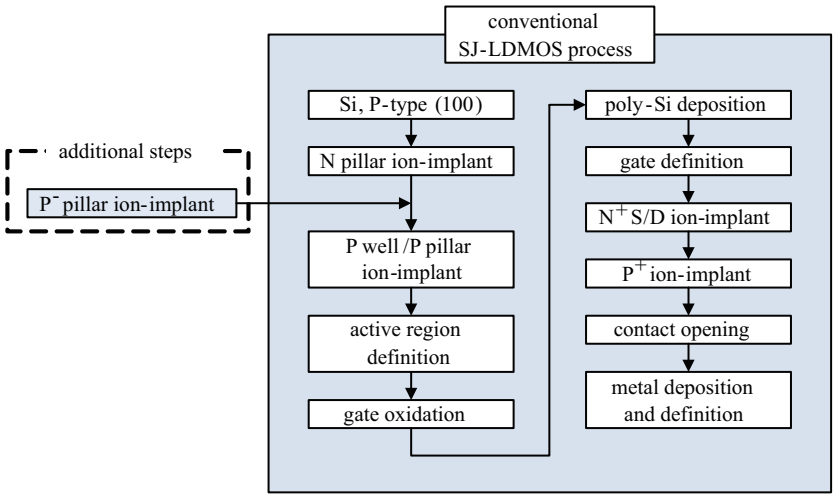


Fig. 6. (color online) Process flow for the PD SJ-LDMOS.

4. Conclusion

A new SJ-LDMOS with a partial lightly doped P pillar is proposed and investigated by simulation. This structure eliminates charge imbalance to achieve high BV while maintaining almost the same low $R_{on,sp}$ as that of the conventional SJ-LDMOS. The simulation results indicate that a uniform surface electric field profile is obtained, and the PD SJ-LDMOS exhibits a BV of 300 V with a 15 μm drift length, which increases by 300% compared with the conventional SJ-LDMOS.

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