Comparative study of the electrical properties of Au/n-Si (MS) and Au/Si_3N_4/n-Si (MIS) Schottky diodes*

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In this paper, the electrical parameters of Au/n-Si (MS) and Au/Si_3N_4/n-Si (MIS) Schottky diodes are obtained from the forward bias current–voltage (I–V) and capacitance–voltage (C–V) measurements at room temperature. Experimental results show that the rectifying ratios of the MS and MIS diodes at ± 5 V are found to be 1.25×10^3 and 1.27×10^4, respectively. The main electrical parameters of the MS and MIS diodes, such as the zero-bias barrier height (Φ_{Bo}) and ideality factor (n), are calculated to be 0.51 eV (I–V), 0.53 eV (C–V), and 4.43, and 0.65 eV (I–V), 0.70 eV (C–V), and 3.44, respectively. In addition, the energy density distribution profile of the interface states (N_{ss}) is obtained from the forward bias I–V, and the series resistance (R_s) values for the two diodes are calculated from Cheung's method and Ohm's law.

Keywords: Au/n-Si and Au/Si_3N_4/n-Si type diodes, I–V and C–V measurements, ideality factor, barrier height

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1. Introduction

The metal–semiconductor (MS) contact is one of the most widely used rectifying contacts in the electronics industry due to the technological importance of the Schottky diodes (SDs). An insulator layer between the metal and semiconductor converts an MS SD into a metal–insulator–semiconductor (MIS)-type SD.[1–6] The main electrical parameters, such as barrier height (Φ_B), ideality factor (n), series resistance (R_s), and the interface states (N_{ss}) of the MS and MIS SDs, are affected strongly by the existence of an insulator layer, since the insulator layer increases the values of Φ_B, n, and R_s, thereby leading to a decrease in the reverse leakage current and N_{ss}.[1,2,7] Furthermore, an insulator layer alleviates the electric field reduction in MIS SDs.

In addition, localized interface states at the semiconductor/insulator interface can be divided into two groups and are dependent on the thickness of the insulator layer. One of these groups communicates most readily with the metal, while the other group does with the semiconductor.[1,2,8,9] The communication of the interface states with the metal decreases with increasing insulator thickness. Also, the interface states originate from defects such as dangling bounds at the insulator/substrate interface with energy states in the Si forbidden band-gap, and are dependent on the chemical composition of the interface.[10–12]

Due to its chemical, mechanical, and electronic properties, silicon nitride (Si_3N_4) is an industrially important material. Excellent thermomechanical properties have made this material usable for engine parts, bearings, metal machining, and other industrial applications. Si_3N_4 films are also used as an essential part of metal–insulator–semiconductor inversion layer solar cells, as antireflection and passivation coatings, as well as the active layer causing energy band bending.[13–15]

In this study, an attempt is made to investigate the detailed electrical properties of Si Schottky diodes with and without an interfacial insulator layer (Si_3N_4) using forward bias I–V measurements and reverse bias C–V measurements at room temperature. In order to compare the diodes with and without Si_3N_4, their main electrical parameters are extracted from these measurements at room temperature.

2. Experimental details

The Au/n-Si (MS) and Au/Si_3N_4/n-Si (MIS) type SDs were fabricated on phosphorus-doped (n-type) single-crystal Si substrates, each with a 2″ diameter, 300 μm thickness, (100) orientation, and 0.5 Ω·cm resistivity. For the fabrication process, the n-Si substrates were chemically cleaned using a conventional method, then chemically etched and finally quenched in deionized water. Prior to each cleaning step, the Si substrate was rinsed thoroughly in deionized water at a resistivity of 18 MΩ·cm using an ultrasonic bath. After the cleaning and etching steps, the Si substrates were mounted on a stainless-steel sputtering holder that was heated optically, and loaded into a radio frequency (RF) magnetron sputtering system. The Si substrate was heated up to 400 °C in 1×10^8 mbar (1 bar = 100 kPa) high vacuum and sputter cleaned in pure argon ambient to ensure the removal of any residual organic substances. Then, the silicon nitride (Si_3N_4) film was deposited on n-Si using an RF magnetron sputtering system and high purity (99.999%) silicon nitride target.

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In addition, the film was deposited at a constant pressure of 3×10^{-3} mbar and a constant substrate temperature of 200 °C.

For the electrical characterization, the Ohmic and rectifier contacts were formed in a thermal evaporation system with a tungsten holder at a pressure of 1×10^{-7} mbar. High-purity Au (99.999% purity) with a thickness of $\sim$ 2000 Å (1 Å = 0.1 nm) was evaporated onto the whole back surface of the substrate, as a back contact, at 450 °C, and annealed at 400 °C for 7 min to form a good Ohmic contact. After that, circular dot-shaped rectifier front contacts of 2 mm diameter and $\sim$ 2000-Å thickness were formed by the deposition of Au (99.999% purity) onto Si_3N_4 film at 50 °C. In this way, Au/n-Si (MS) and Au/Si_3N_4/n-Si (MIS) SDs were fabricated for the electrical measurements. The electrode connections were made using silver paste.

The current–voltage (I–V) measurements were performed using a Keithley 2400 source-meter at room temperature. The capacitance–voltage (C–V) measurements were carried out using an HP 4192A LF impedance analyzer (5 Hz–13 MHz) at 1 MHz, and a small AC test signal 50 mV_{rms} from the external pulse generator was applied to the sample in order to meet the requirements.

3. Results and discussion

3.1. Current–voltage (I–V) characteristics

According to the thermionic emission (TE) theory, when MS- or MIS-type SD has a series resistance (R_s) and the value of ideality factor is greater than unity, the relation between the applied forward voltage ($V > 3kT/q$) and the current can be expressed as[16,17]

$$I = AA*T^2\exp\left(-\frac{q\Phi_{Bo}}{kT}\right)\left[\exp\left(\frac{q(V-IR_s)}{nkT}\right)-1\right], \quad (1)$$

where V is the applied bias voltage, q the electronic charge, n the ideality factor, k the Boltzmann constant, T the absolute temperature in Kelvin, and the term IR_s the voltage drop across the R_s of the diode. The reverse saturation current (I_o) can be extracted from the straight-line intercept of the ln(I)–V plot at zero bias and given by

$$I_o = AA^*T^2\exp\left(-\frac{q\Phi_{Bo}}{kT}\right), \quad (2)$$

where A is the rectifier contact area, A^* the effective Richardson constant (= 112 Å/cm^2·K^2 for n-type Si),[2] and Φ_{Bo} the zero-bias barrier height. Once I_o is determined, Φ_{Bo} is obtained by rewriting Eq. (2) as

$$\Phi_{Bo} = \frac{kT}{q}\ln\left[\frac{AA^*T^2}{I_o}\right]. \quad (3)$$

The ideality factor, n, is introduced to take the deviation of the experimental I–V data from the ideal TE into account, and can be calculated from the slope of the linear region of the forward bias ln(I)–V plot, and then can be written as

$$n = \frac{q}{kT}\left(\frac{dV}{d(\ln I)}\right), \quad (4)$$

where $dV/d\ln(I)$ is the slope of the linear region of the ln(I) versus V plots.

Figure 1 shows the forward and reverse biased curves of the Au/n-Si (MS) and Au/Si_3N_4/n-Si (MIS) Schottky diodes at room temperature. As can be seen in Fig. 1, the MS and MIS diodes each show a good rectifying behavior, and in particular the MIS diode has a higher rectifying ratio with a low leakage current compared with the MS diode. The rectifying ratio is found to be 1.25×10^3 for the MS diode, while it is 1.27×10^4 for the MIS diode at ±5 V. The insulator layer in the MIS diode not only prevents leakage current, but also raises the rectifying ratio. This situation is attributed to the image force lowering of the Schottky barrier height.[1,2,16–18] In addition, the ln(I)–V plots of the MS and MIS SDs deviate considerably from linearity at high forward bias voltages due to the effects of some factors such as series resistance, interface states, etc.

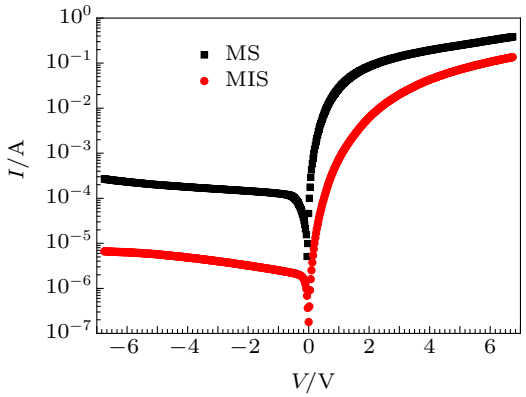


Fig. 1. (color online) Semi-logarithmic forward and reverse bias ln(I)–V plots at room temperature for the MS and MIS Schottky diodes.

The experimental values of I_o and n of the MS and MIS SDs are calculated from Eqs. (3) and (4), respectively. The values of I_o and n of the MS and MIS SDs are found to be 1.92×10^{-4} A and 4.43 and 9.15×10^{-7} A and 3.44, respectively. The ideality factor values of these two diodes are considerably larger than unity. The high value of n is attributed to the particular distribution of the interface states, the insulator layer grown on the semiconductor, the image force effect, recombination–generation, the wide distribution of low Schottky barrier height patches at the Au/n-Si interface, and tunneling which might be the other possible mechanism that causes the ideality factor value to be greater than unity.[1,2,8–10,18–21] The experimental value of the barrier height (Φ_{Bo}) for the MS and MIS SDs are found to be 0.51 eV and 0.65 eV, respectively. The increase in barrier height of the MIS SD could be explained by an increase in negative charges at the interface.

These negative charges probably come into being due to the electron traps localized at the semiconductor interface.[19–23]

In order to understand the conduction mechanism in detail or to understand the deviation of the $\ln(I)$–V plot from the linearity in a forward bias region, double logarithmic $\ln(I)$–$\ln(V)$ plots for the two diodes are shown in Fig. 2.

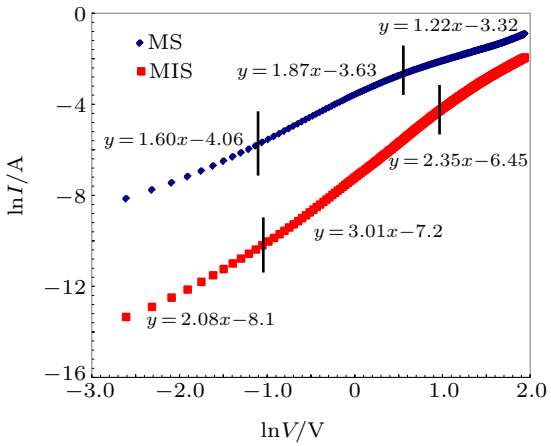


Fig. 2. (color online) The $\ln(I)$ versus $\ln(V)$ plots of the MS and MIS Schottky diodes at room temperature.

As can be seen in Fig. 2, $\ln(I)$–$\ln(V)$ plots have three distinct linear regions, each with its own slope (region 1: $-2.6\ \text{V} < V < -1.2\ \text{V}$; region 2: $-1.3 < V < 0.57$ V, and region 3: $0.59 < V < 1.94$ V), that obey the $I \propto V^m$ relation. Here, m represents the slope of each region's linear part, and the values of m are found to be 1.60, 1.87, and 1.22 for the MS diode. On the other hand, the $\ln(I)$–$\ln(V)$ plot for the MIS diode has three distinct linear regions (region 1: $-2.6\ \text{V} < V < -1.05$ V; region 2: $-0.98\ \text{V} < V < 0.99$ V, and region 3: $1.00\ \text{V} < V < 1.94$ V) and their slopes are found to be 2.08, 3.01, and 2.35, respectively. It is clear that the current conductions in the low bias region (region 1) for two diodes each show an Ohmic behavior, that is, the current is directly proportional to the applied bias voltage.[24–27] This behavior can be attributed to the superiority of the bulk generated current in the film to the injected free carrier generated current. In the second region, for two diodes, the I–V relation can be characterized by a power law. In this region, the slopes of the $\ln(I)$–$\ln(V)$ plots are larger than the two, and such a behavior can be explained as the trap-charge limited current (TCLC) mechanism with an exponent trap distribution.[24,27] In this case, the increase in the number of injected electrons causes the filling up of the traps and the rising up of the space charges.[26] In the high bias region (region 3), because of the strong electron injection, the electrons escape from the traps and contribute to the space-charge-limited current (SCLC).[25–28] In this region, the current through the diode appears to become limited by another process, and the current values reveal that this limitation is not due to either the R_s of the bulk Si or the Ohmic contact.

The forward bias $\ln(I)$–V curves deviate considerably from linearity due to the effect of R_s. The R_s value is calculated using a method developed by Cheung and Cheung.[29] Cheung's functions are expressed as

$$\frac{dV}{d(\ln I)} = IR_s + n\left(\frac{kT}{q}\right) \tag{5}$$

and

$$H(I) = V - n\left(\frac{kT}{q}\right)\ln\left(\frac{I}{AA^*T^2}\right) = n\Phi_{Bo} + IR_s. \tag{6}$$

These two equations should give a straight line for the data of the downward curvature region in the forward bias I–V characteristic. In Figs. 3(a) and 3(b), experimental $dV/d\ln(I)$ versus I and $H(I)$ versus I plots are presented at room temperature for the MS and MIS SDs, respectively. The values of R_s are obtained from the slopes of the $dV/d\ln(I)$ versus I plot and $H(I)$ versus I plot. The calculated values of R_s for the MS and MIS diodes from Figs. 3(a) and 3(b) are 18.82 Ω and 21.49 Ω, and 15.76 Ω and 32.56 Ω, respectively. As a result, the values of R_s obtained from these slopes are in good agreement with each other.[30–33]

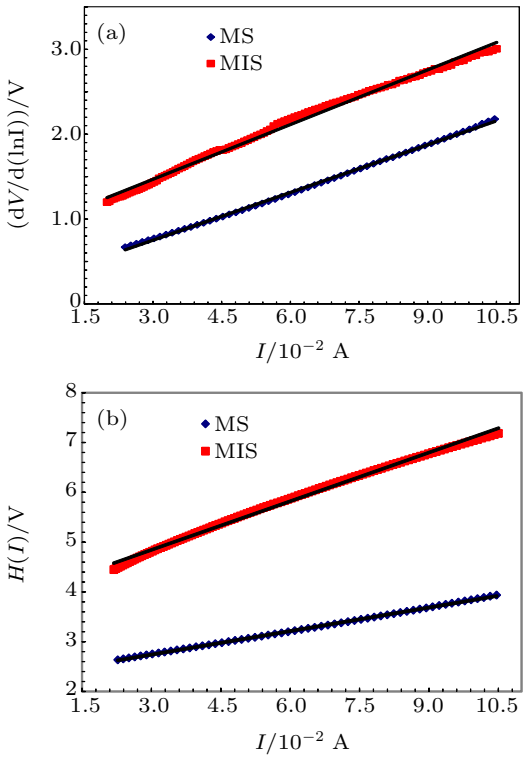


Fig. 3. (color online) The (a) $dV/d\ln(I)$ versus I and (b) $H(I)$ versus I characteristics of the MS and MIS Schottky diodes obtained from the forward bias I–V data at room temperature.

Furthermore, it is well known that both the series resistance (R_s) and shunt resistance (R_{sh}) of the diode are important parameters that affect the diode performance or quality. The R_s and R_{sh} values of the MS and MIS SDs are obtained from the structure resistance (R_i) versus applied bias voltage (V_i) plot determined from both the reverse and forward bias I–V

characteristics by using Ohm's law as the following relation

$$R_{\rm i} = \frac{{\rm d}V_{\rm i}}{{\rm d}I_{\rm i}}. \tag{7}$$

Therefore, the voltage-dependent resistance profiles of the MS and MIS SDs are obtained from the I–V data using Ohm's law (Eq. (7)) and given in Fig. 4. As can be seen in Fig. 4, in the sufficiently high forward bias region ($V \geq 6.5$ V), the values of resistance correspond to the $R_{\rm s}$ values of these diodes. On the other hand, the values of resistance in the negative bias region ($V \leq -6.5$ V) correspond to the $R_{\rm sh}$ values of these diodes. The values of $R_{\rm s}$ and $R_{\rm sh}$ for the MS and MIS diodes are found to be $\sim 18\ \Omega$ and 26 kΩ, and $\sim$42 Ω and 1 MΩ, respectively.

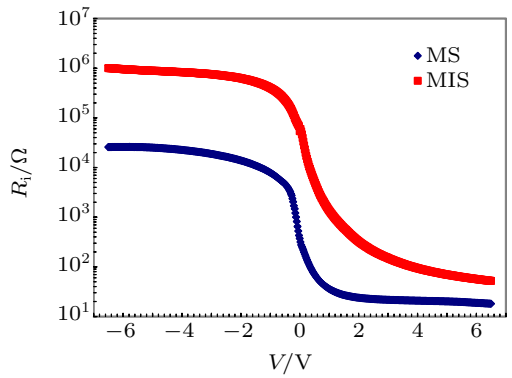


Fig. 4. (color online) Plots of structure resistance versus voltage for the MS and MIS Schottky diodes at room temperature.

The energy density distribution profiles of the interface states ($N_{\rm ss}$) for both the MS diode and the MIS diode can be determined from the forward bias I–V data considering their corresponding values of voltage-dependent ideality factor $n(V)$, effective barrier height ($\Phi_{\rm e}$), and $R_{\rm s}$. The quantity of $\Phi_{\rm e}$ can be described as a function of V.[1,8] Thus the derivative of the effective barrier height with respect to V can be written as

$$\frac{{\rm d}\Phi_{\rm e}}{{\rm d}V} = \beta = 1 - \frac{1}{n(V)}, \tag{8}$$

where β is the voltage coefficient of the effective barrier height $\Phi_{\rm e}$ and is given by[8,21,34]

$$\Phi_{\rm e} = \Phi_{\rm Bo} + \beta(V - IR_{\rm s}) = \Phi_{\rm Bo} + \left(1 - \frac{1}{n(V)}\right)(V - IR_{\rm s}). \tag{9}$$

For SDs with interface states in equilibrium with the semiconductor, the ideality factor becomes greater than unity and is given by[8]

$$n(V) = 1 + \frac{\delta}{\varepsilon_{\rm i}}\left[\frac{\varepsilon_{\rm s}}{W_{\rm D}} + qN_{\rm ss}(V)\right], \tag{10}$$

where $W_{\rm D}$ is the space charge region width, δ the thickness of the interfacial insulator layer, and $\varepsilon_{\rm i}$ ($= 7.5\varepsilon_{\rm o}$) and $\varepsilon_{\rm s}$ ($= 11.9\varepsilon_{\rm o}$) the permittivity values of the insulator layer and the semiconductor, respectively. The values of $W_{\rm D}$ for the MS and MIS diodes are calculated from the reverse bias C^{-2} versus V plot at 1 MHz. The native interfacial insulator layer (SiO_2) (for MS) and interfacial insulator layer (Si_3N_4) thickness (δ) are found to be about 20 Å and 55 Å, respectively, from the insulator layer capacitance ($C_{\rm ox} = \varepsilon_{\rm i}\varepsilon_{\rm o}A/\delta$). This expression of voltage-dependent ideality factor is identical to Eq. (18) given by Card and Rhoderick.[8] The expression for the interface state density ($N_{\rm ss}$) deduced in Refs. [8] and [35] is reduced to[1,2]

$$N_{\rm ss}(V) = \frac{1}{q}\left[\frac{\varepsilon_{\rm i}}{\delta}(n(V) - 1) - \frac{\varepsilon_{\rm s}}{W_{\rm D}}\right]. \tag{11}$$

Furthermore, in an n-type semiconductor, the energy of the interface state $E_{\rm ss}$ with respect to the bottom of the conduction band, $E_{\rm c}$, at the surface of the semiconductor, is given by[8,13,18,34]

$$E_{\rm c} - E_{\rm ss} = q(\Phi_{\rm e} - V). \tag{12}$$

Figure 5 shows the energy distribution profiles of the $N_{\rm ss}$ with and without taking into account the values of $R_{\rm s}$ obtained from the forward bias I–V characteristics of the MS and MIS diodes at room temperature. As seen in Fig. 5, the magnitudes of the $N_{\rm ss}$ without and with the $R_{\rm s}$ at the $E_{\rm c}$ value of 0.35 (eV) are 1.5×10^{14} eV^{-1}·cm^{-2} and 4.30×10^{13} eV^{-1}·cm^{-2} for the MS diode, respectively. On the other hand, the magnitudes of $N_{\rm ss}$ without and with the $R_{\rm s}$ at $E_{\rm c}$ value of 0.35 (eV) are 1×10^{14} eV^{-1}·cm^{-2} and 3.30×10^{13} eV^{-1}·cm^{-2} for the MIS diode, respectively. It is clear that the values of $N_{\rm ss}$ obtained by taking the $R_{\rm s}$ values into account are lower than those obtained without considering the $R_{\rm s}$.[36,37]

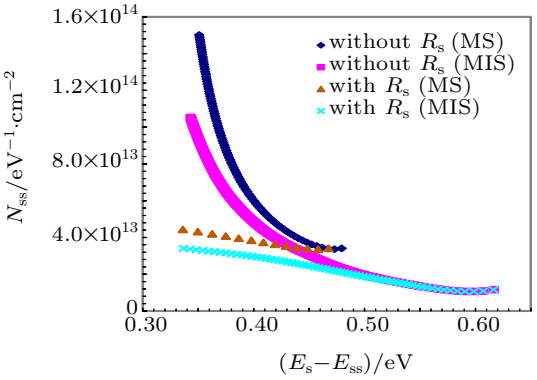


Fig. 5. (color online) Interface state density distribution profiles, each as a function of $E_{\rm c} - E_{\rm ss}$, for the MS and MIS Schottky diodes.

3.2. Capacitance–voltage (C–V) characteristics

The C–V characteristics are analyzed from the reverse bias C^{-2}–V characteristics. To extract the other important electrical parameters of the MS and MIS diodes, such as the intercept voltage $V_{\rm o}$, diffusion potential $V_{\rm D}$, Fermi energy $E_{\rm F}$, donor concentration $N_{\rm D}$, and the width of the space charge region $W_{\rm D}$, the capacitance–voltage (C–V) measurements are performed at 1 MHz frequency. The C^{-2}–V characteristics of the MS and MIS diodes are given in Fig. 6. As can be seen from Fig. 6, each of the C^{-2}–V plots for the two diodes gives a straight line in a wide range of applied bias voltage.

The depletion layer capacitance is given in the following equations[1,2,38–40]

$$C^{-2} = \frac{2(V_o + V)}{\varepsilon_s \varepsilon_o q A^2 N_D}, \tag{13}$$

$$\frac{d(C^{-2})}{dV} = \frac{2}{\varepsilon_s \varepsilon_o q A^2 N_D}. \tag{14}$$

Here, V is the reverse bias voltage, and N_D the equivalent to the free electron concentration when all shallow donor levels are ionized. V_o is the intercept voltage at zero bias, and can be obtained by means of extrapolation of the C^{-2}–V plot to the voltage axis as 0.28 V and 0.44 V for the MS and MIS diodes, respectively. In addition, the values of the doping concentration (N_D) for the MS and MIS diodes are calculated to be 2.72×10^{15} cm^{-3} and 2.19×10^{15} cm^{-3}, respectively. The apparent decrease in the doping concentration for the MIS diode invokes interface states in equilibrium with the semiconductor. Another possible explanation is that it could be due to traps associated with the insulator layer.[8,19]

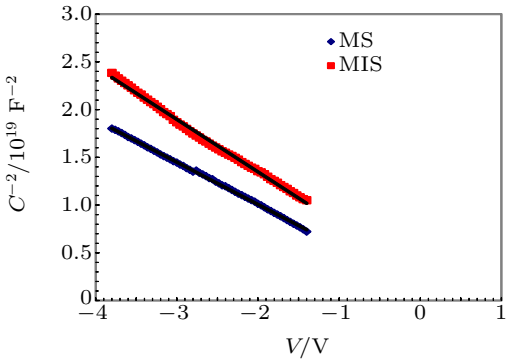


Fig. 6. (color online) The C^{-2}–V plots at 1 MHz frequency and room temperature for the MS and MIS Schottky diodes.

Using the obtained V_o values, the diffusion potential (V_D) at zero bias can be calculated using the following relation:

$$V_D = V_o + \frac{kT}{q}. \tag{15}$$

The values of diffusion potential (V_D) are found to be 0.30 V and 0.47 V for the MS and MIS diodes, respectively. The value of the barrier height (Φ_B) can be calculated using the C–V measurements through the following well-known equation:

$$\begin{aligned}\Phi_B(C\text{–}V) &= V_D + E_F - \Delta\Phi_B \\ &= V_D + \left(\frac{k_B T}{q}\right)\ln\left(\frac{N_C}{N_D}\right) - \Delta\Phi_B,\end{aligned} \tag{16}$$

where E_F is the energy difference between the bulk Fermi level and conductance band edge, and the values of E_F are calculated to be 0.24 eV and 0.25 eV for MS and MIS diodes, respectively. N_C is the effective density of states in the conduction band, and is $N_c = 2.8 \times 10^{19}$ cm^{-3} for n-Si at room temperature,[1,2,38,41,42] and $\Delta\Phi_B$ is the image force barrier lowering and given by[1,2]

$$\Delta\Phi_B = \left[\frac{qE_m}{4\pi\varepsilon_s\varepsilon_o}\right]^{1/2}, \tag{17}$$

where E_m is the maximum electric field and given by

$$E_m = \left[\frac{2qN_D V_o}{\varepsilon_s \varepsilon_o}\right]^{1/2}. \tag{18}$$

The values of E_m and $\Delta\Phi_B$ for the MS and MIS diodes are found to be 15787.75 V/cm and 0.014 eV, and 17665.53 V/cm and 0.015 eV, respectively. As a result, the values of the barrier height (Φ_B) are calculated to be 0.53 eV and 0.70 eV for the MS and MIS diodes, respectively. These obtained values are in good agreement with the barrier height values obtained from the I–V characteristics.

In addition, the values of the depletion layer width (W_D) for the two diodes are also calculated from C^{-2}–V plots at 1 MHz using the following equation:[1,2]

$$W_D = \sqrt{\frac{2\varepsilon_s \varepsilon_o V_D}{qN_D}}, \tag{19}$$

and they are 3.82×10^{-5} cm and 5.30×10^{-5} cm for the MS and MIS diodes, respectively.

4. Conclusions

To compare the electrical properties of Au/n-Si (MS) and Au/Si_3N_4/n-Si (MIS) Schottky diodes, current–voltage (I–V) and capacitance–voltage (C–V) measurements are used. Experimental results show that MS and MIS diodes each show a good rectifying behavior, and the MIS diode in particular has a higher rectifying ratio with lower leakage current than the MS diode. Calculations show that the zero-bias barrier height (Φ_{Bo}) and ideality factor (n) values of the MS diode are 0.51 eV (I–V), 0.53 eV (C–V), and 4.43, respectively. It is observed that the Φ_{Bo} values increase to 0.65 eV (I–V) and 0.70 eV (C–V), and the value of n deceases to 3.44 for the MIS diode. The decrease in the value of n in the MIS diode as compared with that of the MS is attributed to the presence of an insulator layer at the Au/n-Si interface. Also, the barrier height values obtained from the I–V characteristics are in good agreement with those obtained from the C–V characteristics. The values of the interface state (N_{ss}) obtained by taking the R_s values into account are lower than those obtained without considering R_s. In addition, the R_s values obtained from the $dV/d\ln(I)$–I and $H(I)$–I plots for the two diodes are in good agreement with each other.

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