The charge storage characteristics of ZrO_2 nanocrystallite-based charge trap nonvolatile memory*

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ZrO_2 nanocrystallite-based charge trap flash memory capacitors incorporating a $(ZrO_2)_{0.6}(SiO_2)_{0.4}$ pseudobinary high-k oxide film as the charge trapping layer were prepared and investigated. The precipitation reaction in the charge trapping layer, forming ZrO_2 nanocrystallites during rapid thermal annealing, was investigated by transmission electron microscopy and X-ray diffraction. It was observed that a ZrO_2 nanocrystallite-based memory capacitor after post-annealing at 850 °C for 60 s exhibits a maximum memory window of about 6.8 V, good endurance and a low charge loss of ∼25% over a period of 10 years (determined by extrapolating the charge loss curve measured experimentally), even at 85 °C. Such 850 °C-annealed memory capacitors appear to be candidates for future nonvolatile flash memory device applications.

Keywords: charge storage, ZrO_2 nanocrystallites, atomic layer deposition, pulse laser deposition

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1. Introduction

With the development of semiconductor technology, the feature size of conventional floating gate-type nonvolatile semiconductor memory (FG-NVSM) is approaching its scaling limitation, so tremendous efforts have been made to explore novel solid-state nonvolatile memory devices with the desired characteristics, such as low cost, high density, and a fast program/erase (P/E) speed for use in mobile electronics.[1–3] Based on the concept that charges are stored in discrete traps within the charge trapping layer, silicon–oxide–nitride–oxide–silicon (SONOS) charge trap flash (CTF) memories with nitride (Si_3N_4)[4] as the charge trapping layer have attracted much attention, with the hope of replacing the conventional FG-NVSM in commercial applications. One problem in SONOS memory devices is the small conduction band offset at the Si_3N_4/tunneling layer interface,[5] which leads to poor retention. To overcome the problem, employing high-k dielectrics in SONOS structures has been reported by many researchers.[6–8] However, conventional CTF memory devices have fundamental problems with the trade-off between operating speed and retention time.[9] Among the family of nonvolatile memories, nanocrystallite (NC)-based CTF memory devices have been given much attention in the electronics industry due to their advantages such as lower operating voltage, better endurance, discrete traps, and a simple fabrication process compatible with standard complementary metal–oxide–semiconductor (CMOS) technology.[10] But so far, much of the work has focused on developing charge trapping layers containing metallic or semiconducting NCs for use in NVM devices,[11–16] while oxide NCs are rarely reported. In addition, Wu *et al.*[17] reported that the cubic ZrO_2 can effectively store charges. Based on the above considerations, ZrO_2 NC-based CTF memory using $(ZrO_2)_{0.6}(SiO_2)_{0.4}$(ZSO) pseudobinary high-$k$ oxide film as the charge trapping layer between an SiO_2 tunneling layer and an Al_2O_3 blocking layer will be reported in this paper. As a high-k dielectric, ZSO allows a higher electric field across the tunneling layer due to electric flux density continuity[8] and the results in modified Fowler–Nordheim tunneling due to the smaller conduction band offset (CBO) with an Si substrate.[18] ZrO_2 NC as the storage medium was precipitated from an amorphous ZSO film matrix by means of rapid thermal annealing (RTA) treatment. The effect of annealing temperature on the memory characteristics is then discussed.

2. Experiment

ZrO_2 NC-based charge trap flash memory capacitors with a Pt/Al_2O_3/ZSO/SiO_2/p-Si stack structure were fabricated. Prior to film deposition, the substrates, p-type Si (100) wafers with a resistivity of 3 Ω·cm–20 Ω·cm, were cleaned by the standard Radio Corporation of America (RCA) process to remove native oxide. Then, 4 nm SiO_2 was thermally grown in dry O_2 at 900 °C as the tunneling layer. A ZSO charge trapping layer with a thickness of ∼6 nm was deposited by pulsed laser deposition (PLD) at a substrate temperature of 350 °C.

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(A KrF excimer laser operating at 1 Hz–5 Hz was used for ablation. The laser fluence was around 1.8 J/cm^{-2}. The deposition was performed under oxygen pressure of 1×10^{-4} Pa, and the growth rate per laser shot was approximately 0.1 nm.) The ceramic targets were obtained by sintering stoichiometric mixtures of ZrO_2 and SiO_2 at 1400 °C for 8 hours. Subsequently, a $\sim$ 8-nm Al_2O_3 film was deposited by atomic layer deposition (ALD) using trimethylaluminum ($Al(CH_3)_3$) precursors at a substrate temperature of 300 °C. During this process, O_3 was used as the oxygen source. The fabricated memory capacitor without post-annealing is denoted as ZS0. After these processes, the above heterostructures underwent RTA at 800 °C, 850 °C, and 900 °C for 60 s in N_2 atmosphere to precipitate ZrO_2 NC as the charge storage media, denoted ZS1, ZS2, and ZS3, respectively. Finally, platinum (Pt) gate electrodes with an area of 7.85×10^{-5}cm^2 were deposited on the films using the magnetron sputtering technique at room temperature. Silver paste was spread on the back side of the Si substrates as the bottom electrodes. The crystallization behaviors of the ZSO films were examined by X-ray diffraction (XRD) and X-ray photoelectron spectroscopy (XPS), and the cross section and interface quality of the memory capacitors were revealed by high-resolution transmission electron microscope (HRTEM) images. HRTEM samples were prepared using conventional methods (grinding, polishing, and thinning). To prepare the cross sectional sample of the memory structure for HRTEM, a standard technique was used, which included gluing the sample onto a supporting structure, cutting, grinding, polishing, and thinning via room-temperature argon milling procedures. The electrical characteristics of the memory capacitors were measured using a Keithley 4200 semiconductor characterization system (4200 SCS) in DC sweeping mode and pulse mode.

3. Results and discussion

Since the ZrO_2 NC is a key factor for the charge storage characteristics of the ZrO_2 NC-based CTF memory, it is important to know the size of the ZrO_2 NCs after RTA treatment. The ZSO films were grown by PLD, and then underwent RTA in N_2 atmosphere at different temperatures (800 °C, 850 °C, and 900 °C). Previously, we confirmed that the as-deposited ZSO films were amorphous, whereas some crystalline XRD diffraction peaks appeared after RTA in N_2 atmosphere at different temperatures, and these diffraction peaks corresponded to the (111), (200), (220), and (311) planes of the cubic ZrO_2 phase, respectively, as shown in Fig. 1. The results show that the crystalline ZrO_2 phase precipitated from the amorphous ZSO matrix after RTA treatment. The selected area electron diffraction (SAED) pattern of both the as-deposited and 850 °C-annealed ZSO films are shown in the inset of Fig. 1. The as-deposited film is amorphous according to the SAED pattern observed. The diffraction spots marked as A, B, C, and D correspond to the (111), (200), (220), and (311) planes of the cubic ZrO_2 phase for the 850 °C-annealed ZSO film, respectively. This demonstrates that there is no crystalline phase except for the cubic ZrO_2. Furthermore, the diffusive rings indicate the existence of an amorphous matrix after the formation of ZrO_2 NC for the 850 °C-annealed ZSO film. We also observed that in the O 1s spectra, two peaks with binding energies of 530.1 eV[19] (corresponding to ZrO_2) and 532.1 eV (corresponding to the Si-rich amorphous ZSO matrix), respectively, appear for the 850 °C-annealed ZSO film, as shown in the inset of Fig. 1. This indicates that the amorphous matrix in the annealed ZSO films is more Si-rich than the as-deposited ZSO, and that the ZrO_2 NCs are embedded in the Si-rich amorphous ZSO matrix.

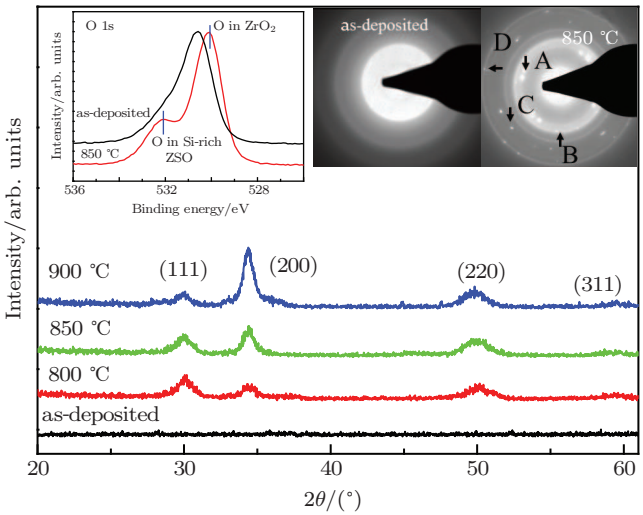


Fig. 1. (color online) XRD patterns of as-deposited and RTA-treated ZSO films. The insets are the O 1s XPS spectra of 850 °C-annealed ZSO film (left), the selected area electron diffraction pattern of the as-deposited film (middle), and the 850 °C-annealed ZSO film (right).

The cross-sectional HRTEM images of the memory structure before and after RTA treatment are shown in Fig. 2. The interfaces of the Si substrate/TL, TL/CTL, and CTL/BL are clear and there is no formation of ZrO_2 NC for ZSO (i.e., Fig. 2(a)). It is observed from Figs. 2(b)–2(d) that ZrO_2 NCs are precipitated from the ZSO films due to the phase separation after the annealing treatment. The NC sizes were about 3 nm, 5 nm, and 20 nm for ZS1, ZS2, and ZS3, respectively, as marked by the dotted cycles. Compared with ZS1 and ZS2, the larger NC size should be attributed to the coarsening of precipitated ZrO_2 NC after 900 °C-annealing treatment for ZS3. The experimental results can be explained by the diffusive phase transformation theory, according to which the precipitation reaction starts from the nucleation of the precipitated phase, followed by the growth of the nuclei, and then, together with a decrease in the supersaturation in the matrix, coarsening of the precipitated particles occurs, leading to dissolution of the smaller particles and growth of larger particles.

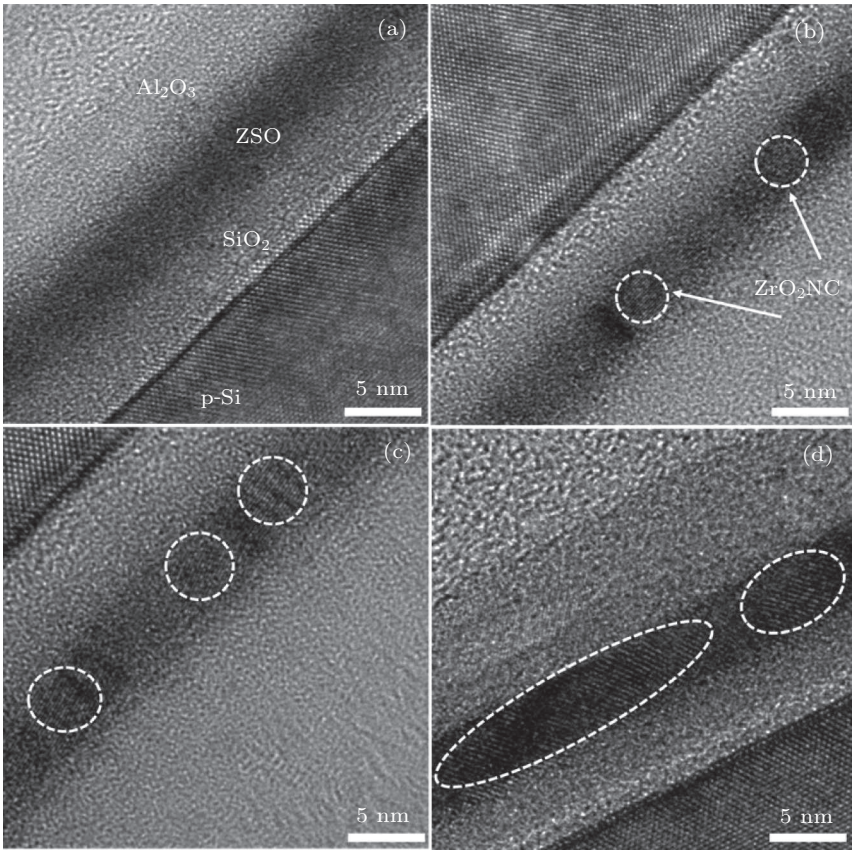


Fig. 2. Cross-sectional HRTEM images of the ZrO_2 NC-based memory capacitors, (a) ZS0; (b) ZS1; (c) ZS2; (d) ZS3.

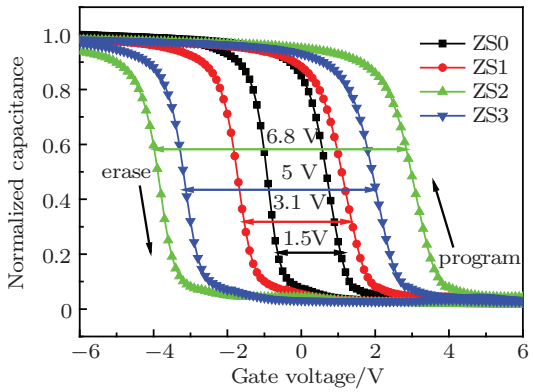


Fig. 3. (color online) The high-frequency (1 MHz) capacitance versus gate voltage (C–V) curves of the ZrO_2 NC-based memory capacitors.

Figure 3 demonstrates the counterclockwise high-frequency (1MHz) C–V hysteresis memory windows of the memory capacitors, measured with identical sweeping gate voltage (V_G). The memory window is defined as the difference in the flatband voltages (V_{FB}) between the write and erase states, which is measured by low V_G from +6 V to −6 V and then sweeps back to +6 V. For the four samples, the hysteresis memory windows were measured to be 1.5 V, 3.1 V, 6.8 V, and 5 V, respectively. Note that the memory window is larger in the ZS2 sample than that in the other samples. For ZS2, the amount of stored charges can be estimated by

$$N_t = \frac{C_{OX} V_{FB}}{qA}, \tag{1}$$

where C_{OX} represents the capacitance of the capacitor at the accumulation region, A represents the effective area of the Pt electrode and q is the elementary charge. Thus, the density of charges stored in ZrO_2 NC is estimated to be about $2.5 \times 10^{13}/\text{cm}^2$. Compared to some metal NCs,[20] the ZrO_2 NCs as a storage medium can trap more electrons at low gate voltage.

Figure 4(a) illustrates the room-temperature data retention characteristics of the memory capacitors. The charge loss is defined as[21]

$$\text{Charge loss } (\%) = \left(\frac{V_P - V_t}{V_P - V_0}\right) \times 100\%, \tag{2}$$

where V_0 is the flatband voltage of the fresh sample, V_P is the flatband voltage being written at 6 V for 1 ms, t is the retention time, and V_t represents the measured flatband voltage after t. The charge loss was 8%, 6%, 4%, and 10%, up to 4×10^4 s, for the four samples, respectively. An extrapolation of the experimental results shows that the charge loss after 10 years would be 26%, 20%, 15%, and 33% for the four samples, respectively. For the four samples, it is noted that the charge loss

after 10 years at 85 °C can be determined to be 43%, 36%, 25%, and 50%, respectively, by extrapolating the charge loss curves (open symbols) that were measured experimentally, as shown in Fig. 4(b). The small ZrO_2 NCs cannot store electrons effectively due to the Coulomb blockade effect[13] of ZS1. As the size of ZrO_2 NCs increases, a well-crystallized structure is achieved (e.g., ZS2), so the electrons trapped in these larger ZrO_2 NCs could be stored for a long time. We ascribe the result to the combined effects of the tight embrace of ZrO_2 NCs by the Si-rich matrix and the sufficiently deep trap energy level.[16,22] Thermal excitation (TE) is the important charge loss mechanism for memory devices at elevated temperature — trapped electrons become thermally excited to the charge trapping layer conduction band and then tunnel back to the Si substrate.[23] Since more deep level traps for charge storage exist in the ZS2, so the retention characteristics are significantly improved. However, for the ZS3 sample, the contact area between ZrO_2 NC and the tunneling layer becomes so large that a single defect in the TL could discharge all of the electrons. This is very similar to the case of the conventional floating gate flash memory, in which the charges are stored in conducting polysilicon floating gates, and a single defect in the TL can discharge the whole memory.[24]

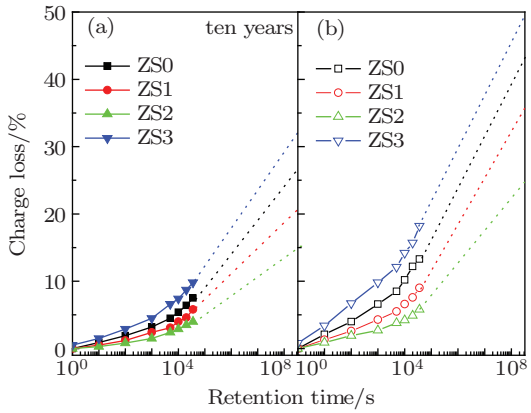


Fig. 4. (color online) Retention characteristics at room temperature (a) and 85 °C (b) of the ZrO_2 NC-based memory capacitors.

Figure 5 shows the endurance characteristics of four memory capacitors. The program (solid symbols)/erase (open symbols) conditions were +6 V for 1 ms and −6 V for 1 ms, respectively. For the four memory capacitors, the memory window is degraded by 11%, 10%, 5%, and 15% after 10^5 W/E cycles, respectively. Program/erase operations can cause a fairly uniform wear-out of cell performance,[25] which eventually limits memory endurance and gives rise to a decrease in the memory window. This should be attributed to oxide traps and interface state generation at different locations depending on bias conditions due to the device being stressed for a long time. In our results, the slight decrease in the memory window for ZS2 proves that the 850 °C-RTA-treated memory capacitor has good endurance characteristics and will be a candidate for application in future nonvolatile flash memory devices.

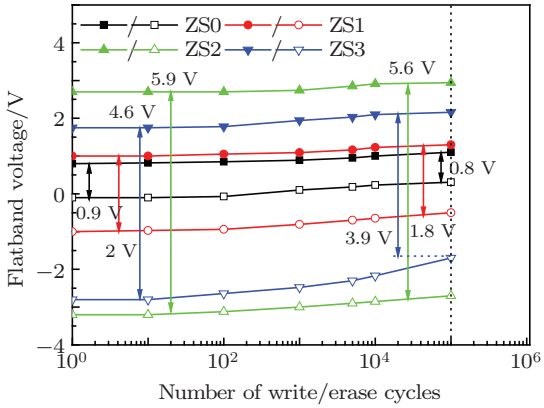


Fig. 5. (color online) The endurance characteristics of the four memory capacitors.

4. Conclusions

In summary, ZrO_2 NC-based charge trap memory capacitors incorporating a $(ZrO_2)_{0.6}(SiO_2)_{0.4}$ film as the charge trapping layer were prepared and investigated. The precipitation reaction in ZSO films, forming ZrO_2 NC as the storage medium, during RTA was investigated by TEM. It was found that the ZrO_2 NC-based memory capacitor, after annealing at 850 °C, exhibits improved electrical characteristics with a 6.8 V memory window, good endurance, and a low charge loss of ∼25% after 10 years, even at 85 °C.

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