A low on-resistance buried current path SOI p-channel LDMOS compatible with n-channel LDMOS*

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(Received 9 August 2012; revised manuscript received 5 January 2013)

A novel low specific on-resistance ($R_{on,sp}$) silicon-on-insulator (SOI) p-channel lateral double-diffused metal–oxide semiconductor (pLDMOS) compatible with high voltage (HV) n-channel LDMOS (nLDMOS) is proposed. The pLDMOS is built in the N-type SOI layer with a buried P-type layer acting as a current conduction path in the on-state (BP SOI pLDMOS). Its superior compatibility with the HV nLDMOS and low voltage (LV) complementary metal–oxide semiconductor (CMOS) circuitry which are formed on the N-SOI layer can be obtained. In the off-state the P-buried layer built in the N-SOI layer causes multiple depletion and electric field reshaping, leading to an enhanced (reduced) surface field (RESURF) effect. The proposed BP SOI pLDMOS achieves not only an improved breakdown voltage (BV) but also a significantly reduced $R_{on,sp}$. The BV of the BP SOI pLDMOS increases to 319 V from 215 V of the conventional SOI pLDMOS at the same half cell pitch of 25 μm, and $R_{on,sp}$ decreases from 157 mΩ·cm^2 to 55 mΩ·cm^2. Compared with the PW SOI pLDMOS, the BP SOI pLDMOS also reduces the $R_{on,sp}$ by 34% with almost the same BV.

Keywords: silicon-on-insulator, p-channel LDMOS, p-buried layer, breakdown voltage

PACS: 73.40.Ty, 73.90.+f, 73.61.Ng **DOI:** 10.1088/1674-1056/22/6/067306

1. Introduction

The lateral double-diffused metal–oxide semiconductor (LDMOS) transistor is widely used in power integrated circuits (ICs) due to its superior integration.[1,2] Silicon-on-insulator (SOI) technology offers superior isolation and strong immunity to latch-up.[3–8] The hole mobility in the p-channel LDMOS (pLDMOS) is much lower than electron mobility in the n-channel LDMOS (nLDMOS), leading to higher specific on-resistance ($R_{on,sp}$) of the pLDMOS. Therefore the pLDMOS has received little attention. However, the pLDMOS is desirable for high-side applications since it has the advantage of circuit simplification.[9–11] Unfortunately, conventional SOI pLDMOS (Con. SOI pLDMOS) at high-side operation suffers from handler wafer biasing, leading to a reduced BV, compared with the nLDMOS at low-side operation.[12–14]

In the present paper, a novel low resistance SOI pLDMOS device is proposed. The pLDMOS is characterized by a P-buried layer (PBL) implanted in the N-type SOI layer (BP SOI pLDMOS). This PBL acts as the low resistance current path during the on-state. In the off-state, the PBL causes multiple depletion with the N-type SOI layer, thus enhancing the RESURF effect, which not only improves the breakdown voltage (BV) but also reduces the $R_{on,sp}$. In addition, the proposed BP SOI pLDMOS exhibits excellent compatibility, which can be easily integrated with the high voltage (HV) nLDMOS. Thus, high performance high voltage complementary metal–oxide semiconductor (CMOS) devices can be built conveniently.

2. Device structure and mechanism

Figure 1(a) shows the schematic cross section of the BP SOI pLDMOS (in the dashed rectangle) integrated with the HV nLDMOS and low voltage (LV) CMOS. The BP SOI pLDMOS features a P-type buried layer within the N-type SOI layer. The P-sinker and the P+ drain are implanted to connect the PBL, which forms a current conduction path in the on-state. W_P and L_P are the width and length of the PBL, respectively. D_P is the depth of the PBL and N_{BP} is its doping concentration. t_s and N_D are the thickness and doping concentration of the N-SOI layer. t_{ox} is the thickness of the buried oxide (BOX). The schematic cross sections of the PW and Con. SOI pLDMOS are also provided in Figs. 1(b) and 1(c).

In the on-state, in the presence of a negative gate-source voltage, the holes flow from the P+ source through the channel, P-sinker, and the PBL to the P+ drain, which is shown by the bold arrow head in Fig. 1. In the off-state the high voltage is applied to the source and gate, and the drain as well as the substrate are grounded. The PBL is depleted by the upper and lower PN junctions, resulting in a high N_{BP}

*Project supported by the National Natural Science Foundation of China (Grant No. 61176069), the State Key Laboratory Science Fund of Electronic Thin Films and Integrated Devices of China (Grant No. CXJJ201004), and the National Key Laboratory Science Fund of Analog Integrated Circuit, China (Grant No. 9140C090304110C0905).

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and low on-resistance. Note that the N-type region underneath the PBL is depleted by both the PBL and the inverted metal–insulator–semiconductor (MIS) structure consisting of the substrate, buried oxide, and the silicon-on-insulator layer (as shown in the dashed rectangle of Fig. 1). The PBL built in the N-type silicon-on-insulator layer causes multiple depletion and electric field reshaping, and thus, the P-sinker, PBL, and the N-type region are fully depleted to support the high voltage between the source and drain (the depleting directions are indicated by the arrow heads in Figs. 3(a)–3(c)).

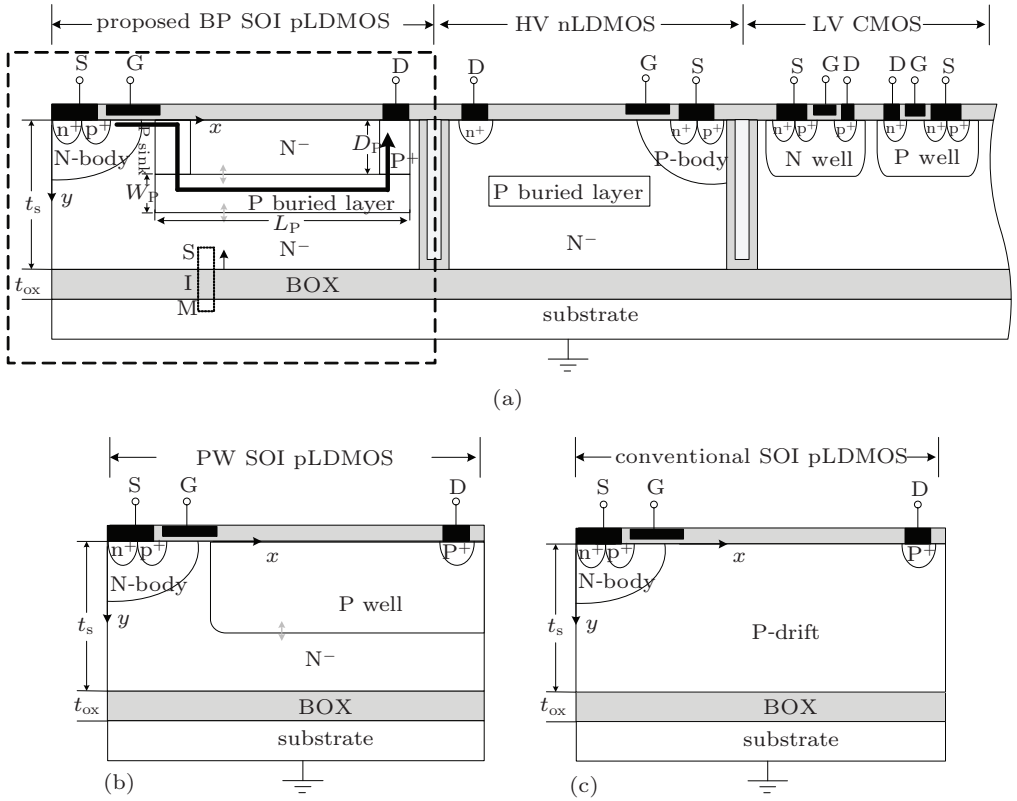


Fig. 1. Schematic cross sections of (a) BP SOI pLDMOS proposed in an integrated circuit, (b) PW SOI pLDMOS, (c) conventional SOI pLDMOS.

As a simplified one-dimensional (1D) analysis in the y direction, Fig. 2 provides a depiction of the vertical electric field at the midpoint of the BP SOI pLDMOS and PW SOI pLDMOS (shown in Fig. 1(b)) when the two devices are fully depleted. Based on the 1D Poisson's equation, the vertical electric field $E_y(y)$ for the BP SOI pLDMOS can be written as

$$\frac{\mathrm{d}E_y(y)}{\mathrm{d}y} = \frac{qN_\mathrm{D}}{\varepsilon_\mathrm{s}}, \quad 0 \le y \le D_\mathrm{P}, \quad (D_\mathrm{P}+W_\mathrm{P}) \le y \le t_\mathrm{s}, \tag{1}$$

$$\frac{\mathrm{d}E_y(y)}{\mathrm{d}y} = -\frac{qN_\mathrm{BP}}{\varepsilon_\mathrm{s}}, \quad D_\mathrm{P} \le y \le (D_\mathrm{P}+W_\mathrm{P}). \tag{2}$$

The boundary conditions are

$$\begin{cases} E_y(y)\,\big|_{y=0} = 0, \\ \varepsilon_\mathrm{s}E_y\,\big|_{y=t_\mathrm{s}^-} = \varepsilon_\mathrm{ox}E_y\,\big|_{y=t_\mathrm{s}^+}. \end{cases} \tag{3}$$

On the surface, the vertical electric field component is assumed to be zero.[15] At the SOI/BOX interface, the vertical electric field E_y satisfies the Gauss law. Combining Eq. (3) with Eqs. (1) and (2), we can obtain

$$\begin{cases} \dfrac{E_y(D_\mathrm{P})-E_y(0)}{D_\mathrm{P}} = \dfrac{qN_\mathrm{D}}{\varepsilon_\mathrm{s}}, \\ \dfrac{E_y(D_\mathrm{P}+W_\mathrm{P})-E_y(D_\mathrm{P})}{W_\mathrm{P}} = -\dfrac{qN_\mathrm{BP}}{\varepsilon_\mathrm{s}}, \\ \dfrac{E_y(t_\mathrm{s})-E_y(D_\mathrm{P}+W_\mathrm{P})}{t_\mathrm{s}-(D_\mathrm{P}+W_\mathrm{P})} = \dfrac{qN_\mathrm{D}}{\varepsilon_\mathrm{s}}. \end{cases} \tag{4}$$

The on-resistance is dominated by the drift region resistance (R_drift) for HV devices. The R_drift for BP SOI pLDMOS represents the resistance of the PBL, expressed as $R_\mathrm{drift}=L_\mathrm{P}/(q\mu N_\mathrm{BP}S)=L_\mathrm{P}/(q\mu N_\mathrm{BP}W_\mathrm{P}\cdot 1)$, where the S is the cross-sectional area of the current ($S=W_\mathrm{P}\cdot 1$, considering that distance perpendicular to the x–y plane is unit length). Therefore, higher doping dose Q_BP ($Q_\mathrm{BP}=N_\mathrm{BP}W_\mathrm{P}$) is conducive to the reduction of R_drift. According to Eq. (4), Q_BP can be calculated approximately as

$$Q_\mathrm{BP} = \frac{-\varepsilon_\mathrm{s}\left[E_y(D_\mathrm{P}+W_\mathrm{P})-E_y(D_\mathrm{P})\right]}{q} = \frac{\varepsilon_\mathrm{s}\cdot\left|\Delta E_y\right|}{q}, \tag{5}$$

From Eq. (5), we can conclude that the doping dose $Q \propto |\Delta E_y|$. A similar 1D analysis can be performed for the PW SOI pLDMOS. To ensure the full depletion at breakdown, both the $E_y(D_P + W_P)$ for BP SOI pLDMOS and the $E_y(D_{PW})$ for PW SOI pLDMOS are assumed to reach the maximum (absolute) value $-E_m$, i.e., $E_y(D_P + W_P) = E_y(D_{PW}) = -E_m$. Thus, for the PW SOI pLDMOS, the $|\Delta E_y|$ across the P-well is described as $|\Delta E_{y,PW}| = |(-E_m) - 0| = E_m$. For the BP SOI pLDMOS, owing to the positive field peak at the upper boundary of the PBL, the $|\Delta E_y|$ across the PBL is $|\Delta E_{y,PBL}| > E_m$. According to $Q \propto |\Delta E_y|$, Q_{BP} can be greatly increased compared with Q_{PW}, thus enabling a significant reduction in $R_{on,sp}$ of the proposed BP SOI pLDMOS.

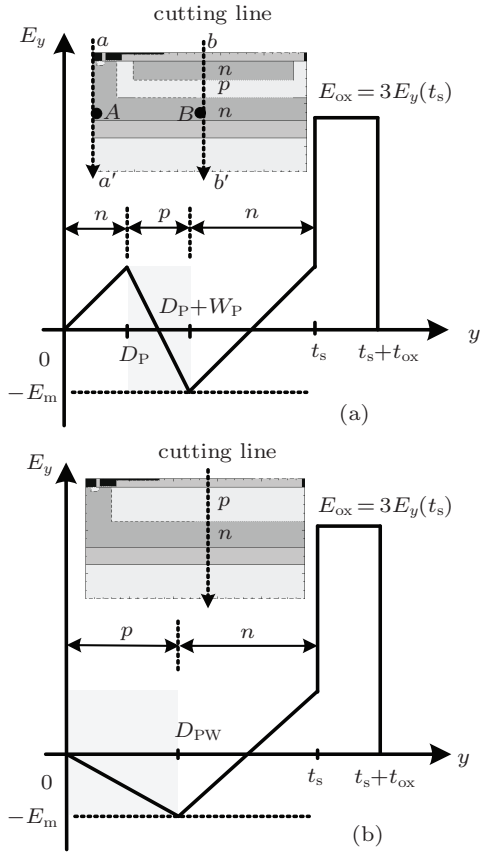


Fig. 2. Schematic depictions of electric field in the y direction at the midpoint of (a) BP SOI pLDMOS, (b) PW SOI pLDMOS.

Considering that the highest electric field is at point A shown in Fig. 2(a), $E_y(t_s)$ at point B (in the middle of the drift region) is approximated to be $E_c/2$, where E_c is the critical electric field (normally, $E_c = 30$ V/μm∼40 V/μm). Therefore, at the lower boundary of the PBL, $-E_c/2 \le E_y(D_P + W_P) < 0$ can be obtained by considering that $dE_y(y)/dy$ values along the aa' line and bb' line are approximately equal, because both variation rates are determined by $dE_y(y)/dy = qN_D/\varepsilon_s$. Analogously, $-E_c/2 \le E_y(D_{PW}) < 0$ is obtained for the PW SOI pLDMOS. It should be noted that almost all the electric flux lines of the ionized donors above the PBL can be absorbed by the ionized acceptors in the PBL. Consequently, $E_y(D_P)$ could reach a relatively high value, which is described by $E_y(D_P) = \alpha E_c$, where α denotes the impact factor of the depth of the PBL and the gate field plate. Under the optimal breakdown conditions, $0.5 < \alpha < 1$ can be achieved, enabling $E_c < |\Delta E_{y,PBL}| < 1.5E_c$. However, $|\Delta E_{y,PW}|$ can just reach $0.5E_c$ at most according to the above analysis. Thus, $2Q_{PW} < Q_{BP} < 3Q_{PW}$ can be achieved by appropriate optimization.

Another advantage of the BP SOI pLDMOS is the excellent process compatibility. Only one additional mask is needed for the BP SOI pLDMOS compared with that for the PW SOI pLDMOS. Owing to the choice of N-type SOI layer to form the BP SOI pLDMOS, it exhibits good compatibility with HV nLDMOS and conventional LV CMOS. It is worth pointing out that the BP SOI pLDMOS can be integrated directly with the triple RESURF nLDMOS as shown in Fig. 1(a). This benefit facilitates the fabrication of high performance HV complementary device in the same power integrated circuit (PIC).

3. Results and discussion

In order to demonstrate the multiple-dimensional depletion in the off-state, Fig. 3 shows equi-potential contours for the BP, PW, and Con. SOI pLDMOS at different values of drain voltage V_{DS}. In the off-state, the high voltage (V_{app}) is applied to the source and gate (i.e., $V_s = V_G = V_{app}$) with the handler wafer and the drain grounded (i.e., $V_{sub} = V_D = 0$ V) in practical operations. For convenience, equivalent voltage conditions in simulation are employed in the off-state: $V_s = V_G = 0$ V, and $V_{sub} = V_D = -V_{app}$.[16] The arrow heads denote the depleting directions, which indicate that the PBL is depleted by the upper and lower two PN junctions. Consequently, the dose in the PBL (i.e. Q_{BP}) is higher and thus $R_{on,sp}$ is lower than those of the PW and Con. SOI pLDMOS. Comparing Fig. 3(c) with Fig. 3(f), we see that the proposed BP SOI pLDMOS exhibits stronger electric field reshaping than the PW SOI pLDMOS, owing to the two field peaks induced at the PBL/N-junctions. In addition, the lateral and vertical PN junctions as well as the vertical MIS reshape the electric field, which is advantageous to achieve a high BV. It can be observed from Figs. 3(g), 3(h), and 3(i) that there is only the lateral N_{body}/P-junction depletion for the Con. SOI pLDMOS. There is no voltage drop between the substrate and the P-SOI layer below the drain during the depleting process. Thus the MIS structure is completely suppressed and cannot assist in depleting the P-SOI layer of the Con. SOI pLDMOS. This is the intrinsic reason why the Con. SOI pLDMOS does not meet the RESURF principle and suffers degraded BV and undesirably high $R_{on,sp}$.

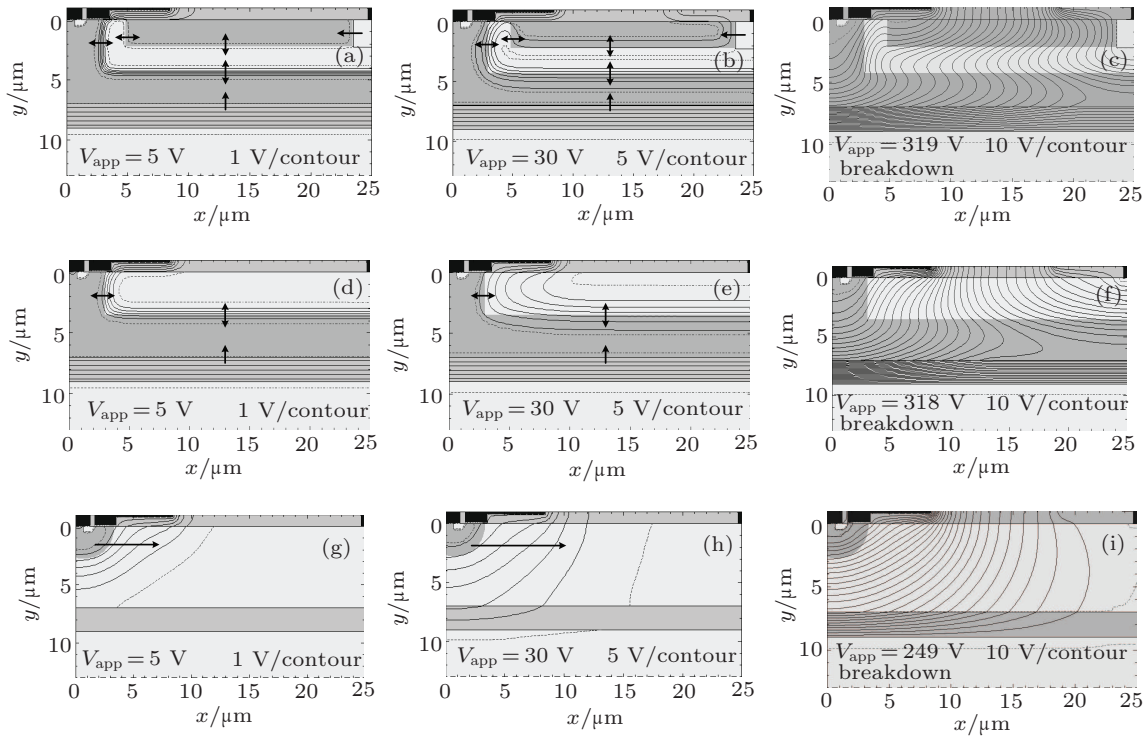


Fig. 3. Equipotential contours for BP, PW, and Con. SOI pLDMOS at different drain voltages ($t_s = 7$ μm and $t_{ox} = 2$ μm).

Figure 4(a) shows the comparisons of the vertical electric field distribution between the BP and PW SOI pLDMOS. The electric field reshaping induced by the PBL in the y direction is obvious. Two field peaks are induced at the upper and lower boundaries of the PBL, verifying the above 1D analysis. The simulation results accord well with the 1D analytical model. With $E_y(D_P) = 29$ V/μm and $E_y(D_P + W_P) = -15$ V/μm, $|\Delta E_{y,PBL}| = 44$ V/μm is attained. From Eq. (5), the Q_{BP} is obtained to be 2.9×10^{12} cm^{-2}, which is in good accordance with the simulation result of 2.8×10^{12} cm^{-2}. For the PW SOI pLDMOS, there is only one field peak, leading to $|\Delta E_{y,PW}| = |(-15 \text{ V}/\mu\text{m}) - 0| = 15$ V/μm. In consequence, the Q_{PW} allowed for the PW SOI pLDMOS is (1×10^{12} cm^{-2}) much lower than the Q_{BP} for the BP SOI pLDMOS. Therefore the greatest superiority of the BP SOI pLDMOS over the PW SOI pLDMOS consists in the significantly reducing $R_{on,sp}$ and maintaining a high BV.

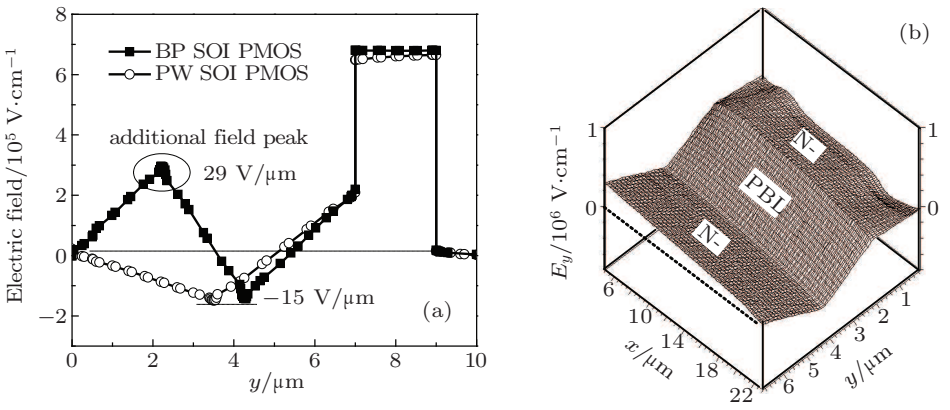


Fig. 4. (a) Vertical electric field distributions: (a) at the midpoint ($x = 13$ μm), and (b) 3D distribution of E_y for BP SOI pLDMOS.

The surface electric field distribution, vertical electric field, and potential distributions underneath the source regions of the BP, PW, and Con. SOI pLDMOS are shown in Fig. 5. Field plates are used, thus the surface electric field distributions of BP and PW SOI pLDMOS exhibit four field peaks in Fig. 5(a). Compared with the PW SOI pLDMOS, the BP SOI has a uniform surface field distribution. However, for the Con. SOI pLDMOS, the P-region underneath the drain is not effec-

tive to share the *BV*. Figure 5(b) shows the electric fields below the source regions of the three structures. Both the BP and PW SOI pLDMOS can achieve high field strength in the BOX, from 4.1×10^5 V/cm of the Con. SOI to 11.6×10^5 V/cm of the BP or PW SOI pLDMOS. The electric field of the Con. SOI pLDMOS varies with a negative slope in the *y* direction due to the negative ionized acceptor charges, leading to a low electric field of 1.5×10^5 V/cm on the SOI/BOX interface. Different from the Con. SOI pLDMOS, the BP SOI pLDMOS is built in the N-type SOI layer rather than P-type. The electric field in the N-type SOI layer varies with a positive slope. Therefore high electric field strengths on the SOI/BOX interface are obtained for the BP and PW SOI pLDMOS.

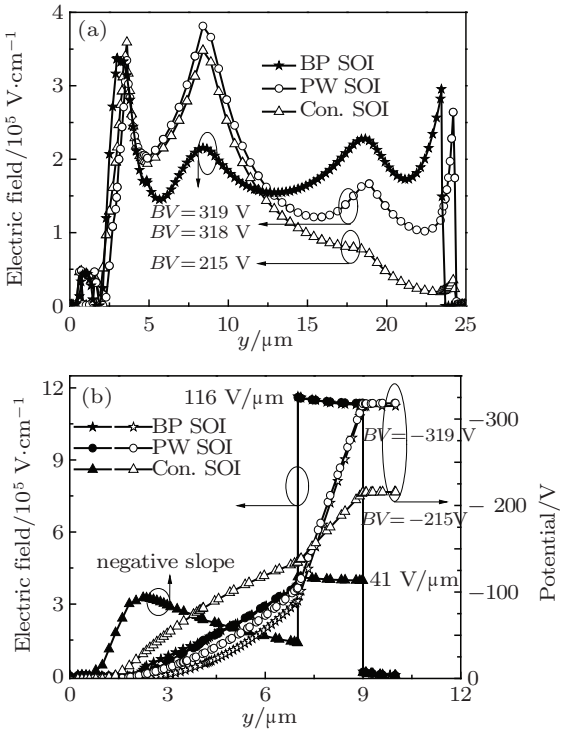


Fig. 5. (a) Surface electric field distributions, (b) electric field and potential distributions in the *y* direction ($x = 0.1$ μm) at breakdown.

Figure 6 shows the current flowline contours for the three structures. The current flows along the highly doped PBL for the BP SOI pLDMOS, while flowing along the top P-well for the PW SOI pLDMOS. Owing to the multiple depletion and enhanced RESURF effect, the optimal Q_{BP} of the BP SOI pLDMOS reaches 2.8×10^{12} cm^{-2}, while the optimal Q_{PW} of the PW SOI is 1.2×10^{12} cm^{-2}. Consequently, the $R_{on,sp}$ of the BP SOI pLDMOS (55 mΩ·cm^2) decreases by 34% compared with that of the PW SOI pLDMOS (83 mΩ·cm^2). For the Con. SOI pLDMOS, the *BV* exceeds 200 V only when the $N_A < 1\times10^{15}$ cm^{-3}, leading to the poor on-state performance.

Figure 7 shows the influences of N_D, N_{BP}, D_P on *BV* and $R_{on,sp}$. The N_{BP} and N_D need to be appropriately optimized. Each N_{BP} value corresponds to an optimal N_D, which increases with N_{BP} increasing as shown in Fig. 7(a). Too high (low) a value of N_D causes a high electric field in the source (drain) region, leading to premature breakdown. The maximum *BV*

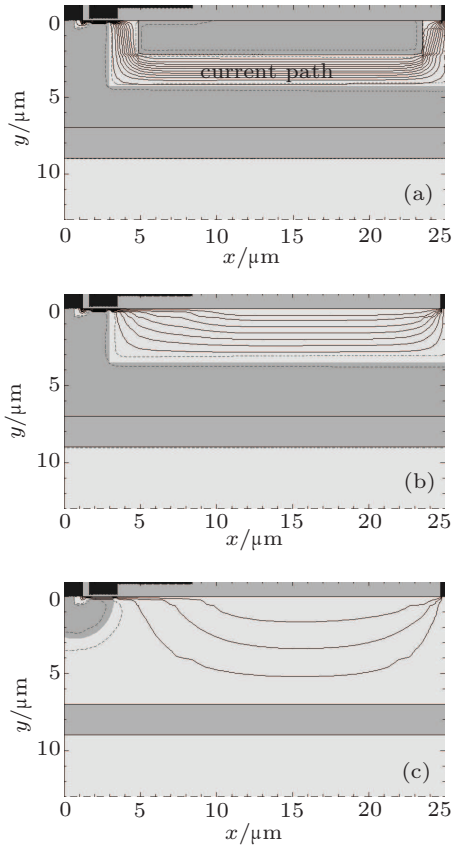


Fig. 6. Current flowline contours for (a) BP SOI pLDMOS, (b) PW SOI pLDMOS, (c) Con. SOI pLDMOS (2×10^{-7} A·μm^{-1}/contour).

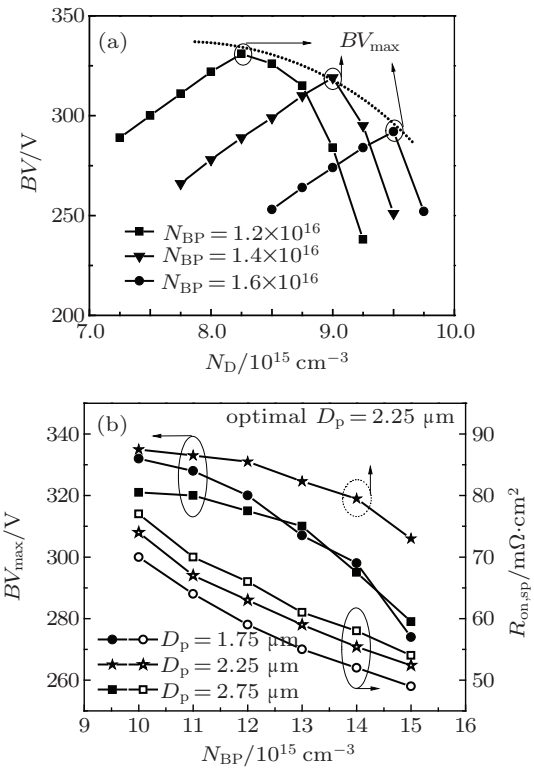


Fig. 7. Dependences of the *BV* and $R_{on,sp}$ on (a) N_D as a function of N_{BP}, (b) N_{BP} as a function of D_P.

[BV_{max}, marked by open circles in Fig. 7(a)] is obtained with the optimal N_D. As expected, the $R_{on,sp}$ decreases with N_{BP} increasing. Figure 7(b) shows the dependences of BV_{max} and $R_{on,sp}$ on N_{BP} at different values of D_P. Each BV_{max} is obtained at the optimal N_D for a given N_{BP}. The BV_{max} decreases with N_{BP} increasing for each D_P. A high N_{BP} leads to incomplete depletion, reducing the BV. There is a steady increase in $R_{on,sp}$ as D_P increases from 1.75 μm to 2.75 μm because of a lengthened current path. It can be seen from Fig. 7(b) that the optimal D_P is 2.25 μm, at which the utmost trade-off between the BV and $R_{on,sp}$ can be obtained.

Figure 8 gives the temperature distributions of the three devices. The maximum temperature values T_{max} are also given in Table 1. The temperature of substrate bottom is maintained at 300 K with $V_G = -20$ V in simulations. The heat is mainly dissipated through the heat sink attached to the substrate and thus temperature decreases from the surface to the substrate as shown in Fig. 8. For a silicon-on-insulator device, low thermal conductivity of the BOX (0.015 W/cm·K of SiO_2; 1.4 W/cm·K of Si) is responsible for severe self-heating effect (SHE). The temperature is extracted at a current of 3×10^{-5} A/μm (our baseline is the same on-state current for all the three structures). At the same current, a lower on-resistance is advantageous to alleviate the SHE. In Fig. 8(a) the T_{max} of the BP silicon-on-insulator reduces to 321 K from 369 K of conventional silicon-on-insulator. Figure 8(b) shows a comparison of the $R_{on,sp}$ versus BV between the three structures. The conventional silicon-on-insulator p-channel lateral double-diffused metal–oxide semiconductor suffers a degraded BV and high $R_{on,sp}$ due to the suppressed RESURF effect. The $R_{on,sp}$ of the conventional silicon-on-insulator p-channel lateral double-diffused metal–oxide semiconductor increases rapidly with the value of BV as observed in Fig. 8(b). The BP silicon-on-insulator p-channel lateral double-diffused metal–oxide semiconductor increases the value of BV and simultaneously achieves the reduction in $R_{on,sp}$ by 30% compared with the PW silicon-on-insulator p-channel lateral double-diffused metal–oxide semiconductor. The $R_{on,sp}$ of the BP silicon-on-insulator p-channel lateral double-diffused metal–oxide semiconductor increases more slowly with the value of BV than the PW and the conventional silicon-on-insulator p-channel lateral double-diffused metal–oxide semiconductor. A summary of the characteristics of the three structures is provided in Table 1. The BP silicon-on-insulator p-channel lateral double-diffused metal–oxide semiconductor exhibits the best improvement in terms of the $BV/R_{on,sp}$ trade-off and the thermal characteristic in the three structures.

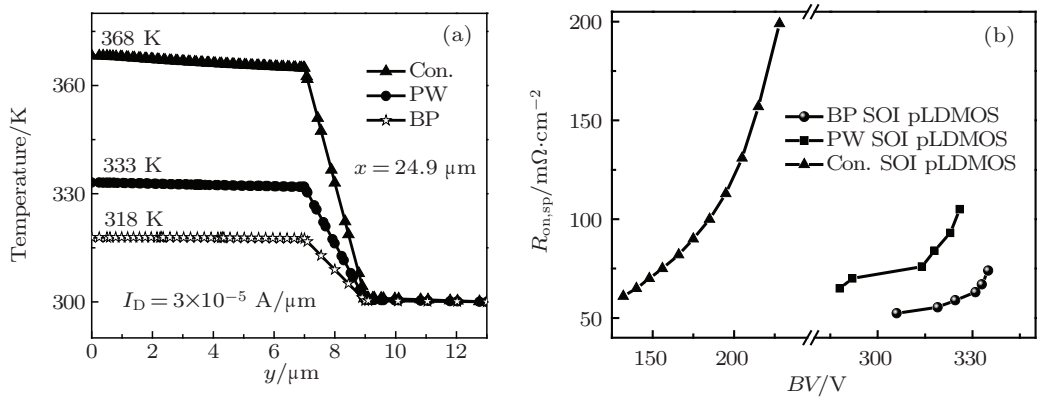


Fig. 8. (a) Temperature distributions in the y direction via the T_{max} point, and (b) $R_{on,sp}$ versus BV.

Table 1. Values of BV, $R_{on,sp}$, FOM, and T_{max} for BP, PW, and Con. SOI pLDMOS.

Device types	BV/V	$R_{on,sp}$/mΩ·cm^2	$(BV^2/R_{on,sp})$/(MW/cm^2)	T_{max}/K	Optimal doping dose of the P region/cm^{-2}
BP SOI pLDMOS	319	55	1.9	318	2.8×10^{12}
Con. SOI pLDMOS	215	157	0.3	368	0.56×10^{12}
PW SOI pLDMOS	318	83	1.2	333	1.2×10^{12}

4. Conclusion

A low on-resistance p-channel SOI LDMOS is proposed and investigated by simulation. In the on-state, the PBL acts as a low resistance current path. In the off-state, the PBL and the N-type SOI layer cause multiple depletion and electric field reshaping, leading to an enhanced BV and reduced $R_{on,sp}$. Compared with the Con. SOI pLDMOS, the proposed BP SOI pLDMOS increases BV from 215 V to 319 V and re-

duces $R_{on,sp}$ by 65% with the device dimensions of $t_s = 7$ μm, $t_{ox} = 2$ μm, $L_d = 25$ μm. The thermal characteristic is improved. Furthermore, the BP SOI pLDMOS is compatible with the HV nLDMOS devices and low voltage CMOS circuitry, thus facilitating the fabrication of high voltage integrated circuits (HVICs).

Appendix A: List of symbols

List of symbols		
W_P	width of the P-buried layer	for the BP SOI pLDMOS
L_P	length of the P-buried layer	
D_P	depth of the P-buried layer	
N_D	doping concentration of the N-SOI layer	
N_{BP}	doping concentration of the P-buried layer	
Q_{BP}	doping dose of the P-buried layer $Q_{BP} = N_{BP}W_P$	
$\Delta E_{y,PBL}$	the change of E_y across the P-buried layer, $\Delta E_{y,PBL} = E_y(D_P + W_P) - E_y(D_P)$	
D_{PW}	depth of the P well	for the PW SOI pLDMOS
Q_{PW}	doping dose of the P well	
$\Delta E_{y,PW}$	the change of E_y across the P well, $\Delta E_{y,PW} = E_y(D_{PW}) - E_y(0)$	
N_A	doping concentration of the P-SOI layer	for the Con. SOI pLDMOS

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