Fabrication and characterization of V-gate AlGaN/GaN high-electron-mobility transistors*

Zhang Kai(张 凯)[a], Cao Meng-Yi(曹梦逸)[a], Chen Yong-He(陈永和)[a], Yang Li-Yuan(杨丽媛)[a], Wang Chong(王 冲)[a], Ma Xiao-Hua(马晓华)[a)b)†], and Hao Yue(郝 跃)[a]

[a] *Key Laboratory for Wide Band-Gap Semiconductor Materials and Devices, School of Microelectronics, Xidian University, Xi'an* 710071, *China*
[b] *School of Technical Physics, Xidian University, Xi'an* 710071, *China*

(Received 17 September 2012; revised manuscript received 27 November 2012)

V-gate GaN high-electron-mobility transistors (HEMTs) are fabricated and investigated systematically. A V-shaped recess geometry is obtained using an improved Si_3N_4 recess etching technology. Compared with standard HEMTs, the fabricated V-gate HEMTs exhibit a 17% higher peak extrinsic transconductance due to a narrowed gate foot. Moreover, both the gate leakage and current dispersion are dramatically suppressed simultaneously, although a slight degradation of frequency response is observed. Based on a two-dimensional electric field simulation using Silvaco "ATLAS" for both standard HEMTs and V-gate HEMTs, the relaxation in peak electric field at the gate edge is identified as the predominant factor leading to the superior performance of V-gate HEMTs.

Keywords: high-electron-mobility transistors, electric-field distribution, field plate, current dispersion

PACS: 73.40.Kp, 73.61.Ey, 85.30.Tv **DOI:** 10.1088/1674-1056/22/5/057304

1. Introduction

AlGaN/GaN high-electron-mobility transistors (HEMTs) are good candidates for power radio-frequency (RF) applications due to their high breakdown field, high-mobility two-dimensional electron gas (2DEG), and high drift velocity.[1–4] The high microwave power density of GaN HEMTs relies on both the high breakdown voltage and the effective suppression of direct current (DC)–RF dispersion. To achieve this, various technologies have been developed. Among these, a surface-state passivation layer to stabilize the surface is considered to be a necessity by many groups.[5–7] Moreover, field-modulating plates have been shown to be effective in both enhancing the breakdown voltage and eliminating current collapse by alleviating the peak electric field at the edge of the gate.[8,9] Already, several field plate (FP) technologies have been demonstrated, including gate-connected FPs,[10] source-connected FPs,[11] gate-connected dual-FPs,[12] and gate-source-connected dual-FPs.[13] More than 40 W/mm of output power at 4 GHz was achieved with dual FPs. Therefore, the benchmarks of GaN-based high-electron-mobility transistors have been dramatically raised with the help of multi-field-plate structures.

The effects of these conventional FP structures are, however, insufficient because an electric field still concentrates at the gate edge. This is due to the fact that traditional recess etching technologies pursue the vertical gate sidewall, which in turn results in the excess electric-field crowding due to point discharge effect. Hence, reshaping the recess sidewall geometry to eliminate the negative effect could further enhance devices' microwave power performance. To obtain the goal, HEMTs with integrated slant field plates had been presented to successfully achieve the high breakdown voltage, which was considered to be the result of the alleviation of the peak electric field at the drain edge of the gate.[14–16] However, no comparisons of the detailed characteristics of these devices with those of conventional HEMTs have been reported.

Meanwhile, because of the difficulties in the manufacturing process, there are few reports of HEMTs made with such a structure. In the present work, by using an improved recess etching condition, we demonstrate the fabrication of V-gate HEMTs, which features a linearly graded gate sidewall, and we conduct comparisons with standard HEMTs in DC, pulsed and AC small-signal characteristics. Electric field distributions of these structures are also presented, using a two-dimensional device simulator, the Silvaco "ATLAS", to explain the effectiveness of V-gate HEMTs in electric-field management.

2. Devices and experiments

The AlGaN/GaN hetero-junction structure in this paper was grown by metal-organic chemical vapor deposition (MOCVD) on two-in sapphire substrates. Both the GaN buffer layer (2 μm) and the AlGaN layer (25 nm) were unintentionally doped, and the AlGaN layer had an Al content of around 30%. Device processing started with the Ti/Al/Ni/Au (30 nm/180 nm/40 nm/60 nm) source and drain electrodes.

*Project supported by the Program for New Century Excellent Talents in University, China (Grant No. NCET-12-0915) and the National Natural Science Foundation of China (Grant Nos. 61106106 and 61204085).

†Corresponding author. E-mail: xhma@xidian.edu.cn

© 2013 Chinese Physical Society and IOP Publishing Ltd

These were consecutively annealed at 830 °C for 30 s under nitrogen ambience. The resulting ohmic contact resistance was about 0.3 Ω·mm. Device isolation was achieved by Cl_2-based plasma etching to a depth of 80 nm. This was followed by the deposition of an 80-nm plasma enhanced chemical vapor deposition (PECVD) Si_3N_4 passivation layer. Then a portion of the wafer was subject to the standard etching process, in which the SiN was removed in the recess openings using a CF_4 reactive ion etch (RIE) with a gas flow of CF_4/O_2:20/2 sccm at a pressure of 5 mT. Another portion of the wafer was done with double-layer lithography in order to yield a liftoff overhang, facilitating the lateral flow of reactive ions. This was followed by recess etching in conditions similar to the standard process except at a higher pressure of 28 mT. Through adjusting the etching chamber pressure, the slope of the etched sidewall could be well controlled. A low pressure of 5 mT led to an ion flux mostly in the normal direction, giving a vertical sidewall. However, lateral scattering of reactive ions could be dramatically enhanced due to the reduction in the ion mean free path at a high chamber pressure (28 mT), which resulted in drastic lateral etching of the SiN sidewall. As a consequence, a V-shaped recess with a narrowed gate footprint L_G of 0.43 μm was achieved as shown in Fig. 1.

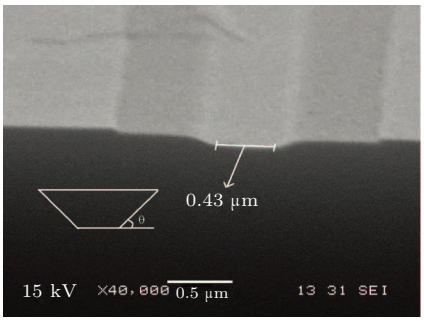


Fig. 1. SEM scan of the fabricated gate recess profile for a V-gate HEMT after SiN recess etching. An angle of about 30° ($\theta = 30°$) can be observed.

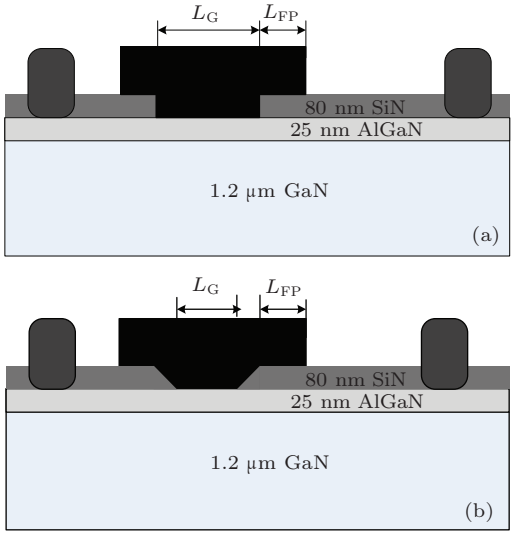


Fig. 2. (color online) Schematic diagrams of (a) standard HEMT and (b) V-gate HEMT.

After etching the SiN recess, an Ni/Au/Ni gate electrode was evaporated onto the whole wafer. All devices had a lithographic gate length of 0.5 μm, a gate width of 100 μm, gate-source spacing of 0.7 μm, and gate-drain spacing of 2.8 μm. An FP length of 0.3 μm (L_{FP}=0.3 μm) was utilized to increase the breakdown voltage in both structures, as described in Fig. 2.

3. Results and discussion

Figure 3 illustrates the transfer and transconductance characteristics for standard HEMTs and V-gate HEMTs at a drain bias of 10 V. Both devices pinch off completely at about $V_{gs} = -3.7$ V. Compared with the standard HEMTs, V-gate HEMTs exhibit a 17% increase in the maximum transconductance from 207 mS/mm to 243 mS/mm, which is due to a narrower gate footprint.

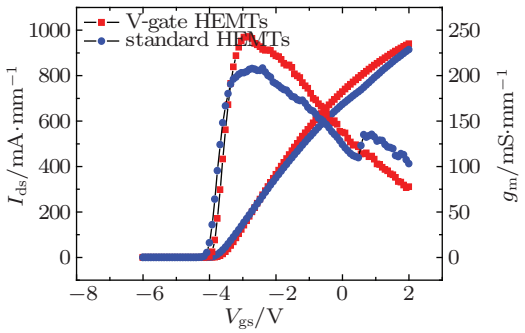


Fig. 3. (color online) Measured transfer and transconductance characteristics for V-gate HEMTs and standard HEMTs at $V_{ds} = 10$ V.

The OFF-state current–voltage (I–V) characteristics of both devices are shown in Fig. 4, with V_{gs} biased at −6 V. The three-terminal breakdown voltage for V-gate HEMTs is slightly improved from 108 V to 123 V, measured at a drain current density of 1 mA/mm. It should be noted that the buffer leakage dominates the OFF-state current before the breakdown occurs. Furthermore, the gate leakage is dramatically suppressed with only 0.034 mA/mm at $V_{ds} = 100$ V, which is five times lower than that of the standard HEMTs. The electric field relaxation introduced by the graded field plate reduces electron tunneling from the gate, which must be the cause of this suppressed gate leakage current.

The pulsed I–V measurements were performed using Keithley 4200SCS to characterize the DC-to-RF dispersion in the HEMTs. They were measured by pulsing both the drain-source voltage and gate-source voltage synchronously away from the bias point ($V_{GSQ} = -6$ V, $V_{DSQ} = 20$ V) to the point where the current is measured. For these measurements, pulse width and duty cycle were 500 ns and 0.05%, respectively. The results are shown in Fig. 5. For both HEMTs, the self-heating causes the negative resistance effect in the saturation region of DC curves (see Fig. 5(a)). However, with L_G of V-gate HEMTs, the saturation current declines much less (see

Fig. 5(b)), indicating the presence of a more pronounced short channel effect. With the inclusion of an integrated slant field plate, a remarkable improvement in the pulsed *I*–*V* characteristics for V-gate is observed. The collapse factor, defined as $(I_{\rm pulse} - I_{\rm DC})/I_{\rm DC}$ at $V_{\rm ds} = 3$ V and $V_{\rm gs} = -1$ V, is significantly reduced from 29% for standard HEMTs to 8.2% for V-gate HEMTs, demonstrating a substantial suppression of current dispersion. Considering the identical Si_3N_4 passivation conditions and GaN material characteristics, this improvement can be attributed to the mitigation of the electric field at the gate edge resulting in lower electron injection into surface traps,[15,17] as will be shown below.

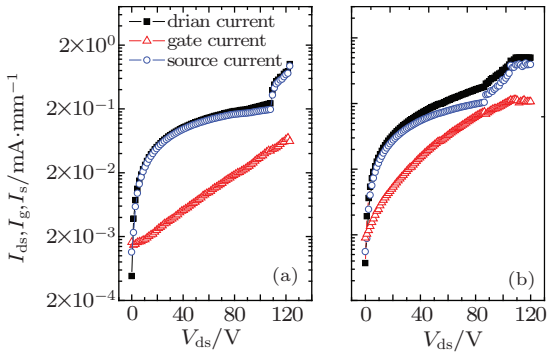


Fig. 4. (color online) Three-terminal OFF-state *I*–*V* characteristics of (a) V-gate and (b) standard HEMTs.

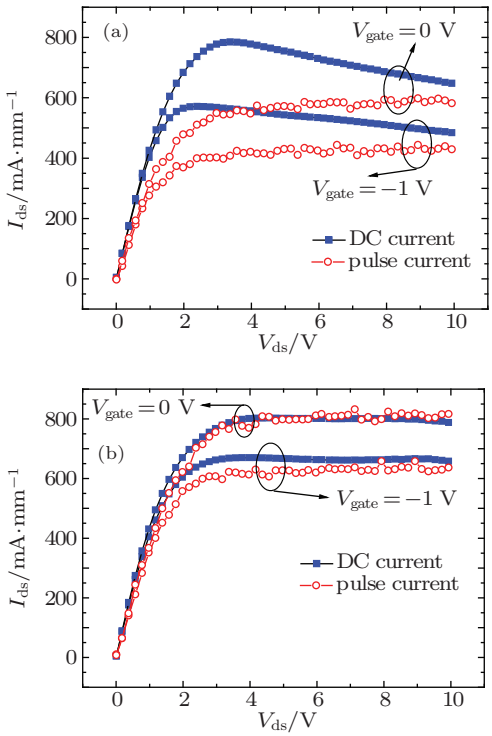


Fig. 5. (color online) DC and pulsed *I*–*V* characteristics of (a) standard HEMTs, and (b) V-gate HEMTs. Quiescent bias is $(V_{\rm DSQ}, V_{\rm GSQ}) = (20\ {\rm V}, -6\ {\rm V})$.

To compare the electric field distributions of both structures, ATLAS simulation was employed. As shown in Fig. 6, a more even electric field distribution around the gate electrode is observed in V-gate HEMTs as compared with the standard HEMTs. Figure 6(c) presents the detailed electric field distribution at the Si_3N_4/AlGaN interface at the gate edge, simulated at $V_{\rm ds} = 20$ V and $V_{\rm gs} = -6$ V. For a V-gate device, the peak electric field is suppressed by more than 10% compared to that of a standard device, which is due to the inclusion of the linearly graded field plate effect. With a standard vertical gate sidewall, the electric field concentrates at the gate edge due to point discharge effect. However, some of the electric field lines from the drain electrode are screened by the

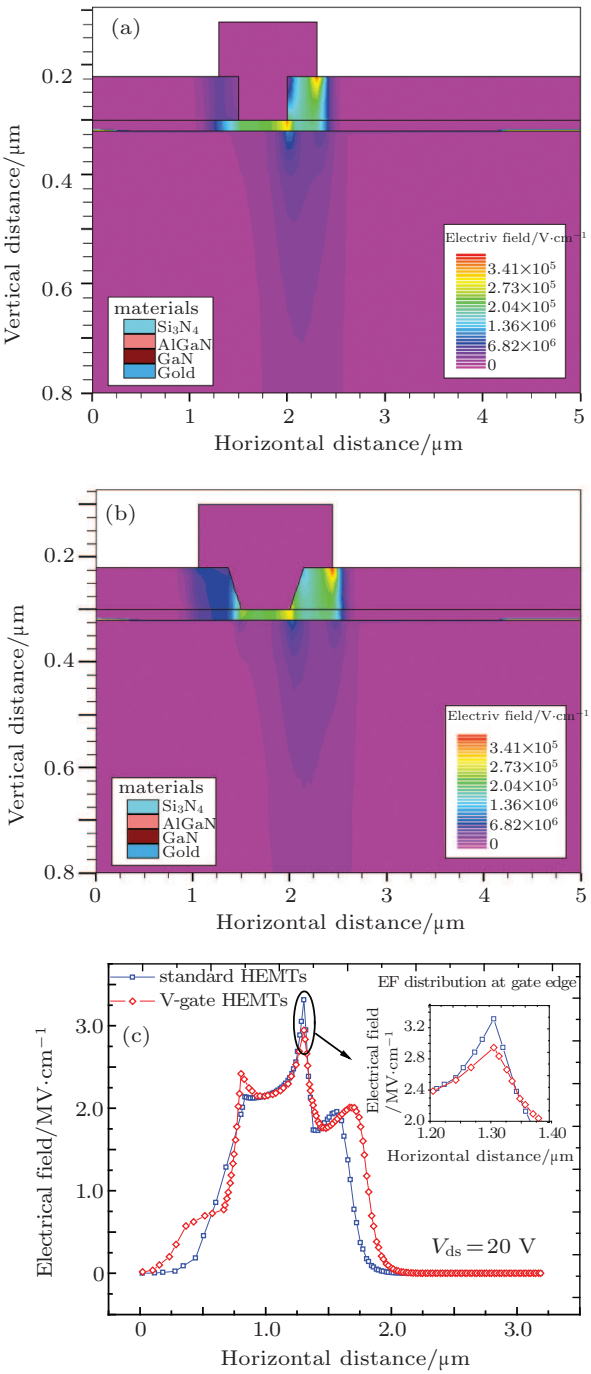


Fig. 6. (color online) Simulated electric field distribution (a) for standard HEMTs, (b) for V-gate HEMTs with an angle of 30°, and (c) at Si_3N_4/AlGaN interface of both HEMTs. The inset shows the peak electric field at the gate edge from 3.3 MV/cm to 2.9 MV/cm.

linearly graded sidewall in the V-gate devices. This evens out the electric field distribution, thus reducing the magnitude of the electric field at the gate edge. This electric field modulation is believed to be responsible for both the improvement in the gate leakage and the current dispersion characteristics.

The RF small-signal performance of the transistor was also investigated by measuring S-parameters from 10 MHz to 40 GHz by using an Agilent E8363 vector network analyzer. The value of the unity current gain cutoff frequency (f_T) is determined by the extrapolation of the current gain $|h_{21}|$. For V-gate HEMTs, the maximum f_T decreased from 15.8 GHz to 15.2 GHz, and the small signal power gain is also degraded slightly (see Fig. 7). This is attributed to an increase in the input capacitance ($C_{GS}+C_{GD}$), which is introduced by the linearly graded field plate.

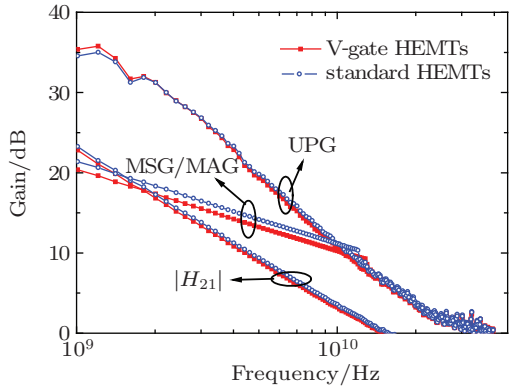


Fig. 7. (color online) Comparison of small-signal measurements of V-gate HEMTs and standard HEMTs.

4. Conclusion

We demonstrated the fabrication of V-gate HEMTs and performance comparisons with the standard HEMTs. The V-gate HEMTs showed both better breakdown and pulsed *I*–*V* characteristics compared with the standard HEMTs, despite a slightly degraded frequency response. A physics-based two-dimensional simulation was employed to illustrate the electric field modulation effect of the integrated linearly graded field plate. A 10% reduction in peak electric field at the drain-side gate edge for V-gate HEMTs was responsible for the improved device characteristics. The results indicate that V-gate HMETs are very promising for microwave high-power applications.

References

[1] Ando Y, Okamoto Y, Miamoto H, Nakayama T, Inoue T and Kuzuhara M 2003 *IEEE Electron Device Lett.* **24** 289
[2] Wu Y F, Saxler A, Moore M, Smith R P, Sheppard S and Chavarkar P M 2004 *IEEE Electron Device Lett.* **25** 117
[3] Wu Y F, Moore M, Saxler A, Wisleder T and Parikh P 2006 *Device Research Conference*, June 26–28, 2006, PA, USA, p. 151
[4] Xie G, Edward X, Niloufar H, Zhang B, Fred Y F and Wai T N 2012 *Chin. Phys. B* **21** 086105
[5] Hao Y, Yang L, Ma X H, Ma J G, Cao M Y, Pan C Y, Wang C and Zhang J C 2011 *IEEE Electron Device Lett.* **32** 626
[6] Yang L, Hu G Z, Hao Y, Ma X H, Quan S, Yang L Y and Jiang S G 2010 *Chin. Phys. B* **19** 047301
[7] Bruce M G, Kenneth K C, Chumbes E M, Joseph A S, James R S and Lester F E 2000 *IEEE Electron Device Lett.* **21** 268
[8] Sun H F and Bologesi C R 2007 *IEEE Electron Lett.* **43** 23
[9] Koudymov A, Adivarahan V, Simin G and Asif K M 2005 *IEEE Electron Device Lett.* **26** 704
[10] Brannick A, Nick A Z, Brian K R, James R S, William J S and Lester F E 2009 *IEEE Electron Device Lett.* **30** 436
[11] Okamoto Y, Ando Y, Nakayama T, Hataya K, Miyamoto H, Inoue T, Senda M, Hirata K, Kosaki M, Shibata N and Kuzuhara M 2004 *IEEE Electron Device Lett.* **51** 2217
[12] Wei W, Lin R B, Feng Q and Hao Y 2008 *Acta Phys. Sin.* **57** 467 (in Chinese)
[13] Wu Y F, Moore M, Wisleder T, Chavarkar P M, Mishra U K and Parikh P 2004 *Electron Devices Meeting 2004 IEDM Technical Digest. IEEE International*, December 13–15, 2004, CA, USA, p. 1078
[14] Xing H, Dora Y, Chini A, Heikman S and Mishra U K 2004 *IEEE Electron Device Lett.* **25** 161
[15] Ando Y, Wakejima A, Okamoto Y, Nakayama T, Ota K, Yamanoguchi K, Murase Y, Kasahara K, Matsunaga K, Inoue T and Miyamoto H 2005 *IEDM Tech. Dig*. p. 576
[16] Dora Y, Chakraborty A, McCarthy L, Keller S, DenBaars S P and Mishra U K 2006 *IEEE Electron Device Lett.* **27** 713
[17] Brannick A, Zakhleniuk N A, Ridley B K, Shealy J R, Schaff W J and Eastman L F 2009 *IEEE Electron Device Lett.* **30** 436