Dual-gate lateral double-diffused metal–oxide semiconductor with ultra-low specific on-resistance*

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A new high voltage trench lateral double-diffused metal–oxide semiconductor (LDMOS) with ultra-low specific on-resistance ($R_{on,sp}$) is proposed. The structure features a dual gate (DG LDMOS): a planar gate and a trench gate inset in the oxide trench. Firstly, the dual gate can provide a dual conduction channel and reduce $R_{on,sp}$ dramatically. Secondly, the oxide trench in the drift region modulates the electric field distribution and reduces the cell pitch but still can maintain comparable breakdown voltage (BV). Simulation results show that the cell pitch of the DG LDMOS can be reduced by 50% in comparison with that of conventional LDMOS at the equivalent BV; furthermore, $R_{on,sp}$ of the DG LDMOS can be reduced by 67% due to the smaller cell pitch and the dual gate.

Keywords: breakdown voltage, specific on-resistance, dual gate, oxide trench

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1. Introduction

In recent years, the breakdown voltage (BV) has been the focus of power lateral double-diffused metal–oxide semiconductor (LDMOS) field-effect transistors.[1–6] However, the long drift region, which is essential to sustaining high voltage in power lateral metal–oxide semiconductor field-effect transistors (MOSFETs), limits the improvement in the specific on-resistance ($R_{on,sp}$). In order to reduce the $R_{on,sp}$ and increase the current density while maintaining a high breakdown voltage, numerous structures and technologies were proposed.[7–14] The $R_{on,sp}$ can be reduced by introducing a superjunction into the power MOSFET structure.[11] Besides, a secondary drift region, which is placed under the drift region, is utilized to further improve the $R_{on,sp}$ and BV for CLAVER LDMOS structure.[12] In these cases, $R_{on,sp}$ is reduced by optimizing the drift region of the device. On the other hand, the combination of planar and trench gate structure has been investigated.[13,14] In contrast, the $R_{on,sp}$ of power LDMOS can be further reduced when the resistances of the channel region and the drift region are improved simultaneously.

Here, we propose a novel trench LDMOS with dual gate (DG LDMOS) and an oxide trench in the drift region. A planar gate and a trench gate integrated in this novel structure can form a dual gate. This dual gate not only can provide an additional conduction channel to mitigate the resistance of the channel region, but also can fold the drift region and reduce the cell pitch but still maintain comparable BV. These two aspects can lead to low $R_{on,sp}$ compared with that by the optimized conventional LDMOS (C-LDMOS) and planar gate trench-type LDMOS (PG LDMOS) with a similar BV. MEDICI TCAD simulator is used to help analyze the electrical characteristics of the proposed dual-gate structure.

2. Device structure

The schematic cross section view of the proposed DG LDMOS is shown in Fig. 1. In the drift region, an oxide trench is located in a region between the drain and the source. An additional trench gate is introduced in this oxide trench. The dual gate is formed by the trench gate and the planar gate. On the one hand, in the ON-state, dual conduction channels are formed, and thus, the current can flow through both the surface channel and the vertical channel (along the oxide trench sidewall). The lower $R_{on,sp}$ can be obviously obtained. On the other hand, in the OFF-state of the DG LDMOS, the oxide trench folds the drift region in the vertical direction, thereby increasing the effective drift region length. In comparison with the conventional LDMOS, the proposed DG LDMOS consumes small cell pitch at the comparable breakdown voltage (BV). To fabricate the oxide trench and trench gate structure, many fabrication methods are reported.[15–17] Based on these fabrication methods, the proposed DG LDMOS can be fabricated only by employing an extra planar gate. In Fig. 1, w_T and t_T are the width and depth of the oxide trench, respectively; t_S and N_d are the thickness and the doping concentration of the

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n-type silicon layer, respectively; P_{sub} is the doping concentration of the p-type substrate. Thickness $t_S = 7$ μm is used in this paper. Furthermore, N_d is optimized in order to obtain the maximum BV for each device.

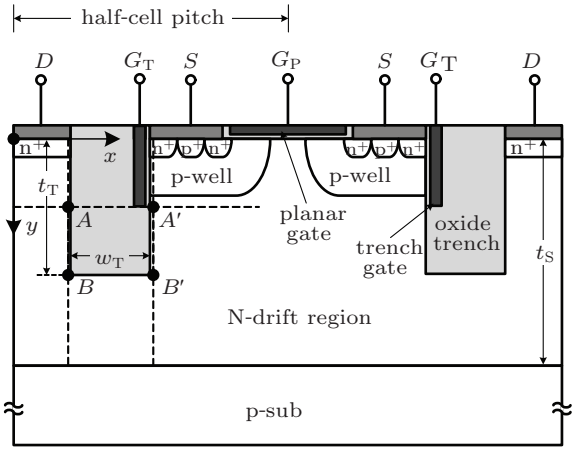


Fig. 1. Schematic cross section of DG LDMOS.

3. Simulation results and discussion

In the ON-state, the inversion channel can be formed at the sidewall of the trench gate and under the planar gate. Compared with single channel device in C-LDMOS, and PG LDMOS, the proposed dual-gate LDMOS offers a large conduction current region, resulting in a reduced $R_{on,sp}$. The forward I_{ds}–V_{ds} characteristics of the proposed dual-gate LDMOS are shown in Fig. 2(a) for three different combinations of the two gate voltages (G_T and G_P). As shown in this figure, the drain current can be independently controlled by the planar gate (G_P contact) and the trench gate (G_T contact), but in single-channel operation, the DG LDMOS exhibits a relatively low saturation current: 9 mA/mm with the biased planar gate only, and 24 mA/mm with the biased trench gate only. When the dual gate is biased at the same time, a larger saturation current of 51 mA/mm is obtained, attributing to two current paths. Thus, it is evident that the dual gates of the DG LDMOS should be biased simultaneously in order to reduce $R_{on,sp}$. Figure 2(b) illustrates the current flowing through the vertical channel, the planar channel and the dual channels when the dual gate is biased simultaneously. It indicates that the threshold voltage of the vertical channel is almost the same as that of the planar channel. This can be explained from the following two aspects: the trench gate shields the influence of the electric field in the oxide trench on the dual channels; the similar diffused impurity concentration distributions and the same thickness values of gate oxide for the dual channels. These two aspects can lead to the fact that the electron concentrations in the inversion layers of the two channels are similar to each other as illustrated in the inset of Fig. 2(b). From this figure, similar electron distributions in the inversion layer can be observed along the two channels when $V_{gs} = 1.5$ V.

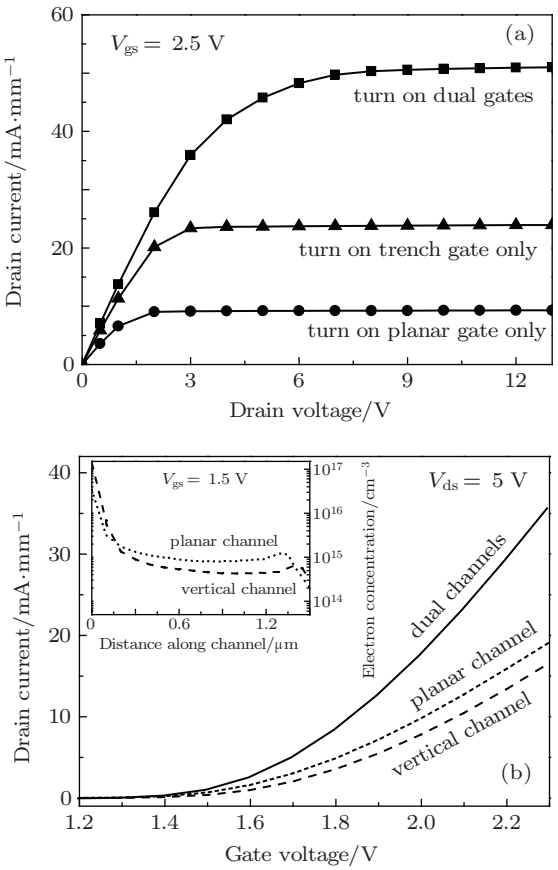


Fig. 2. Forward characteristic curves of (a) I_{ds}–V_{ds} and (b) I_{ds}–V_{gs} for the proposed dual-gate LDMOS. The inset in panel (b) shows the corresponding electron distributions along the dual channels. (t_S = 7 μm, t_T = 4 μm, w_T = 3.5 μm, $N_d = 4.5 \times 10^{15}$ cm^{-3}, $P_{sub} = 3.5 \times 10^{15}$ cm^{-3}, half-cell pitch = 9.5 μm.)

Figure 3 shows the current flowline contours for DG LDMOS (see Fig. 3(a)), PG LDMOS (see Fig. 3(b)) and C-LDMOS (see Fig. 3(c)) at $V_{gs} = 5$ V, $V_{ds} = 1$ V. Comparing Fig. 3(a) with Fig. 3(b), it can be seen that an additional vertical channel is formed along the oxide trench sidewall for DG LDMOS. As a result, the drain current of 16 mA/mm flows through the vertical channel and the planar channel at the same time. The drain currents of PG LDMOS and C-LDMOS are limited by the single channel compared with the drain current of DG LDMOS. The drain current thus decreases to 8.4 mA/mm for the PG LDMOS, and it reduces to 10.7 mA/mm for the C-LDMOS. So the drain current decreases to 53% for the PG LDMOS, and it reduces to 66.9% for the C-LDMOS in comparison with that of the DG LDMOS.

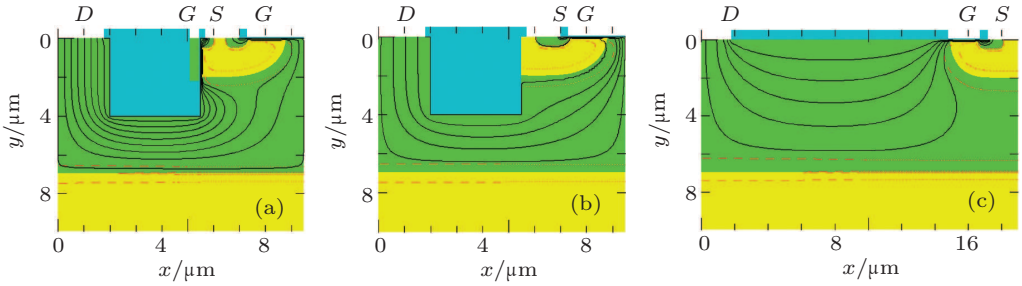


Fig. 3. (color online) Current flowline contours for (a) DG LDMOS ($N_d = 4.5\times10^{15}$ cm^{-3}, $I_{ds} = 16$ mA/mm), (b) PG LDMOS ($N_d = 4.3\times10^{15}$ cm^{-3}, $I_{ds} = 8.4$ mA/mm), and (c) C-LDMOS ($N_d = 2.1\times10^{15}$ cm^{-3}, $I_{ds} = 10.7$ mA/mm). ($t_T = 4$ μm, $w_T = 3.5$ μm and half-cell pitch = 9.5 μm for DG and PG LDMOS. Half-cell pitch = 19 μm for C-LDMOS in order to obtain the comparable BV. $t_S = 7$ μm, $P_{sub} = 3.5\times10^{15}$ cm^{-3}. 2 mA·mm^{-1}/contour)

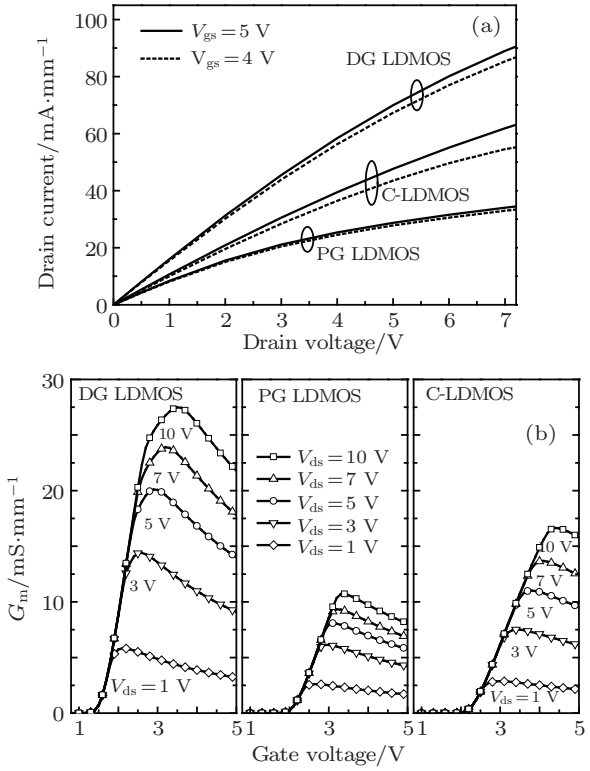


Fig. 4. Transfer characteristic curves of (a) I_{ds}–V_{ds} and (b) G_m at the comparable BV, with the same structure parameters as those in Fig. 3.

The output characteristics of DG LDMOS, PG LDMOS, and C-LDMOS are compared in Fig. 4(a) at the equivalent BV (221 V∼ 228 V). For DG LDMOS and PG LDMOS, the oxide trench folds the drift region, and thus, the cell pitch decreases but can still hold the high BV. The cell pitch of C-LDMOS is increased in order to obtain the comparable BV. Owing to the contribution of the dual-gate, DG LDMOS exhibits the largest drain current in Fig. 4(a). The drain current of 16 mA/mm is obtained for DG LDMOS at $V_{ds} = 1$ V and $V_{gs} = 5$ V, which is larger than that of PG LDMOS (8.4 mA/mm) and also larger than that of C-LDMOS (10.7 mA/mm). Therefore, the low $R_{on,sp}$ of 5.9 mΩ·cm^2 is obtained for DG LDMOS at $V_{gs} = 5$ V, while that of PG LDMOS is 11.3 mΩ·cm^2. Note that although the drain current of C-LDMOS is higher than that of PG LDMOS, the $R_{on,sp}$ of C-LDMOS is higher due to its larger cell pitch at the equivalent BV. The transconductance (G_m, $G_m = I_{ds}/V_{gs}$) as a function of V_{gs} is shown in Fig. 4(b). It is obvious that the G_m of DG LDMOS is much higher than that of PG LDMOS and also that of C-LDMOS in the same bias conditions. The peak G_m of 5.8 mS/mm is obtained at $V_{ds} = 1$ V and $V_{gs} = 2.1$ V for DG LDMOS. However, the values of G_m for PG LDMOS and C-LDMOS are both less than 3 mS/mm when $V_{ds} = 1$ V.

In the OFF-state, BV is improved by the oxide trenches of DG LDMOS and PG LDMOS, which results in a smaller cell pitch at the equivalent BV. Figures 5(a) and 5(b) show the lateral electric fields along the line of surface (see Fig. 5(a)) and $y = 2.2$ μm (AA' line in Fig. 1) (see Fig. 5(c)) for DG LDMOS, PG LDMOS, and C-LDMOS. Since an oxide trench is inserted between the source and the drain, the effective drift region length for DG LDMOS is increased and also is for PG LDMOS. This helps to achieve smaller half-cell pitch with the same BV. In other words, the surface electric field between the source and the drain is enhanced by the oxide trench and thus the half-cell pitch is reduced at the comparable BV. As shown in Fig. 5(a), the electric field strength near the drain region decreases from 1×10^6 V/cm for DG LDMOS to 0.5×10^6 V/cm for C-LDMOS due to the absence of the oxide trench. Therefore, the half-cell pitch of C-LDMOS needs to be lengthened from 9.5 μm for DG LDMOS and PG LDMOS to 19 μm in order to obtain the comparable BV. The smaller cell pitch helps to reduce $R_{on,sp}$. Furthermore, the BV of DG LDMOS is nearly the same as that of PG LDMOS, although the trench gate is placed in the oxide trench (the surface field strength in the trench gate is zero). This can be explained by the fact that the electric field distribution in the oxide trench is modulated by the trench gate. Especially under the trench gate as illustrated by Fig. 5(b), the field strength is much higher than that of PG LDMOS.

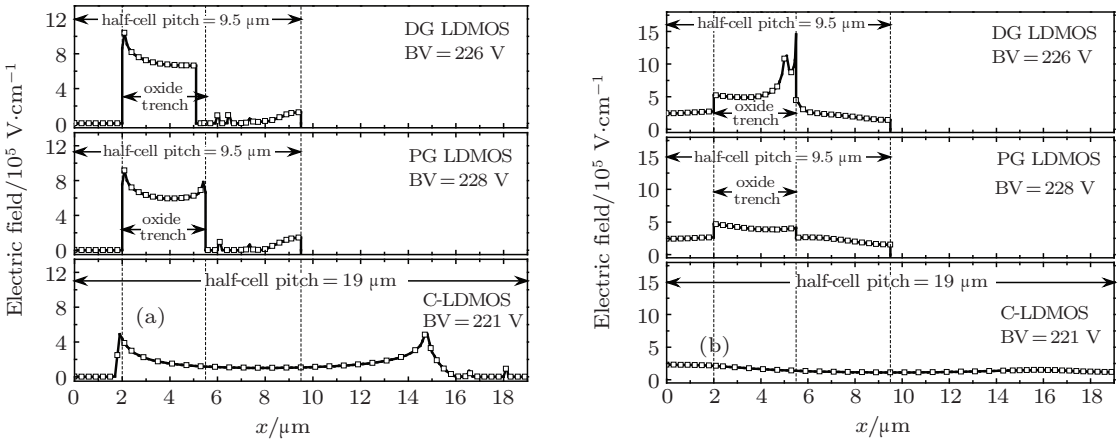


Fig. 5. Field distributions along (a) surface and (b) AA' line in Fig. 1. The structure parameters are the same as those in Fig. 3.

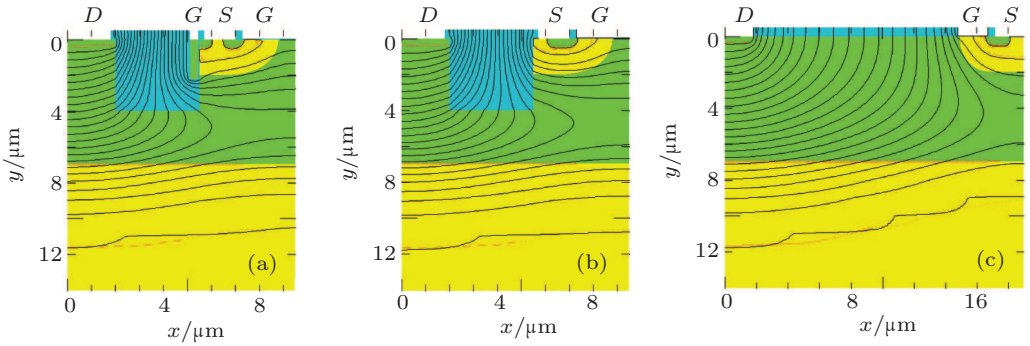


Fig. 6. Equipotential contours at breakdown voltage for (a) DG LDMOS (226 V), (b) PG LDMOS (228 V), and (c) C-LDMOS (221 V). The same structure parameters are used as those in Fig. 3. 10 V/contour.

Figure 6 shows the equipotential contours for DG LDMOS, PG LDMOS, and C-LDMOS. Comparing Figs. 6(a)–6(c), the enhancement and modulation effects for the oxide trench and trench gate on the field distribution can be observed, respectively. It is clearly obtained from Figs. 6(a) and 6(b) that the voltage drop from the drain to the source in the drift region is equal to that in the oxide trench, implying that the drift region is folded by the oxide trench in the vertical direction. The effective drift region length is thus increased by the oxide trench. So in order to achieve the equivalent BV, the half-cell pitch of C-LDMOS increases from 9.5 μm for DG LDMOS and PG LDMOS up to 19 μm. The values of $R_{on,sp}$ are thus reduced for DG LDMOS and PG LDMOS. Comparing Fig. 6(a) with Fig. 6(b), it can be seen that the BV is barely affected by the trench gate.

Figure 7 illustrates the electric field distribution along AB line in Fig. 1 under breakdown condition. In the OFF-state, the electric field peaks Q and Q' are generated at the n+/n- junction and the n-/p-sub junction, respectively. Owing to the oxide trench, new electric field peaks P_1, P_2, and P_3 are generated at B point in Fig. 1. The new field peak enhances the electric field of the drift region. When the oxide trench is shallow ($t_T = 3$ μm in Fig. 7), the average electric field is small in region II. However, the oxide trench cannot be too deep ($t_T = 6$ μm in Fig. 7), otherwise the average electric field of region I will be lowered. As a result, the new field peak P_2 will lead to a uniform electric field distribution in the drift region. This indicates that the maximum of BV will be obtained at $t_T = 4$ μm.

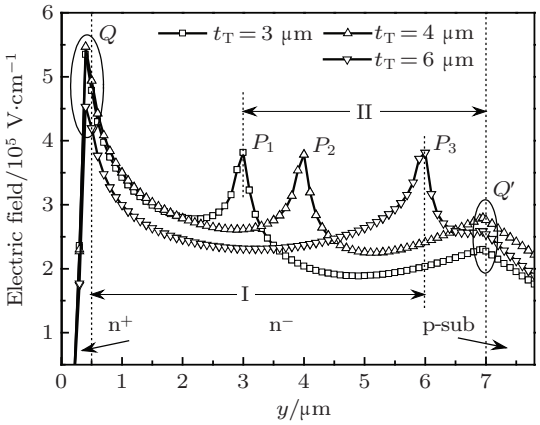


Fig. 7. Electric field distributions along AB line ($x = 2$ μm) in Fig. 1. ($w_T = 3.5$ μm, $t_S = 7$ μm, half-cell pitch = 9.5 μm, $P_{sub} = 3.5 \times 10^{15}$ cm^{-3}. N_d is optimized to obtain the maximum BV for each t_T.)

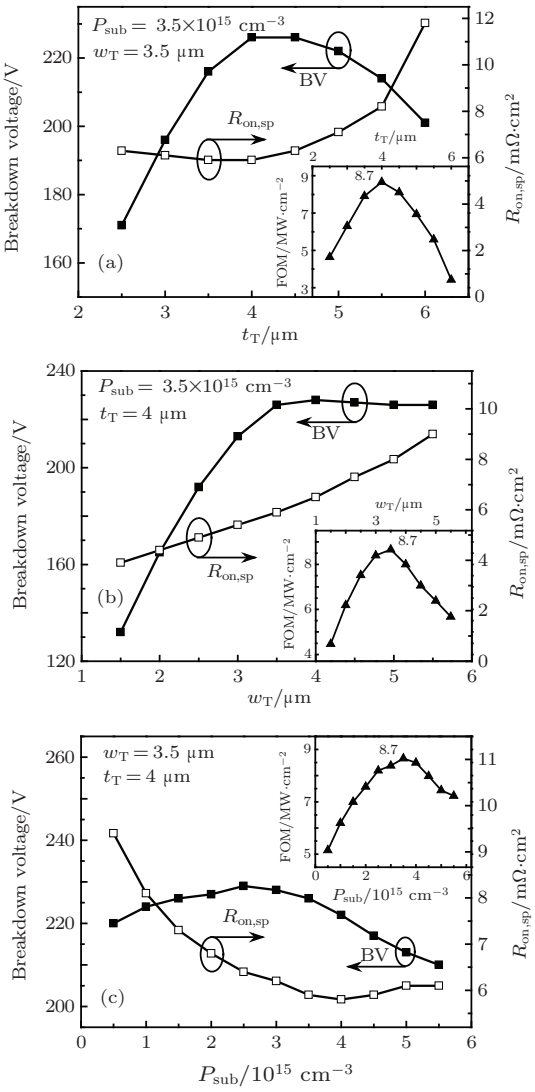


Fig. 8. Dependences of BV, $R_{on,sp}$, and FOM on t_T, w_T, and P_{sub} for DG LDMOS. (a) t_T (w_T = 3.5 μm, P_{sub} = 3.5×10^{15} cm^{-3}), (b) w_T (t_T = 4 μm, P_{sub} = 3.5×10^{15} cm^{-3}), and (c) P_{sub} (t_T = 4 μm, w_T = 3.5 μm). (t_S = 7 μm and half-cell pitch = 9.5 μm for panels (a)–(c).)

The reduced $R_{on,sp}$ results in a far higher figure-of-merit (FOM) (FOM=BV^2/$R_{on,sp}$ in this paper)[18] value for DG LDMOS. Figure 8 shows the influences of t_T, w_T, and P_{sub} on BV, $R_{on,sp}$, and FOM. Owing to the electric field distributions shown in Fig. 7, BV first increases from 171 V to 226 V with t_T increasing from 2.5 μm to 4 μm. After that, as shown in Fig. 8(a), BV decreases to 201 V with t_T further increasing. Due to the narrow conduction path in the drift region under the oxide trench, the $R_{on,sp}$ of DG LDMOS increases from 5.9 mΩ·cm^2 to 11.8 mΩ·cm^2 with t_T increasing. In Fig. 8(b), the increasing of w_T results in an increased BV and $R_{on,sp}$. Moreover, the BV is saturated when $w_T > 3.5$ μm because it is limited by the vertical BV. The simulation results indicate that the vertical electric field distribution and the optimal N_d are influenced by P_{sub}. So as shown in Fig. 8(c), the BV and $R_{on,sp}$ are affected by P_{sub}. As illustrated in the insets of Figs. 8(a)–8(c), the optimal FOM of 8.7 MW/cm^2 is extracted at t_T = 4 μm, w_T = 3.5 μm, and P_{sub} = 3.5×10^{15} cm^{-3}.

Table 1 summarizes the optimal results for these structures. The half-cell pitches of DG LDMOS and PG LDMOS are reduced by 50% at the equivalent BV compared with that of C-LDMOS due to the oxide trench. Moreover, the optimal N_d for C-LDMOS is approximately half of those for DG LDMOS and PG LDMOS. The smaller half-cell pitch and higher N_d both lead to that the $R_{on,sp}$ of PG LDMOS is reduced by 37% compared with that of C-LDMOS. As for DG LDMOS, the further reduced $R_{on,sp}$ of 5.9 mΩ·cm^2 is obtained due to the dual-gate, while that of C-LDMOS is 17.8 mΩ·cm^2. As a result, the FOM of DG LDMOS is the highest in Table 1.

Table 1. Optimal results for each device.

Device parameters	DG LDMOS	PG LDMOS	C-LDMOS
Half-cell pitch/μm	9.5	9.5	19
Thickness of n-type silicon layer, t_S/μm	7	7	7
Width of the oxide trench, w_T/μm	3.5	3.5	–
Depth of the oxide trench, t_T/μm	4	4	–
Doping concentration of n-type silicon layer, N_d/10^{15} cm^{-3}	4.5	4.3	2.1
Doping concentration of p-type substrate, P_{sub}/10^{15} cm^{-3}	3.5	3.5	3.5
Breakdown voltage, BV/V	226	228	221
Specific on-resistance, $R_{on,sp}$/mΩ·cm^2	5.9	11.3	17.8
Figure-of-merit, FOM/MW·cm^{-2}	8.7	4.6	2.7

4. Conclusion

A novel high voltage trench LDMOS with dual-gate structure is proposed and investigated by simulation. The dual gate provides dual conduction channel for reducing $R_{on,sp}$. The oxide trench lengthens the effective drift region in order to shorten the cell pitch at the comparable BV. The dual conduction channel and the shortened cell pitch both result in a dramatically reduced $R_{on,sp}$. The half-cell pitch and $R_{on,sp}$ are reduced by 50% and 67% for DG LDMOS, respectively, compared with those for C-LDMOS at the equivalent BV.

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