Hot carrier degradation and a new lifetime prediction model in ultra-deep sub-micron pMOSFET*

Lei Xiao-Yi(雷晓艺)[a)†], Liu Hong-Xia(刘红侠)[a)], Zhang Kai(张 凯)[a)], Zhang Yue(张 月)[a)], Zheng Xue-Feng(郑雪峰)[a)], Ma Xiao-Hua(马晓华)[a)b)], and Hao Yue(郝 跃)[a)]

[a)] *Key Laboratory of Wide Bandgap Semiconductor Materials and Devices of Ministry of Education, State Key Discipline Laboratory of Wide Bandgap Semiconductor Technologies, School of Microelectronics, Xidian University, Xi'an* 710071, *China*

[b)] *School of Technical Physics, Xidian University, Xi'an* 710071, *China*

(Received 12 September 2012; revised manuscript received 22 October 2012)

The hot carrier effect (HCE) of an ultra-deep sub-micron p-channel metal–oxide semiconductor field-effect transistor (pMOSFET) is investigated in this paper. Experiments indicate that the generation of positively charged interface states is the predominant mechanism in the case of the ultra-deep sub-micron pMOSFET. The relation of the pMOSFET hot carrier degradation to stress time (t), channel width (W), channel length (L), and stress voltage (V_d) is then discussed. Based on the relation, a lifetime prediction model is proposed, which can predict the lifetime of the ultra-deep sub-micron pMOSFET accurately and reflect the influence of the factors on hot carrier degradation directly.

Keywords: pMOSFETs, hot carrier effect (HCE), degradation, lifetime modeling

PACS: 73.40.Qv, 85.30.Tv **DOI:** 10.1088/1674-1056/22/4/047304

1. Introduction

As the device dimensions are continuously shrunk, the hot carrier effect (HCE) is becoming more and more serious, and has long been one of the most important reliability issues for metal–oxide semiconductor field-effect transistor (MOSFET) devices.[1–4] Most of the research about HCE concentrates on n-channel MOSFETs (nMOSFETs) rather than p-channel MOSFETs (PMOSFETs), because hot-carrier-induced problems are more serious in nMOSFETs due to the longer mean-free path, hence higher energy of electrons. However, when the devices enter into ultra-deep sub-micron range, the aggressive scaling of the feature size and reduction of supply voltages have rendered HCE induced performance degradation of a pMOSFET comparable to that of an nMOSFET.[5] Therefore, an investigation of the HCE degradation and a model to extrapolate the lifetime in pMOSFETs are especially necessary.

Several HCE degradation models of pMOSFETs have been proposed to predict the lifetimes of long channel devices and their results coincided well with experimental data.[2,6,7] However, these models lack precision in predicting the lifetime of the ultra-deep sub-micron device and cannot give a direct relation between the various factors and the hot carrier degradation.

In this paper, the hot carrier degradations of pMOSFETs with different sizes are investigated under different stress conditions. By analyzing the influence factors of the HCE, we propose a new lifetime model to predict lifetime about HCE degradation for ultra-deep sub-micron device technology.

2. Devices and experiments

To study HCE degradation of devices, pMOSFETs with gate lengths varying from 90 nm to 0.16 μm and gate widths changing from 2 μm to 20 μm were tested. Gate oxide thickness for each of the devices with the decoupled plasma nitridation (DPN) process was 1.4 nm. The devices used here were of surface channel. They were fabricated using a 90-nm process technology with lightly doped drain (LDD) structure and shallow trench isolation (STI) scheme. A Keithley 4200SCS, a high precision semiconductor parameter analyzer, was used to characterize the performances of devices. The experiments were conducted at room temperature. Figure 1 shows the schematic plot of hot carrier stress. In the experiments, the gate and drain voltage stresses $V_{gstress} = V_{dstress} = -2.0$ V/-1.8 V/-1.2 V were applied to the devices and other terminals were grounded. In all cases, the stress was briefly interrupted to measure its effect on device characteristics. Based on the analysis of the change in electrical characteristic of device, the degradations of the threshold voltage (V_{th}), the maximal transconductance (G_{mmax}), the drain linear current (I_{dlin}) and the drain saturation current (I_{dsat}) were obtained.

*Project supported by the National Basic Research Program of China (Grant No. 2011CBA00606), the National Natural Science Foundation of China (Grant No. 61106106), and the Fundamental Research Funds for the Central Universities, China (Grant No. K50510250006).

†Corresponding author. E-mail: lydialeixy@163.com

© 2013 Chinese Physical Society and IOP Publishing Ltd

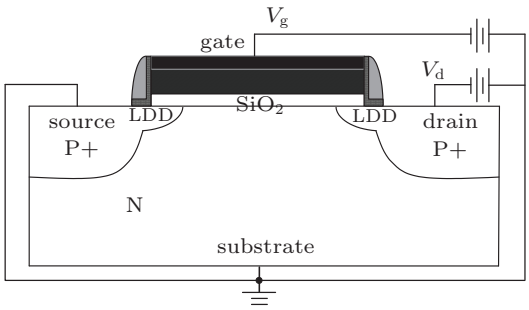


Fig. 1. Schematic plot of hot carrier stress.

3. Results and discussion

Figures 2(a) and 2(b) show the transfer characteristic degradations of pMOSFETs at $V_d = -0.05$ V and $V_d = -1$ V under hot carrier stress, respectively. The degradations of G_{mmax}, I_{dlin}, and I_{dsat} degradations are observed. In addition, the peak transconductance shifts to more negative V_g. Therefore, the V_{th} extracted from the I_{dlin} by the G_{mmax} method is more negative with the increase of stress time, indicating a positive charge build-up in the gate dielectric.

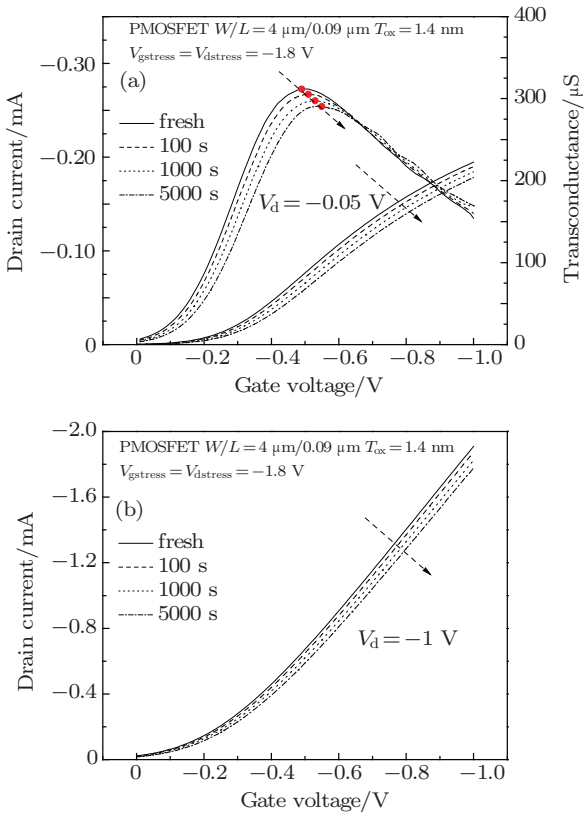


Fig. 2. Transfer characteristics degradations under hot carrier stress at (a) $V_d = -0.05$ V and (b) $V_d = -1$ V.

The positive charge can result either from hole trapping in the dielectric or from the creation of positively charged interface states at the dielectric interface. We believe that the interface state generation is predominant, as the electric field near the drain does not favor the hole injection in the dielectric in the case of $V_g = V_d$.[8] Furthermore, as shown in Fig. 3, under hot carrier stress condition, normalized degradations of device parameters (V_{th}, G_{mmax}, I_{dlin}, and I_{dsat}) can be approximately expressed by a power-law function of time as

$$\Delta V_{th}\%(G_{mmax}\%, I_{dlin}\%, I_{dsat}\%) \propto t^n, \quad (1)$$

which is consistent with the interface state generation model.[9] The power-law slope n is in a range of 0.25∼0.27. Since the degradation of V_{th} is much higher than those of G_{mmax}, I_{dlin}, and I_{dsat}, we take V_{th} degradation to analyze the hot carrier degradation in this paper.

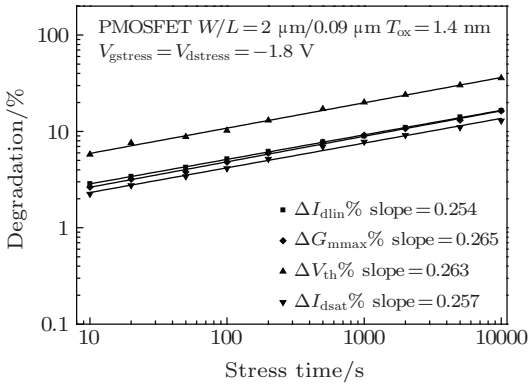


Fig. 3. Normalized degradations of device parameters under the stress condition of $V_{gstress} = V_{dstress} = -1.8$ V.

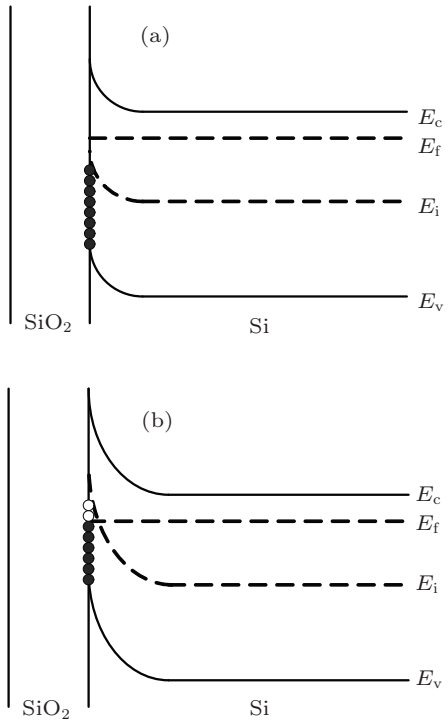


Fig. 4. Energy-band diagrams and donor-type interface traps for pMOSFETs in the conditions of (a) depletion and (b) inversion.

Here, we use energy-band diagrams to explain the interface trap effect on device characteristics as depicted in Fig. 4. When a pMOSFET is biased in the depletion condition, the band edge bends upward near the surface and the intrinsic

level (E_i) is closer to the Fermi level (E_f) as shown in Fig. 4(a). The donor-type interface traps are full of electrons and become neutral. When in the inversion condition, the bands bend even more upward and the E_i at the surface passes over the E_f. The donor-type interface traps between the E_f and the E_i are empty and positively charged as shown in Fig. 4(b). From the above, it is concluded that the generation of interface traps causes the effective gate voltage to decrease and the mobility to degrade, therefore negative V_{th} to shift and G_{mmax}, I_{dlin}, and I_{dsat} to decrease.

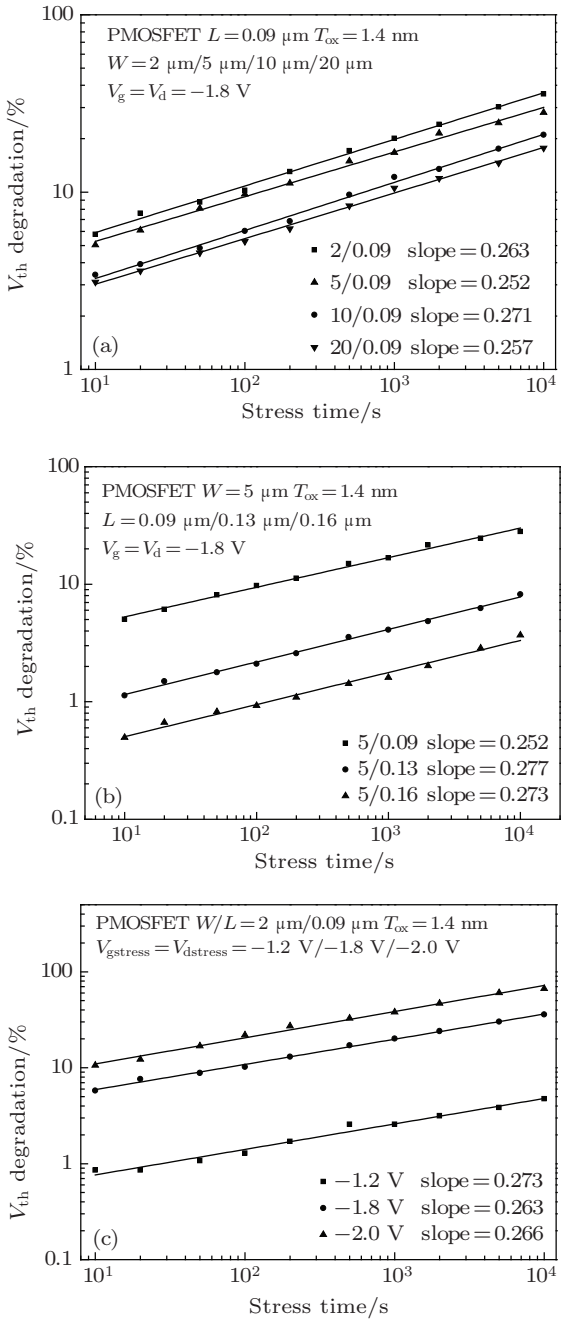


Fig. 5. Plots of V_{th} normalized degradation versus stress time (a) with different channel widths, (b) channel lengths, and (c) under different stress voltages.

Figure 5 shows the plots of V_{th} degradation versus stress time with different channel widths, channel lengths, and under different stress voltages. All data are plotted in a log–log scale. As can be observed, the shifts of V_{th} show excellent accordance with t^n in all curves. Figure 5(a) indicates the degradation of the V_{th} is more serious as the channel width decreases. The same study was done for different channel lengths (see Fig. 5(b)) and the shorter channel length is observed to be more degraded. In Fig. 5(c), the degradation augments as stress voltage increases.

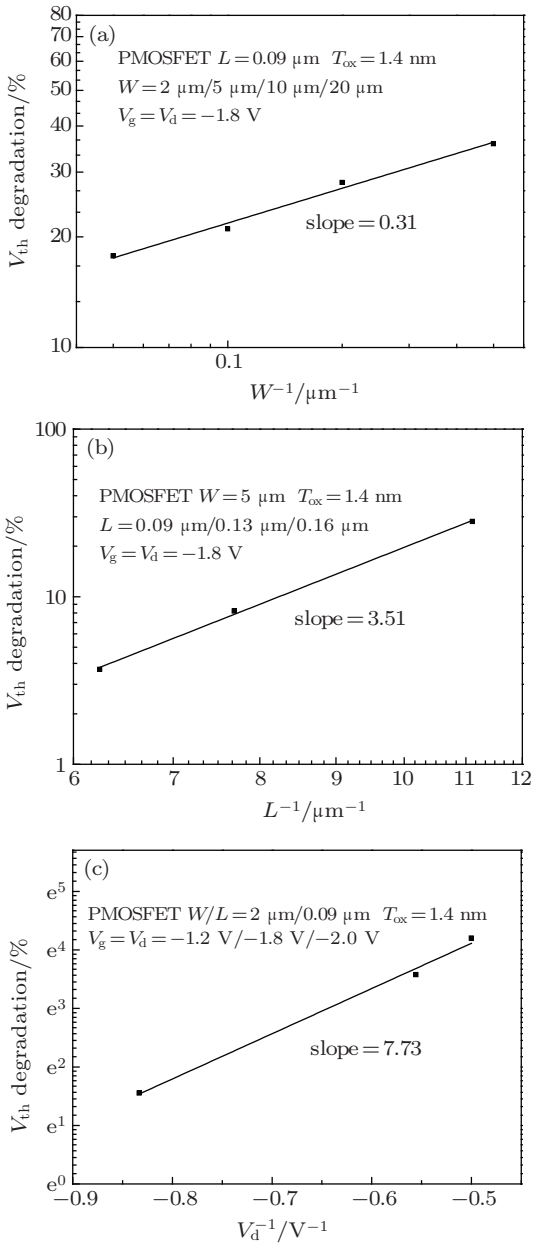


Fig. 6. Dependences of V_{th} degradation on (a) channel width, (b) channel length, and (c) stress voltage.

Figures 6(a)–6(c) show the dependences of V_{th} degradation induced by hot carrier stress after 10^5 s on channel width, channel length, and stress voltage, respectively. In Figs. 6(a) and 6(b) we plot the data in a log–log scale, and obtain the power-law relationships between the V_{th} degradation and $1/W$

and $1/L$ as follows:

$$\Delta V_{\rm th}\% \propto (1/W)^a, \tag{2}$$

$$\Delta V_{\rm th}\% \propto (1/L)^b. \tag{3}$$

The parameter a in expression (2) is extracted from the power-law slope and approximately equal to 0.31. The parameter b in expression (3) is extracted in the same way as the above, and has a value of 3.51. A much larger value of b than that of a indicates that the channel length has a more critical effect on hot carrier degradation. The shift of $V_{\rm th}$ versus the reciprocal of stress voltage $1/V_{\rm d}$ is plotted in Fig. 6(c) with a ln–linear scale, and all data under different stresses are fitted with

$$\Delta V_{\rm th}\% \propto \exp(c/V_{\rm d}). \tag{4}$$

The parameter c extracted from the data of Fig. 6(c) is 7.73.

Hence, according to expressions (1)–(4), we can obtain the $V_{\rm th}$ degradation model, including various factors affecting hot carrier effects, which is expressed as

$$\Delta V_{\rm th}\% = {\rm C}t^n(1/W)^a(1/L)^b\exp(c/V_{\rm d}), \tag{5}$$

where C is a constant related to specific technology, which can be extracted from the experiment data.

For an electronic device, the "lifetime" refers to life expectancy, the length of time a device is expected to remain workable, i.e., the length of time an important device parameter degrades to a point where the device can no longer function properly in its intended application. Hence, by defining $\Delta V_{\rm th}\%$ reaching some value P as the end of device life, the lifetime τ can be expressed as

$$\tau = P/[C(1/W)^a(1/L)^b\exp(c/V_{\rm d})]^{1/n}. \tag{6}$$

We take the 10% shift of $V_{\rm th}$ as the lifetime definition conventionally. As shown in Fig. 7, the good agreement between experimental data and modeling value demonstrates the validity of the proposed model in predicting device lifetime limited by the hot carrier effect.

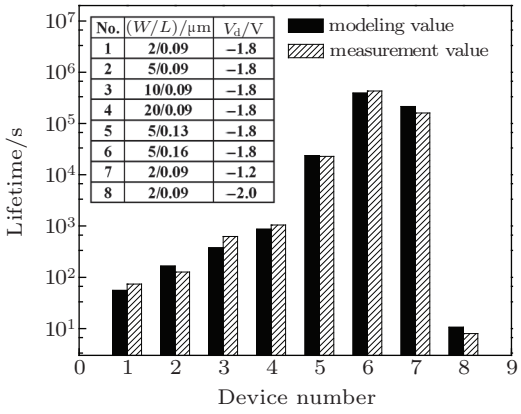


Fig. 7. Comparison between measurement values and modeling values.

4. Conclusion

We examined the hot carrier degradations of ultra-deep sub-micron pMOSFETs with different sizes under different stress conditions and propose a new model on the HCE-related device lifetime prediction. The generation of positively charged interface states at the dielectric interface is identified to be the predominant degradation mechanism in ultra-deep sub-micron pMOSFETs. The relation of $V_{\rm th}$ degradation to t, $1/W$, $1/L$, and $1/V_{\rm d}$ is derived respectively by the experimental data. Finally, the HCE degradation model dependent on t, W, L, and $V_{\rm d}$ is obtained, which could be used to predict the HCE-related device lifetime with great precision.

References

[1] Tu R H, Rosenbaum E, Chan W Y, Li C C, Minami E, Quader K, Ko P K and Hu C 1993 *IEEE Trans. Comput. Aided Des. Integrate Circuits & Syst.* **12** 1524
[2] Hu C, Tam S C, Hsu F C, Ko P K, Chan T Y and Terrill K W 1985 *IEEE Trans. Electron. Dev.* **32** 375
[3] Ma X H, Wang J P, Cao Y R and Chen H F 2006 *Chin. Phys.* **15** 2742
[4] Ma X H, Cao Y R, Hao Y and Zhang Y 2011 *Chin. Phys. B* **20** 037305
[5] Liu H X, Hao Y, Hawkins I D and Peaker A R 2005 *Chin. Phys.* **14** 1644
[6] Huang D H and King E E 1994 32*nd IEEE Int. Reliability Phys. Symp.* April 11–14, 1994, San Jose, CA, USA, p. 34
[7] Zhang J C, Hao Y and Zhu Z Y 2001 *Chin. J. Semicond.* **22** 1586
[8] Polishchuk I, Yeo Y C, Lu Q, King T J and Hu C 2001 39*th IEEE Int. Reliability Phys. Symp.* April 30–May 3, 2001 Orlando, FL, USA, p. 425
[9] Woltjer R, Paulzen G M, Pomp H G, Lifka H and Woerlee P H 1995 *IEEE Trans. Electron. Dev.* **42** 109