Determination of interface states and their time constant for Au/SnO_2/n-Si (MOS) capacitors using admittance measurements

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The frequency dependence of admittance measurements (capacitance–voltage (C–V) and conductance–voltage (G/ω–V)) of Au/SnO_2/n-Si (MOS) capacitors was investigated by taking into account the effects of the interface states (N_{ss}) and series resistance (R_s) at room temperature. Admittance measurements were carried out in frequency and bias voltage ranges of 1 kHz–1 MHz and (−5 V)–(+9 V), respectively. The values of N_{ss} and R_s were determined by using a conductance method and estimating from the admittance measurements of the MOS capacitors. At low frequencies, the interface states can follow the AC signal and yield excess capacitance and conductance. In addition, the parallel conductance (G_p/ω) versus $\log(f)$ curves at various voltages include a peak due to the presence of interface states. It is observed that the N_{ss} and their time constant (τ) range from 1.23×10^{12} $eV^{-1}\cdot cm^{-2}$ to 1.47×10^{12} $eV^{-1}\cdot cm^{-2}$ and from 7.29×10^{-5} s to 1.81×10^{-5} s, respectively.

Keywords: MOS capacitor, admittance measurements, interface states

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1. Introduction

Metal–oxide–semiconductor (MOS) capacitors or structures are important devices in solid-state electronics. The MOS structures constitute a kind of capacitor, which stores the electric charge by virtue of the dielectric property of oxide layers.[1–3] Due to the presence of an oxide layer and two surface-charge regions, MOS physics is more complicated than semiconductor physics. A real MOS structure always contains "oxide charges" located in the bulk of the oxide or at the oxide–silicon interface. In general, several possible sources of error that cause deviations from ideal MOS behavior, such as electrical properties, must be taken into account. Since the interface states (N_{ss}) exist at the semiconductor–insulator interface, the device behavior is different from an ideal case due to the presence of these localized interface states and their relaxation time (τ). Due to the high density of N_{ss} in these devices, characterization and extraction of N_{ss} are extremely important in assessing the quality of dielectric–semiconductor interfaces. The electrical characteristics of these structures are also influenced by the series resistance (R_s), the thickness of interfacial oxide layer, its homogeneity, and the shape of barrier height at M/S interface.

Several suggested methods[4–8] could help to determine N_{ss} and R_s, and among them the most important is the conductance technique developed by Nicollian and Goetzberger.[9] A conductance method is considered to be the most suitable method for determining N_{ss} values as low as 10^9 $eV^{-1}\cdot cm^{-2}$. In addition, the series resistance is an important parameter, which causes changes in the electrical characteristics for MOS structures.[3,10–13]

The purpose of this paper is determination of the N_{ss} and τ in Au/SnO_2/n-Si (MOS) capacitors. The N_{ss} and τ were obtained from measured forward bias admittance measurements. In addition, the effects of N_{ss} and R_s on the capacitance–voltage (C–V) and conductance–voltage (G/ω–V) characteristics have been investigated. The N_{ss} value is determined by using a conductance method. The C–V and G/ω–V measurement were carried out in the wide frequency range of 1 kHz–1 MHz at room temperature.

2. Experimental detail

The MOS (Au/SnO_2/n-Si) capacitors used in this work were fabricated using n-type (P-doped) single crystal silicon wafers with ⟨111⟩ surface orientation, 280-μm thickness, 5.08-cm diameter, and 1-Ω·cm–5-Ω·cm resistivity. The silicon wafer was degreased for 5 min in boiling trichloroethylene, acetone, and ethanol consecutively and then etched: first in H_2SO_4, H_2O_2, and 20% HF solution, then in 6HNO_3: 1 HF: 35-H_2O and 20%-HF solution for 4 min. After each cleaning step, the wafer was rinsed thoroughly in de-ionized water of 18-MΩ·cm resistivity. In order to remove any native thin oxide layer on the Si surface, the samples were dipped in HF:H_2O (1:10) for about 20 s and finally the wafers were rinsed in de-ionized water for 10 min using an ultrasonic bath. After surface cleaning, high purity Au metal (99.999%) with thickness of 2000 Å (1 Å = 0.1 nm) was thermally evaporated from the tungsten filament onto the whole back surface of the wafer in a liquid nitrogen trapped oil-free ultra-high vacuum system at the pressure of $\sim 1\times10^{-6}$ Torr (1 Torr = 1.33322×10^2 Pa). In order to form low-resistivity Ohmic contact, the Au-coated

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n-Si wafer was annealed at about 500 °C for 5 min in flowing dry nitrogen (N_2) in a quartz tube furnace. Immediately after the formation of Ohmic contact, a thin layer of SnO_2 was grown on the Si substrate by spraying a solution consisting of 32.21 wt% of ethyl alcohol (C_2H_5OH), 40.35 wt% of de-ionized water (H_2O), and 27.44 wt% of stannic chloride ($SnCl_4.5H_2O$), which was maintained at a constant temperature of 400 °C. The temperature of the substrates was monitored by a chromel–alumel thermocouple fixed on the top surface of the substrate. The variation of the substrate temperature during spraying was maintained within ±2 °C with the help of a temperature controller. The rate of spraying was kept at about 30 cc/min by controlling the carrier gas flowmeter. N_2 was used as the carrier gas. After the spraying process, circular dots of 2 mm in diameter Au rectifying contacts with 1500-Å thickness were deposited onto the SnO_2 surface of the Si wafer through a metal shadow mask in liquid nitrogen trapped oil-free ultra-high vacuum system in the pressure of $\sim 1 \times 10^{-6}$ Torr. Both the thickness of the metal layer and deposition rates were monitored with the help of a digital quartz crystal thickness monitor. The deposition rates were about 1 Å/s–3 Å/s. The wafer was mounted on a copper holder with the help of silver paste and the electrical contacts were made to the upper electrodes by the use of tiny silver coated wires with silver paste. The interfacial oxide layer thickness was estimated to be about 500 Å from measurement of the oxide capacitance in the strong accumulation region for MOS capacitor.

The capacitance–voltage (C–V) and conductance–voltage (G/ω–V) measurements were carried out by using an HP 4192A LF impedance analyzer (5 Hz–13 MHz) in the frequency range of 1 kHz–1 MHz at room temperature. A low-distortion oscillator generated the AC signal with the amplitude attenuated to 50 mV_{rms} to meet the small signal requirement for oxide capacitors. All measurements were carried out with the help of a microcomputer through an IEEE-488 AC/DC converter card.

3. Results and discussion

The conductance technique[1,3,9,14] is based on the conductance losses resulting from the exchange of majority carriers between the interface states and majority carrier band of the semiconductor when a small AC signal is applied to the metal–insulator/oxide–semiconductor (MIS/MOS) structures. This method requires a lot of C–V and G/ω–V plots for various frequencies in the wide range of applied bias voltage. In Nicollian and Goetzberger's statistical theory,[9,14] the random distribution of discrete oxide charges and charged interface states in the semiconductor/oxide (Si/SnO_2) interface plane cause a non-uniform distribution of surface band bending over the interfacial plane.

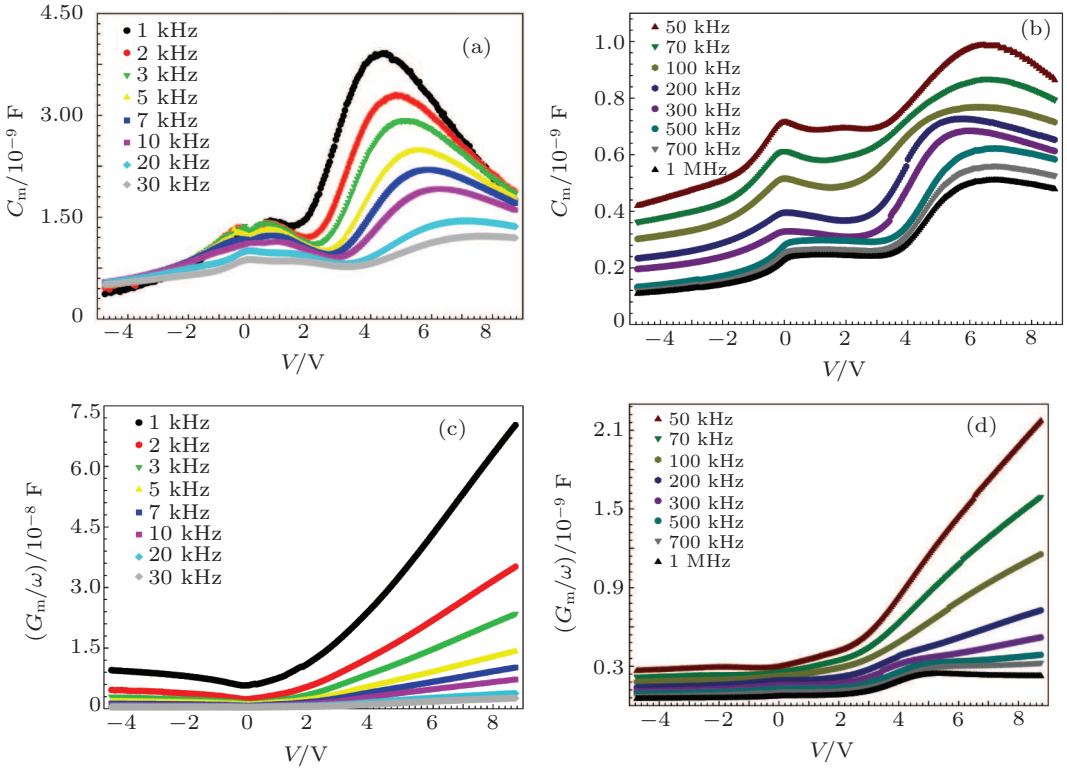


Fig. 1. (color online) Measured (a) C–V and (b) G/ω–V characteristics of $Au/SnO_2/n$-Si (MOS) capacitor for various frequencies.

Figures 1(a) and 1(b) show the measured C–V and G/ω–V characteristics of Au/SnO_2/n-Si (MOS) capacitor for various frequencies and room temperatures, respectively. The applied voltage bias was changed between −5 V and +9 V. The three regimes of accumulation, depletion, and inversion are clearly shown for each frequency, verifying a typical MOS behavior. As can be seen in Fig. 1(a), the C–V plot shows two peaks for each frequency at the depletion and accumulation regions. The first peak at the depletion region was attributed to the existence of N_{ss} at Si/SnO_2 interfaces. On the other hand, the second peak at the accumulation region is attributed to the series resistance of the MOS capacitor.

It is shown that there is significantly larger frequency dispersion in C–V and G/ω–V curves, indicating the existence of interface states which are in thermal equilibrium with the semiconductor and cannot communicate with the metal. It is especially noteworthy that at lower frequencies, the change in C–V and G/ω–V becomes more important and they increase with decreasing frequency. This is evidence of the presence of a continuous distribution of the interface states with different lifetimes. If the C–V or G/ω–V measurements are carried out at sufficiently high frequency such that carrier lifetime (τ) is much larger than $1/2\pi$f, the interface states cannot follow an AC signal.[1,3,15,16] In addition, the values of capacitance and conductance of the MOS capacitor at the strong accumulation region increase with applied bias voltage. Note especially that such behavior of C–V or G/ω–V at the strong accumulation region depends on the series resistance of the MOS capacitor and interfacial oxide layer.

There are several methods to extract the values of series resistance of MOS structures in the literature.[1,17–19] We have applied the method of Nicollian and Goetzberger.[9,14] The real series resistance of a MOS structure can be subtracted from the measured capacitance (C_{ma}) and conductance (G_{ma}) in the strong accumulation region at sufficiently high frequency ($\geq$ 500 kHz). The measured admittance (Y_{ma}) at the strong accumulation region of MOS structures using the parallel RC circuit[1,3,19] is equivalent to the total circuit admittance as:

$$Y_{ma} = 1/Z_{ma} = G_{ma} + j\omega C_{ma}. \quad (1)$$

Comparing the real and imaginary parts of the admittance, the series resistance (R_s) is given by[3,14,17,20,21]

$$R_s = \frac{G_{ma}}{G_{ma}^2 + (\omega C_{ma})^2}, \quad (2)$$

where C_{ma} and G_{ma} represent the measured capacitance and conductance in the strong accumulation region, respectively, and ω is the angular frequency. The real value of R_s of the MOS capacitor was calculated according to Eq. (2) in the strong accumulation region at high frequency. However, the voltage-dependent value of R_s was also calculated according to Eq. (2) for various frequencies and shown in Fig. 2. As can be clearly seen in Fig. 2, the R_s–V plots include a peak. The magnitude of peaks decreases with increasing frequency. Such behavior of R_s is attributed to the particular distribution of N_{ss} localized at Si/SnO_2 interface states and the interfacial oxide layer at Au/n-Si interface. Also, in the depletion and inversion regions, the values of R_s increase while in the accumulation region R_s remains almost constant.[1,9,22–24] These very significant values demand that special attention be given to effects of the series resistance in the application of the admittance–based measuring methods (C–V and G/ω–V).

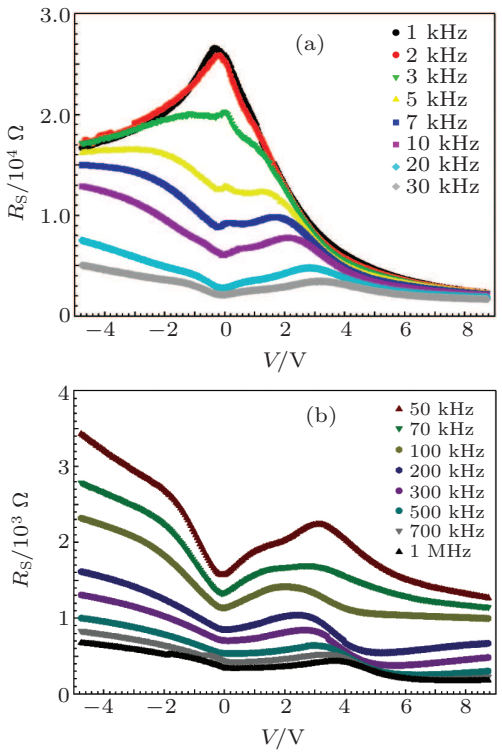


Fig. 2. (color online) Series resistance (R_s) versus gate bias (V) plots for various frequencies at room temperature.

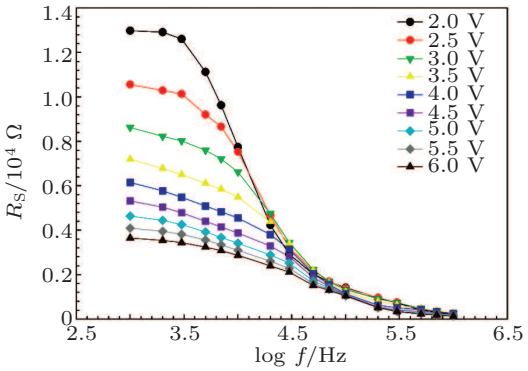


Fig. 3. (color online) The frequency dependence of the series resistance for different forward biases at room temperature.

In addition, the frequency dependence of R_s for different forward biases at room temperature is plotted in Fig. 3. As can be seen from Fig. 3, the values of R_s decrease with increasing frequency in the voltage range of 2 V–6 V, and are almost

independent of voltage at high frequencies. When the C–V or G/ω–V measurements are carried out at sufficiently high frequency, the carrier lifetime (τ) of interface states is much larger than $1/2\pi f$. In this case, the charge at traps cannot follow an AC signal.[1] On the other hand, at low frequencies the situation is different and the charges at traps can easily follow an AC signal and they lead to an increase in the capacitance and conductance values.

The conductance method is generally considered to be the most sensitive and useful method to determine N_{ss}, because it yields N_{ss} in the depletion and weak inversion portion of the band gap, the capture cross section for majority carriers, and information about surface potential fluctuations.[1] Subsequent measurement of the parallel conductance as a function of the frequency for certain DC biases in depletion, and suitable modeling provides the density of interface states. Admittance spectroscopy data were collected for the Au/SnO_2/n-Si (MOS) capacitor and analyzed via the conductance technique described by Nicollian and Brews[1] in order to calculate both the density of interface states and the time constant of the traps. It is well known that this method is the most accurate method to evaluate the density of interface states. In the method, the parallel conductance is measured as a function of frequency at a gate bias, and it is expressed as[1,3,9,12]

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau}\ln(1+\omega^2\tau^2), \tag{3}$$

where D_{it} is the density of the interface states, q is the charge of the electron, ω is the angular frequency, and τ_{it} is the time constant of the interface states. The measured capacitance and conductance are used to extract the equivalent parallel conductance (G_p) as given by[9,25–27]

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2(C_{ox}-C_m)^2}. \tag{4}$$

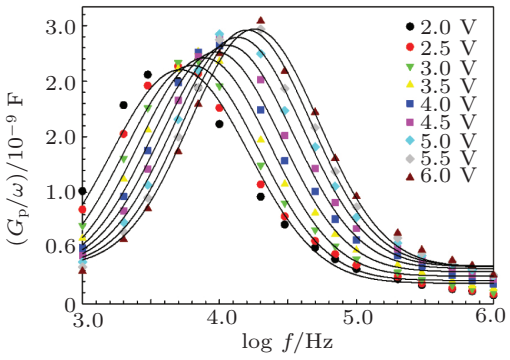


Fig. 4. (color online) The equivalent parallel conductance G_p/ω versus frequency at various gate biases for the MOS capacitor.

Figure 4 shows the plots of parallel conductance (G_p/ω) versus $\log f$ of the MOS capacitor at different voltages. As can be seen in Fig. 4, for each gate bias voltage the G_p/ω curve shows a peak and the peak position shifts toward higher frequencies with increasing applied bias voltage. This behavior can be explained by using the interface trap model. As indicated before, there exists an almost continuous distribution of interface states energy levels. Furthermore, this indicates that the traps are distributed inside the Si band gap. This peak exists because of interface charges at the interface of the silicon–oxide layer which contribute to the total charging current, and in turn a peak appears in the G_p/ω–$\log f$ plot.[23,25,27–30]

In addition, at this peak $[\partial(G_p/\omega)]/\partial(\omega\tau) = 0$ and this maximum condition gives $\omega\tau = 1.98$. Substituting this value in the above equation one gets $N_{ss} = (G_p/\omega)_{max}/(0.402qA)$ and interface state time constant $\tau = 1.98/\omega_p$, where ω_p is the frequency at which the G_p/ω peak occurs. The calculated values of the interface states (N_{ss}) and the time constant of interface states (τ) of the MOS capacitor are given in Table 1. As can be seen from Table 1, the values of N_{ss} increase while the τ decreases with the increasing bias voltage. The values of the N_{ss} and τ are changed from 1.23×10^{12} $eV^{-1}\cdot cm^{-2}$ to 1.47×10^{12} $eV^{-1}\cdot cm^{-2}$ and from 7.29×10^{-5} s to 1.81×10^{-5} s, respectively.

Table 1. The calculated value of the interface states (N_{ss}) and their time constant (τ) for an Au/SnO_2/n-Si (MOS) capacitor at room temperature.

V/V	$N_{ss}/10^{12}$ $eV^{-1}\cdot cm^{-2}$	$\tau/10^{-5}$ s
2.0	1.23	7.29
2.5	1.25	5.91
3.0	1.27	5.15
3.5	1.31	4.18
4.0	1.34	3.39
4.5	1.38	2.75
5.0	1.42	2.39
5.5	1.46	1.94
6.0	1.47	1.81

4. Conclusions

The interface states (N_{ss}) and the time constant (τ) of the interface states have been obtained from admittance measurements (capacitance–voltage (C–V) and conductance–voltage (G/ω–V)). The C–V and G/ω–V characteristics exhibit frequency dependence due to the presence of interface states in the SnO_2/Si interface and due to the series resistance (R_s) of the structure. The interface state density (N_{ss}) and corresponding time constant (τ) have been determined using the conductance method. The values of N_{ss} range from 1.23×10^{12} $eV^{-1}\cdot cm^{-2}$ to 1.47×10^{12} $eV^{-1}\cdot cm^{-2}$. In addition, the τ ranges from 7.29×10^{-5} s to 1.81×10^{-5} s.

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