The dual role of multiple-transistor charge sharing collection in single-event transients*

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As technologies scale down in size, multiple-transistors being affected by a single ion has become a universal phenomenon, and some new effects are present in single event transients (SETs) due to the charge sharing collection of the adjacent multiple-transistors. In this paper, not only the off-state p-channel metal–oxide semiconductor field-effect transistor (PMOS FET), but also the on-state PMOS is struck by a heavy-ion in the two-transistor inverter chain, due to the charge sharing collection and the electrical interaction. The SET induced by striking the off-state PMOS is efficiently mitigated by the pulse quenching effect, but the SET induced by striking the on-state PMOS becomes dominant. It is indicated in this study that in the advanced technologies, the SET will no longer just be induced by an ion striking the off-state transistor, and the SET sensitive region will no longer just surround the off-state transistor either, as it is in the older technologies. We also discuss this issue in a three-transistor inverter in depth, and the study illustrates that the three-transistor inverter is still a better replacement for spaceborne integrated circuit design in advanced technologies.

Keywords: multiple-transistor charge sharing collection, single event transient (SET), pulse quenching effect, radiation hardened by design (RHBD)

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1. Introduction

With technologies shrinking in scale, integrated circuits (ICs) present a large number of challenges for their usage in the space environment due to the growing susceptibility to soft errors.[1] The international technology roadmap for semiconductors (ITRS) also identified that soft error is a key reliability concern for advanced technologies.[2] One of the major sources that induce the soft errors is single event transients (SETs), which can be induced by an ion striking the sensitive region of an IC.

In advanced technologies, the decrease in minimum transistor-to-transistor space causes multiple-transistors to be affected by a single ion strike. Some new effects are present in SET due to the charge sharing collection of the adjacent transistors,[3–8] in which the well-known SET pulse quenching effects have been discovered and widely studied: the pulse quenching effect can significantly reduce SET pulse width ($W_{\rm SET}$) in ICs to reduce the soft errors. For example, in the same logic node, the charge sharing collection of the n-channel metal–oxide semiconductor field-effect transistor (NMOS FET) (or p-channel metal–oxide semiconductor field-effect transistor (PMOS FET)) is beneficial to reducing the p-hit (or n-hit) $W_{\rm SET}$ due to the increase in the rate of the charge restorability,[3,4] which is additionally explored for single-event upset (SEU) mitigation in dual interlocked storage cell (DICE) layout design.[5] In the adjacent logic nodes, when the output of the first node is connected to the input of the following inverting node, the charge sharing collection of the following node is also beneficial to reducing the propagated $W_{\rm SET}$,[6,7] which is also explored for SET mitigation in the layout design for some special logic cells.[8] In these radiation hardened by design (RHBD) techniques, the charge sharing collection is intentionally enhanced (in order to enhance the pulse quenching effects) to reduce the total soft errors.

However, when changing the input mode, the off-state transistor will become the on-state one, when a single ion strikes the on-state transistor even it cannot produce SET essentially. The charge sharing collection of the following off-state transistor can also induce an unwanted SET. This illustrates that the SET will no longer just be induced by striking the off-state transistor, and the SET sensitive region will no longer just surround the off-state transistor in the advanced technologies either. The charge sharing collection seems to play a dual role in SET mitigation. For instance, in the inverter chain, the increase in the charge sharing collection will be beneficial to reducing $W_{\rm SET}$ induced by striking the off-state transistor. But, when changing the input mode, the increase in the charge sharing collection will also be beneficial to increasing the unwanted $W_{\rm SET}$ induced by striking the on-state transistor.

In this paper, we will study this issue in a common two-transistor inverter chain in depth, and we will also discuss this issue in three-transistor inverter chain to provide a possible replacement in the RHBD ICs design.

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2. Simulation details

Due to the good look-inside capability, three-dimensional mixed-mode technology computer aided design (TCAD) simulation has been proven to be a useful means of investigating the mechanism of single event charge collection.[9–13] In the simulation, the SET will be produced and propagate in a nine-inverter chain, as shown in Fig. 1(a). The PMOSs in the second, third, fourth, and fifth inverters are modeled as three-dimensional numerical model (as shown in Fig. 1(b)), and the other transistors are modeled as circuit model. The third off-state PMOS or on-state PMOS (determined by the input voltage) will be affected by a single ion. After an ion strikes the third off-state PMOS (referred to as condition 1), the initial SET will appear at the struck node n3. And after an ion strikes the third on-state PMOS (referred to as condition 2), even the initial SET cannot be produced at the struck node n3, the fourth off-state PMOS can also collect the ion induced charges due to the charge sharing collection, so the initial SET can also be present at the following node n4.

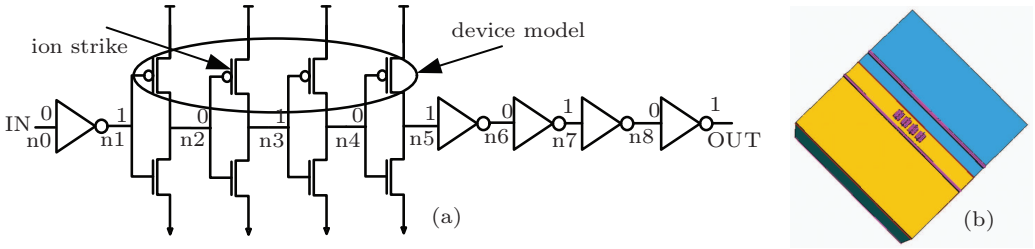


Fig. 1. (color online) Circuit used for SET production and propagation. (a) The circuit, (b) the device model.

Sentaurus TCAD vE-2010.12 from Synopsys is adopted in our work to perform the device simulation. The 60-nm bulk complementary metal–oxide semiconductor (CMOS) technology is used, and the doping profiles of the devices are calibrated by an inverse modeling approach. The width/length (W/L) ratio of NMOS is 200 nm/60 nm and the W/L ratio of PMOS is 500 nm/60 nm, N well contact distance from PMOS is 0.30 μm. Shallow trench isolation (STI) is used to isolate the adjacent PMOSs, the width of STI is 0.20 μm, and the depth of STI is 0.36 μm. The ion strikes through the device on a 10×10×10 substrate. In a way similar to that in Ref. [8], a backside substrate contact is used along the bottom surface of the substrate in series with a 1-kΩ resistor.

Heavy ion strike is simulated with an electron–hole pair column with the track serving as its axis. The linear energy transfers (LETs) of 10, 20, 30, 40, and 50 MeV·cm^2/mg are used, and the values are kept constant along the heavy ion track. The length and the radius of the ion track are 10 μm and 0.05 μm, respectively. Assume that the ion strikes at the center of the drain of the struck device normally.

The following physical models are used: (i) Fermi–Dirac statistics, (ii) band-gap narrowing effect, (iii) doping dependent Shockley–Read–Hall (SRH) recombination and Auger recombination, (iv) the effects of temperature, doping, electric field, carrier–carrier scattering and interface scattering on mobility, (v) hydrodynamic model is used for carrier transport. Unless otherwise specified, default models and parameters provided by Sentaurus TCAD vE-2010.12 are used.

3. Simulation results

SETs at the terminal of the chain are recorded and the pulse widths are calculated. As shown in Fig. 2, W_{SET} in condition 1 shows a parabolic shape and will decrease with LET increasing. W_{SET} in condition 2 will increase and will be larger than that in condition 1 as LET increases. When LET is 50 MeV·cm^2/mg, W_{SET} is 155.864 ps in condition 1, but it is 558.919 ps in condition 2, which is 403.055-ps larger than that in condition 1.

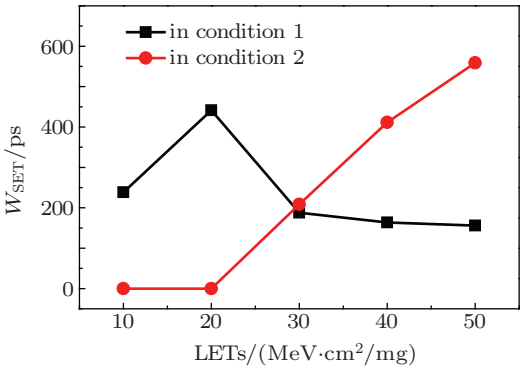


Fig. 2. (color online) Plots of W_{SET} versus LET (condition 1: striking the off-state PMOS; condition 2: striking the on-state PMOS).

SET pulse waveforms at the struck node n3, node n4, and the terminal are shown in Fig. 3 in condition 1 (LET = 50 MeV·cm^2/mg). After an ion strikes the third off-state PMOS, the initial SET is present at the struck node n3 because of the charge collection of the third off-state PMOS. However, when propagating through the next stage, the SET becomes very small at n4, so shorter SET will propagate

through the chain and appear at the terminal. When the initial SET appears at n3, the state of n3 will change from 0 to 1. On the one hand, the fourth off-state NMOS correspondingly becomes the on-state one, which will discharge the charges at n4 and try to change the state of n4 from 1 to 0; on the other hand, the fourth on-state PMOS also correspondingly becomes the off-state one, and the off-state PMOS can also collect the ion-induced charges due to the charge sharing collection to compensate for the charge at n4 to prevent the state of n4 from changing from 1 to 0. The competition between these two processes leads to a shorter SET appearing at n4, this effect has been found first by Ahlbin *et al.*[6] and is referred to as the well-known SET pulse quenching effect. In the older technologies, a single ion strike can only affect one transistor, the second process does not exist, so the initial SET at n3 can completely propagate through the chain. However, in the advanced technologies, when LET is large enough, the charge sharing collection of the following node will increase, the second process will also be enhanced and $W_{\rm SET}$ will become very small as shown in Fig. 3.

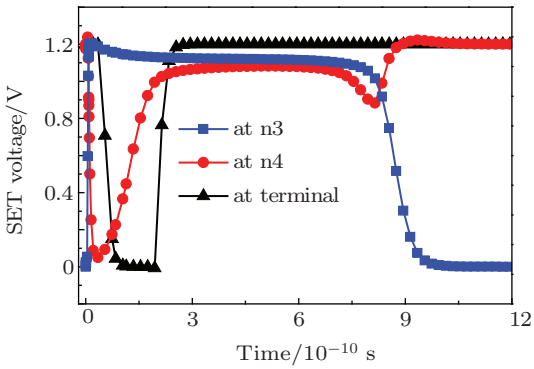


Fig. 3. (color online) SET pulse waveforms at the struck node n3, node n4, and the terminal of the chain in condition 1.

SET pulse waveforms at the struck node n3, node n4, and the terminal are shown in Fig. 4 in condition 2 (LET = 50 MeV·cm^2/mg). There is no SET at n3 because the charge collection of the third on-state PMOS cannot change the state of n3. However, because the charge sharing collection, the fourth adjacent off-state PMOS can also collect the ion induced charges, the SET will be present at n4 and the pulse will propagate through the chain. In the older technology, the single ion strike can only affect one transistor, when striking the on-state PMOS, there is no SET appearing in the circuit, so the SET sensitive region is just around the off-state PMOS. However, in the advanced technologies, SET can be produced by striking the on-state transistor due to the charge sharing collection, and $W_{\rm SET}$ can be larger than that produced in condition 1 when LET is large enough, which is shown in Fig. 2. This indicates that the SET sensitive area will significantly increase in the advanced technologies.

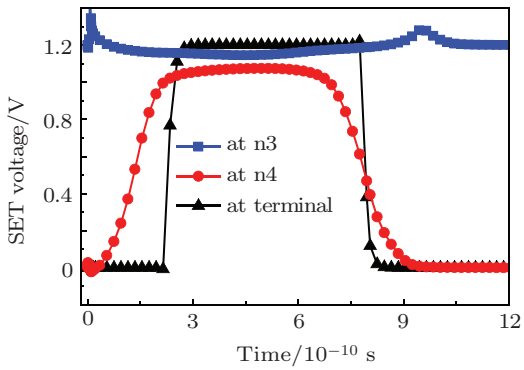


Fig. 4. (color online) SET pulse waveforms at the struck node n3, node n4, and the terminal of the chain in condition 2.

4. Discussion

With technologies scaling down in size, multiple-transistor charge sharing collection becomes a main phenomenon because the distance between two adjacent transistors becomes very small. As shown in Fig. 5, the mechanisms of the charge sharing collection between the adjacent PMOSs can be classified into diffusion and bipolar effect.[14,15] When an ion strikes through the device, the electron–hole pairs are created along the ion track, and the charges will diffuse throughout the N well. All of the adjacent electrodes have the opportunity to collect the charges, and this is the diffusion charge sharing collection. When the N well potential is disturbed by the ion strike, the P–N junction between the P$^+$ source and the N well will be forward-biased, which makes the parasitic source-channel-drain P$^+$–N–P$^+$ bipolar junction transistor (BJT) turned on, the holes will be injected into the N well from the source, and they will be collected at the drain after they have passed through the channel, this is the bipolar effect charge sharing collection.

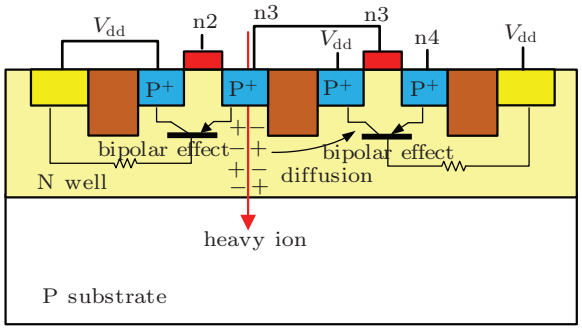


Fig. 5. (color online) Charge sharing collection mechanism between the two adjacent PMOSs.

Both the diffusion and the bipolar effect will be enhanced by reducing the transistor-to-transistor space, and the SET in condition 1 will conspicuously decrease due to the enhanced charge sharing collection of the following transistor. The relationship between $W_{\rm SET}$ and transistor-to-transistor space is studied, when the distance between the PMOSs is varied from

0.20 μm to 1 μm, the LET is 40 MeV·cm^2/mg, and the ion strikes at the drain of the third PMOS normally. As shown in Fig. 6, the SET in condition 1 actually conspicuously decreases with space decreasing. However, figure 6 also shows that the SET in condition 2 will be present in the simulation when the transistor-to-transistor space decreases sufficiently, which indicates that excessively decreasing the transistor-to-transistor space for SET mitigation will play a reversed effect, the traditional SET RHBD rules need to be modified when considering this new effect in the advanced technologies.

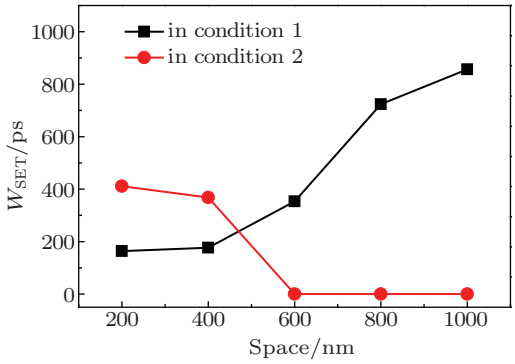


Fig. 6. (color online) Plots of W_{SET} versus the space between PMOSs (condition 1: striking the off-state PMOS; condition 2: striking the on-state PMOS).

The previous work also verified that the bipolar effect will be pronouncedly enhanced by increasing the temperature,[16–18] so the charge sharing collection of the adjacent transistors will also be enhanced correspondingly. The relationship between W_{SET} and temperature is studied in the cases where the temperature is varied from 200 K to 400 K, the distance between the PMOSs is 200 nm, LET is 40 MeV·cm^2/mg, and the ion strikes at the drain of the third PMOS normally. As shown in Fig. 7, the SET in condition 1 actually significantly decreases as temperature increases. However, the SET in condition 2 also significantly increases with temperature increasing. This also indicates that the threat of SET will not be weakened at high temperature in the advanced technology.

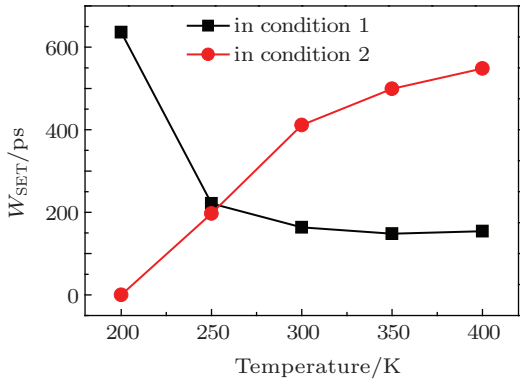


Fig. 7. (color online) Plots of W_{SET} versus temperature (condition 1: striking the off-state PMOS; condition 2: striking the on-state PMOS).

All of the previous discussion indicates that the charge sharing collection plays a dual role in SET mitigation, and that the enhancing of charge sharing collection can significantly reduce W_{SET} in condition 1. However, the enhancing of charge sharing collection can also increase W_{SET} in condition 2, so some traditional SET conclusions or RHBD techniques need to be reevaluated in the advanced technologies. In our previous work, the three-transistor inverter has been proven to be of a better structure than the two-transistor inverter in RHBD IC design.[19,20] As shown in Fig. 8, in the three-transistor inverter layout design, the source is isolated, and the parasitic bipolar junction transistor (BJT) structure is broken by shallow trench isolation (STI), so the bipolar effect is efficiently weakened. In the advanced technologies, when considering the effect of charge sharing collection on SET, the hardening effect of this structure on SET need to be studied again.

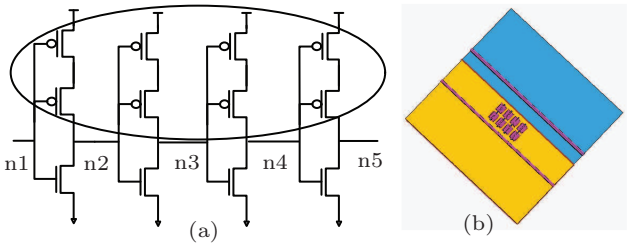


Fig. 8. (color online) Three-transistor inverter chain for SET mitigation. (a) The circuit, (b) the layout configuration.

The relationship between W_{SET} and LET is studied in the three-transistor inverter chain, in the cases where the distance between the PMOSs is also 0.20 μm, and the values of LET are 10, 20, 30, 40, 50 MeV·cm^2/mg, and the ion still strikes at the drain of the third PMOS normally (off-state condition is referred to as condition 3, and on-state condition is named condition 4). The simulation results are shown in Fig. 9. The SET does not appear in the circuit in condition 4. A comparison of the result between Figs. 2 and 9 indicates that the three-transistor still retains a good characteristic in P-hit SET mitigation.

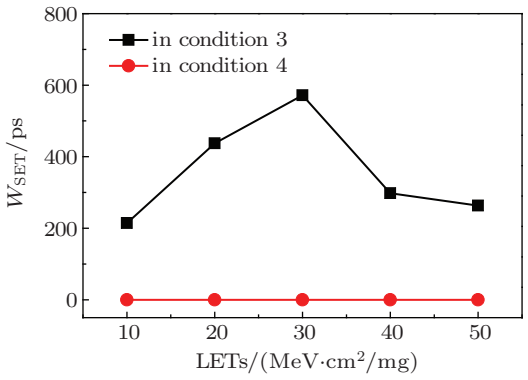


Fig. 9. (color online) Plots of W_{SET} versus LET (condition 3: striking the off-state PMOS; condition 4: striking the on-state PMOS).

The relationship between W_{SET} and the transistor-to-transistor space is also studied in this inverter chain, in the cases where the distance between the PMOSs is varied from 0.20 μm to 1 μm, and LET is 40 MeV·cm^2/mg, and the ion strikes at the drain of the third PMOS normally. As shown in Fig. 10, SET does not appear in the circuit in condition 4 in all simulations, and the SET induced in condition 3 conspicuously decreases when the transistor-to-transistor space decreases sufficiently, so it is beneficial to reducing W_{SET} to try to reduce the transistor-to-transistor space in this three-transistor structure. When the space is 0.20 μm, the values of maximal W_{SET} are 411.443 ps (Fig. 6) and 298.017 ps (Fig. 10), and the value of W_{SET} decreases to 113.426 ps.

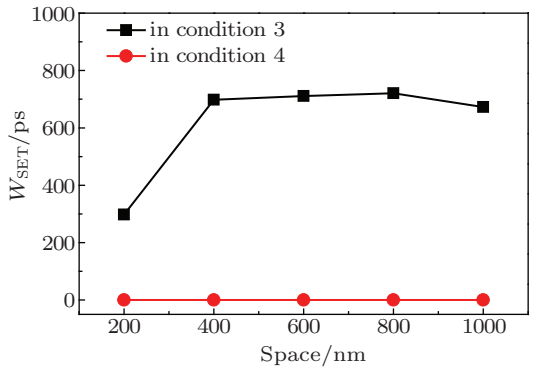


Fig. 10. (color online) Plots of W_{SET} versus the space between PMOSs (condition 3: striking the off-state PMOS; condition 4: striking the on-state PMOS).

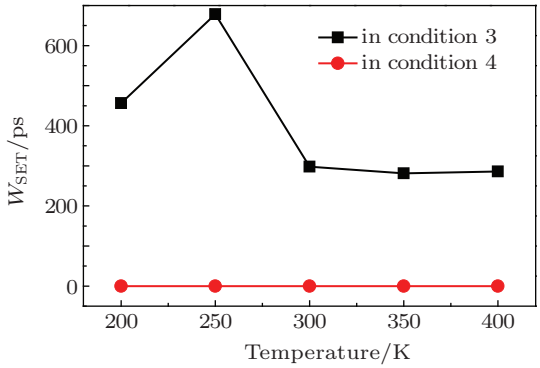


Fig. 11. (color online) Plots of W_{SET} versus temperature (condition 1: striking the off-state PMOS; condition 2: striking the on-state PMOS).

The relationship between W_{SET} and the temperature is also studied in this inverter chain, in the cases where the temperature is varied from 200 K to 400 K, the distance between the PMOSs is 0.20 μm, the LET is 40 MeV·cm^2/mg, and the ion strikes at the drain of the third PMOS normally. As shown in Fig. 11, the SET does not appear in the circuit in condition 4 in all simulations. A comparison of the results between Figs. 7 and 11 indicates that, only when temperature is 250 K, will the value of W_{SET} in condition 3 be larger than that in condition 1. When temperature is larger than 300 K, W_{SET} significantly decreases in the proposed three-transistor inverter, so the proposed RHBD layout structure is still a better method in the RHBD IC design in the extreme environment where both the high temperature and the single event effects are present, and the soft errors will be reduced by using this layout structure.

5. Conclusion

In this paper, we conclude that the electrically-related transistor charge sharing collection plays a dual role in SET mitigation in advanced technologies, and we discuss this phenomenon in the two-transistor inverter chain in depth. Due to the charge sharing collection of the adjacent PMOSs, the SET can be induced by striking the on-state PMOS, which indicates that the SET sensitive area is no longer just around the off-state transistors as it is in the older technologies where only ion struck off-state transistor can induce SET. This dual role of the charge sharing collection in SET puts us in a dilemma, and the enhancing of the charge sharing collection to reduce W_{SET} may face challenges. In the advanced technique, not only the W_{SET} in condition 1, but also the W_{SET} in condition 2 needs to be reduced, and the new RHBD techniques must achieve a good balance between these two types of SET mitigation. The studies additionally indicate that the three-transistor inverter can achieve a good balance.

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