Two-dimensional threshold voltage model of a nanoscale silicon-on-insulator tunneling field-effect transistor*

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The tunneling field-effect transistor (TFET) is a potential candidate for the post-CMOS era. In this paper, a threshold voltage model is developed for this new kind of device. First, two-dimensional (2D) models are used to describe the distributions of potential and electric field in the channel and two depletion regions. Then based on the physical definition of threshold voltage for the nanoscale TFET, the threshold voltage model is developed. The accuracy of the proposed model is verified by comparing the calculated results with the 2D device simulation data. It has been demonstrated that the effects of varying the device parameters can easily be investigated using the model presented in this paper. This threshold voltage model provides a valuable reference to TFET device design, simulation, and fabrication.

Keywords: tunnel field-effect transistor, band-to-band tunneling, subthreshold swing, gated P–I–N diode

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1. Introduction

Up to date, the characteristics (subthreshold swing, transconductance, operation frequency) of conventional field-effect transistors (FETs) have reached their theoretical limits. Transistors based on the tunneling current appear to be promising candidates to overcome these limitations. Simulations and experiments have shown that tunneling field-effect transistors (TFETs) can have subthreshold swing,[1,2] operation frequency,[3] and transconductance better than those of the conventional FETs. Contrary to metal–oxide–semiconductor field-effect transistors, the subthreshold swing of tunneling field-effect transistors is not limited to 60 mV/dec.[1] In addition, a TFET has a very small leakage current (in the range of femtoamperes[4]) due to the large tunneling barrier formed when the device is turned off. However, the TFET suffers from a low ON current. Therefore, various techniques to improve the ON current in the TFET have been proposed,[4–9] such as vertical structures, carbon nanotubes transistors, III–V compounds, double-gate configuration, bandgap engineering, strain engineering, and gate engineering.

The basic structure of the TFET, as shown in Fig. 1, is a gated P–I–N diode. To switch the device on, the P–I–N diode is reversely biased, and a voltage is applied to the gate. The threshold voltage is one of the most important electrical parameters of a solid-state switch. Tere are models for the threshold voltage in MOS transistors.[10–13] However, there has been no research on the TFET regarding the threshold voltage. In this paper, a model for the threshold voltage of the nanoscale TFET (N-TFET) is developed based on the physical definition of threshold voltage for the N-TFET by solving the two-dimensional (2D) Poisson's equation in the channel and two depletion regions. By analyzing the model, the dependences of threshold voltage on the drain–source voltage, the Si layer thickness, the gate length, and the gate dielectric are studied. The model can predict the improved performance of the physical threshold voltage when using high-κ dielectrics and thin Si film and the limited effect on the threshold voltage when scaling the gate length. Based on our results, we demonstrate that our model can be used as an efficient tool for the design and characterization of silicon-on-insulator (SOI) nanoscale TFETs. The efficiency of the model is verified by comparing the model results with the 2D simulation results.

2. Model

Figure 1 shows the N-TFET architecture used for the modeling. The gate length L_g, the gate oxide thickness t_{ox}, the Si film thickness t_{si}, the source doping N_1, the P^- or N^- region doping N_2, the drain doping N_3, and the gate work function Φ_M are the input parameters of this proposed model. The x and y axes are shown in Fig. 1. The thickness of the buried oxide (BOX) is considered as infinite.

The physical definition of the TFET threshold voltage is the gate voltage marking the transition from an exponential dependence of the drain current on the applied bias to a linear dependence. This marks the transition between strong control and weak control of the tunneling energy barrier width at the tunnel junction by that voltage.[14] The inflection point in the tunneling energy barrier width w_{bs}[14,15] shows the transition

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point between a quasi-exponential dependence and a linear dependence of current on the gate voltage. In order to derive the threshold voltage model, we first solve the 2D Poisson's equation on three regions I, II, and III shown in Fig. 1 for the potential and the electric field.

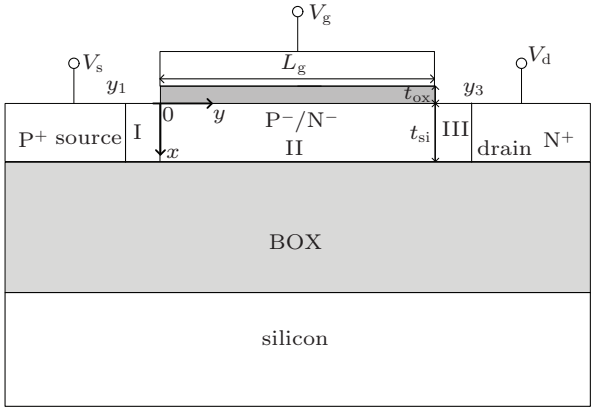


Fig. 1. Schematic diagram of the TFET used in this paper. The three regions studied with the Poisson's equation are the P$^-$ or N$^-$ region (II) and the depletion regions induced by the junctions inside the source and drain (I and III).

We want to predict the characteristic of the N-TFET from the off-state to the onset of the on-state. In this regime, the mobile charge can be negligible.[16] Therefore the potential distribution in the silicon thin film can be written as

$$\frac{\partial^2 \varphi_i(x,y)}{\partial x^2} + \frac{\partial^2 \varphi_i(x,y)}{\partial y^2} = -\frac{qN_s}{\varepsilon_{si}},$$
$$0 \le x \le t_{si}, \quad i = \mathrm{I},\ \mathrm{II},\ \mathrm{III}, \tag{1}$$

where $\varphi_i(x,y)$ is the electrostatic potential in regions I, II, III, ε_{si} is the silicon dielectric constant, and N_s is the Si film effective doping and is equal to $-N_1$ in the P-type source (region I), N_3 in the N-type drain (region III), and $\pm N_2$ in the P$^-$ or N$^-$ region (region II). As long as the doping level is less than 10^{17} cm^{-3}, the exact concentration and the type in region II are not important. The P-type doping in region II is used in this paper.

The potential profile in the vertical direction of the Si film, i.e., the x dependence of $\varphi_i(x,y)$, can be approximated by a second-order polynomial

$$\varphi_i(x,y) = \varphi_{s,i}(y) + a_{0,i}(y)x + a_{1,i}(y)x^2,$$
$$0 \le x \le t_{si}, \quad i = \mathrm{I},\ \mathrm{II},\ \mathrm{III}, \tag{2}$$

where $\varphi_{s,i}(y)$ is the surface potential, and the arbitrary coefficients $a_{0,i}(y)$ and $a_{1,i}(y)$ are functions of y only.

For region II, $a_{0,\mathrm{II}}(y)$ and $a_{1,\mathrm{II}}(y)$ can be determined by the boundary conditions

$$\left.\frac{\mathrm{d}\varphi_{\mathrm{II}}(x,y)}{\mathrm{d}x}\right|_{x=0} = -\frac{\varepsilon_{ox}}{\varepsilon_{si}}\left(\frac{V'_g - \varphi_{s,\mathrm{II}}(y)}{t_{ox}}\right), \tag{3}$$

$$\left.\frac{\mathrm{d}\varphi_{\mathrm{II}}(x,y)}{\mathrm{d}x}\right|_{x=t_{si}} = 0, \tag{4}$$

where $V'_g = V_g - \phi_{MS}$, and $\phi_{MS} = \phi_M - \phi_S$ is the flat band voltage for the gate. The semiconductor work function can be written as

$$\phi_S = \chi_{si} + \frac{E_g}{2} + \phi_F,$$

where χ_{si} is the electron affinity, E_g is the silicon bandgap, $\phi_F = V_T \ln(N_2/n_i)$ is the Fermi potential, V_T is the thermal voltage, and n_i is the intrinsic carrier concentration.

Substituting $a_{0,\mathrm{II}}(y)$ and $a_{1,\mathrm{II}}(y)$ in Eq. (2) and then in Eq. (1), we obtain

$$\frac{\partial^2 \varphi_{s,\mathrm{II}}(y)}{\partial y^2} - \alpha_2^2 \varphi_{s,\mathrm{II}}(y) = \beta_2, \tag{5}$$

where $\alpha_2^2 = C_{ox}/t_{si}\varepsilon_{si}$, $\beta_2 = (qN_2/\varepsilon_{si}) - (C_{ox}V'_g/t_{si}\varepsilon_{si})$, and $C_{ox} = \varepsilon_{ox}/t_{ox}$. The solution for Eq. (5), which is a simple second-order non-homogenous differential equation with constant coefficients, can be written as

$$\varphi_{s,\mathrm{II}}(y) = A_2 \exp(\alpha_2 y) + B_2 \exp(-\alpha_2 y) - \frac{\beta_2}{\alpha_2^2}. \tag{6}$$

The electric field distribution can be written as

$$E_{s,\mathrm{II}}(y) = -A_2\alpha_2 \exp(\alpha_2 y) + B_2\alpha_2 \exp(-\alpha_2 y). \tag{7}$$

In the depletion regions I and III, the fringing field effect is taken into account by using the conformal mapping technique $C'_{ox} \cong \frac{2}{m\pi}\frac{\varepsilon_{ox}}{t_{ox}}$[17] with the condition that m must satisfy $\sin(m\pi/2) = 1$. Therefore the surface potentials in regions I and III can be written as

$$\varphi_{s,\mathrm{I}}(y) = A_1 \exp(\alpha_1 y) + B_1 \exp(-\alpha_1 y) - \frac{\beta_1}{\alpha_1^2}, \tag{8}$$

$$\varphi_{s,\mathrm{III}}(y) = A_3 \exp(\alpha_3 y) + B_3 \exp(-\alpha_3 y) - \frac{\beta_3}{\alpha_3^2}. \tag{9}$$

The electric field distributions can be written as

$$E_{s,\mathrm{I}}(y) = -A_1\alpha_1 \exp(\alpha_1 y) + B_1\alpha_1 \exp(-\alpha_1 y), \tag{10}$$

$$E_{s,\mathrm{III}}(y) = -A_3\alpha_3 \exp(\alpha_3 y) + B_3\alpha_3 \exp(-\alpha_3 y), \tag{11}$$

where $\alpha_1^2 = \alpha_3^2 = C'_{ox}/t_{si}\varepsilon_{si}$, $\beta_1 = (qN_1/\varepsilon_{si}) - (C'_{ox}V'_g/t_{si}\varepsilon_{si})$, and $\beta_3 = -(qN_3/\varepsilon_{si}) - (C'_{ox}V'_g/t_{si}\varepsilon_{si})$.

Now we calculate the values of y_1 and y_3. Since the basic structure of the TFET is a gated P–I–N diode, the potential in the channel region is modulated by the gate voltage. To consider the influence of the two terminals on each other, the lengths of regions I and III should be calculated by imposing $E_{s,\mathrm{I}}(y_1) = 0$ and $E_{s,\mathrm{III}}(y_3) = 0$, but the calculation would be troublesome. Here we make a good approximation, separately considering the two junctions (source–body and drain–body junctions). Then y_1 and y_3 are calculated as

$$|y_1| = \sqrt{2\varepsilon_{si}(\varphi_l - \varphi_s)/(qN_1)},$$

$$y_3 = \sqrt{2\varepsilon_{si}(\varphi_d - \varphi_l)/(qN_3)},$$

where $\varphi_s = -\frac{KT}{q}\log\left(\frac{N_1}{n_i}\right)$ and $\varphi_d = V_d + \frac{KT}{q}\log\left(\frac{N_3}{n_i}\right)$ are the boundary values of the potential at the source and the drain depletion region ends, respectively, $\varphi_l = V'_g - qN_2 t_{si} t_{ox}/\varepsilon_{si}$ is the potential obtained by solving the 1D Possion's equation in the gate oxide and the Si film regions (long-channel approximation). We can see that $|y_1|$ and y_3 depend on the gate voltage. When the gate voltage increases, $|y_1|$ increases, whereas y_3 decreases, as suggested by our simulation. The drain voltage influences y_3, and when V_d increases, y_3 increases.

In order to determine the unknown functions A_1, B_1, A_2, B_2, A_3, and B_3, the following boundary conditions are used:

$$\begin{cases} \varphi_{s,I}(y_1) = -\dfrac{KT}{q}\log\left(\dfrac{N_1}{n_i}\right), \\ \varphi_{s,III}(y_3 + L_g) = V_d + \dfrac{KT}{q}\log\left(\dfrac{N_3}{n_i}\right), \\ \varphi_{s,I}(0) = \varphi_{s,II}(0), \\ \varphi_{s,II}(L_g) = \varphi_{s,III}(L_g), \\ E_{s,I}(0) = E_{s,II}(0), \\ E_{s,II}(L_g) = E_{s,III}(L_g). \end{cases} \tag{12}$$

Then we can obtain coefficents A_1, B_1, A_2, B_2, A_3, and B_3 in Eqs. (6), (8), and (9).

The threshold voltage of the TFET is the gate voltage marking the transition between the strong and the weak controls of the tunneling energy barrier width at the tunnel junction. When the potential in $y = w_{bs}$ reaches the potential $V_d + \frac{KT}{q}\log\left(\frac{N_3}{n_i}\right)$, the drain current has a liner dependence on the applied bias. By substituting $y = w_{bs}$ and $V_d + \frac{KT}{q}\log\left(\frac{N_3}{n_i}\right)$ into Eq. (6), the equation can be written as

$$A_2\exp(\alpha_2 w_{bs}) + B_2\exp(-\alpha_2 w_{bs}) - \frac{\beta_2}{\alpha_2^2} = V_d + \frac{KT}{q}\log\left(\frac{N_3}{n_i}\right),$$

where A_2, B_2, and β_2 are functions of the gate voltage V_g. By solving this equation numerically for V_g, the threshold voltage can be obtained, which will be shown in Section 4.

3. Simulation

All simulations are done in Silvaco Atlas.[18] Junctions are ideally abrupt, with the doping concentrations of $N_1 = 10^{20}$ cm^{-3} in the P-type source, $N_3 = 5\times10^{18}$ cm^{-3} in the N-type drain, and $N_2 = 10^{17}$ cm^{-3} in the lightly doped P-type region. The buried oxide has a thickness $t_{box} = 300$ nm. The gate work function is $\Phi_M = 4.5$ eV. The simulations use a very fine mesh across the region where the tunneling takes place. The gate leakage is neglected in these simulations. Models employed in our simulation study include the nonlocal band-to-band tunneling (BTBT) model, the band-gap-narrowing model, and the quantum density-gradient model.

The simulated TFET is a gated P–I–N diode with a lightly doped P-type intrinsic region to avoid convergence problems as shown in Fig. 1. Applying a positive voltage to the drain reversely biases the P–I–N diode, then a positive gate voltage is used to enable the TFET conduction by electron band-to-band tunneling between the source and the insulator region.

As shown in Figs. 2–5, the TFETs have outstanding nonlinear abrupt I_{ds}–V_g characteristics. Figure 2 shows I_{ds}–V_g curves for TFETs with three different V_d values. The curves are shown on a logarithmic scale on the left, and on a linear scale on the right. The shape of the curve can be understood by using both the logarithmic and the linear scales. Figure 3 shows the normalized I_{ds}–V_g characteristics for two different gate dielectrics. It is clear that the current increases as the gate dielectric constant increases. Figure 4 plots TFET I_{ds}–V_g characteristics for various silicon body thicknesses. It is clear that the TFETs are sensitive to this

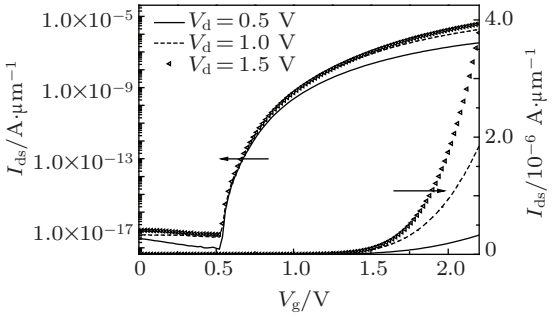


Fig. 2. Tunneling FET I_{ds}–V_g curves obtained from the Silvaco simulations for varying values of V_d, where $L_g = 50$ nm, $t_{ox} = 3$ nm, $t_{si} = 10$ nm, and $\varepsilon_{ox} = 7.5$.

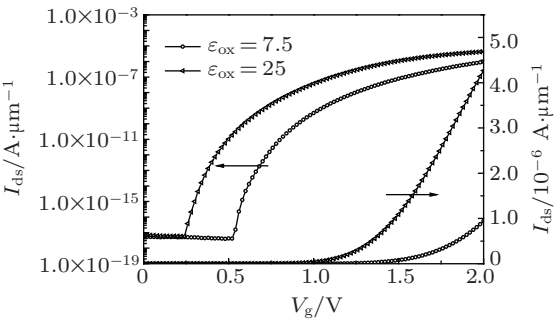


Fig. 3. The I_{ds}–V_g curves obtained from the Silvaco simulations for a TFET with two different gate dielectric stacks: Si_3N_4 and ZrO_2, where $L_g = 50$ nm, $t_{ox} = 3$ nm, $t_{si} = 10$ nm, and $V_d = 1$ V.

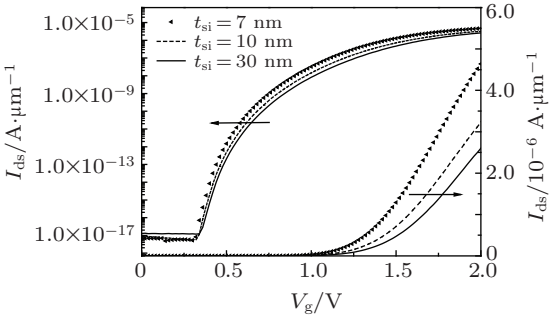


Fig. 4. Tunneling FET I_{ds}–V_g curves obtained from the Silvaco simulations for various silicon body thicknesses, where $L_g = 50$ nm, $t_{ox} = 3$ nm, $\varepsilon_{ox} = 29$, and $V_d = 1$ V.

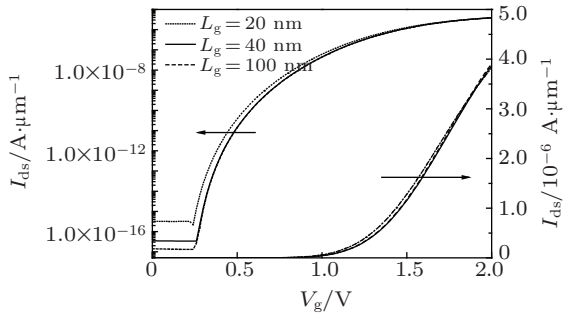


Fig. 5. Tunneling FET I_{ds}–V_g curves obtained from the Silvaco simulations for various gate lengthes, where $t_{si} = 10$ nm, $t_{ox} = 3$ nm, $\varepsilon_{ox} = 29$, and $V_d = 1$ V.

thickness, which influences the shapes of their I_{ds}–V_g curves. Figure 5 plots the typical I_{ds}–V_g characteristics for TFETs with channel lengths 20 nm, 40 nm, and 100 nm. We can see that the on current is nearly independent of L_g, and it has little effect on the transfer characteristics as long as the device is longer than a critical length below which too many P–I–N leakage currents present in the off state.

4. Model evaluation

The model is tested against the simulation results with different sets of parameters. We verify that the threshold voltages of the TFET for different drain biasing conditions, Si body thicknesses, gate dielectrics, and gate lengths are well predicted.

The easiest way to extract the threshold voltage for the TFET is to use the constant current method by finding the gate voltage at which $I_{ds} = 10^{-7}$ A/μm,[5,6,14] however, this technique uses an arbitrary value and has practically no physical meaning despite of its practical interest. In this paper, we use the transconductance change (TC) method to extract the threshold voltage (already validated for the MOS transistor[19]) of the N-TFET. The TC method universally defines the threshold voltage of any non-linear device as the gate voltage corresponding to the maximum of the transconductance derivative $\mathrm{d}g_m/\mathrm{d}V_g$. This derivative method of threshold voltage extraction thus locates the voltage where there is a transition between strong and weak controls of the tunneling energy barrier width.

The model is first tested on a TFET with $L_g = 50$ nm, $t_{ox} = 3$ nm, and $t_{si} = 10$ nm under a change in the drain voltage. Figure 6 plots the variation of threshold voltage with drain voltage for different gate dielectrics. The line represents the model results, and the scatter represents the simulation results which have been extracted using the TC method as show in Figs. 7 and 8. It can be found that the calculated and the simulation results agree very well with each other. We can observe that V_{th} increases when V_d increases. This can be explained by the fact that the gate retains the quasi-exponential control of the current over a larger voltage range with a higher drain voltage applied, as shown in Figs. 7 and 8.

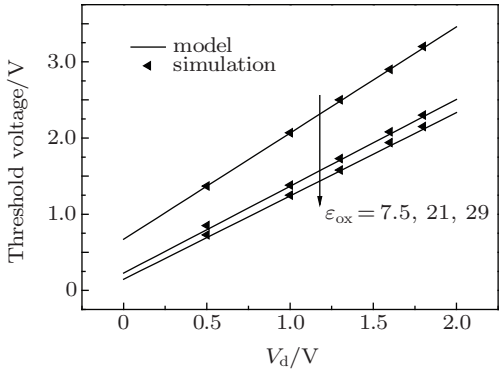


Fig. 6. Variations of threshold voltage with the drain voltage for different gate dielectrics, where $L_g = 50$ nm, $t_{ox} = 3$ nm, and $t_{si} = 10$ nm.

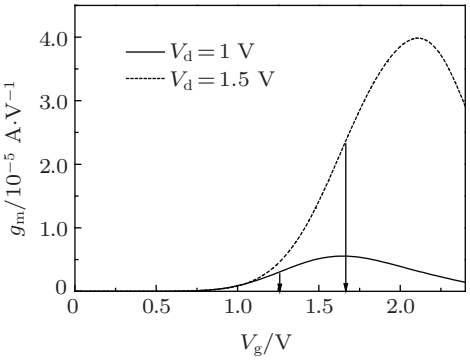


Fig. 7. The V_{th} extracted from the derivative g_m for $L_g = 50$ nm, $t_{ox} = 3$ nm, $t_{si} = 10$ nm, and $\varepsilon_{ox} = 29$.

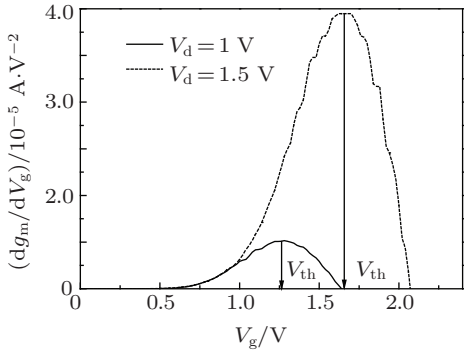


Fig. 8. The V_{th} extracted from the derivative $\mathrm{d}g_m/\mathrm{d}V_g$ for $L_g = 50$ nm, $t_{ox} = 3$ nm, $t_{si} = 10$ nm, and $\varepsilon_{ox} = 29$.

Looking at the length dependence of the threshold voltage V_{th} in Fig. 9, reported for the derivative extract method and the model result, we find a good coincidence. In Fig. 9, no roll-off can be seen. This is motivated by the fact that the conduction mechanism in the TFET is completely different from that in the MOSFET. The maximum field is always at the tunnel junction, and is independent of the device length. Our model is able to describe this phenomenon. The derivative extract threshold voltage method is shown in Fig. 10.

Figure 11 shows the threshold voltage characteristic of the N-TFET as a function of the gate dielectric at $V_d = 1$ V and 0.5 V. Here ε_{ox} is scaled from 29 to 3.9 at constant $t_{ox} = 3$ nm. Figure 12 shows the derivative $\mathrm{d}g_m/\mathrm{d}V_g$ for a structure with 3 nm dielectric ($\varepsilon_{ox} = 29$ and $\varepsilon_{ox} = 7.5$), 10 nm Silicon thin

film, and 50 nm gate length. The high-κ dielectric provides the gate with a better capacitive control of the barrier width in the tunnel junction, so the threshold voltage V_{th} decreases when the gate dielectric increases. Figure 13 plots the threshold voltage variation with the change in the Si layer thickness. The V_{th} decreases linearly when the Si film thickness decreases. In Fig. 14, the derivatives dg_m/dV_g for 10 nm and 30 nm Si films are plotted. The TFET is sensitive to the thickness, which influences the shape of its I_{ds}–V_g curve, as shown in Fig. 4. A thinner film modifies the electric field lines, increasing the gate control of the barrier width in the tunnel junction. The model presented in this paper can describe this effect well.

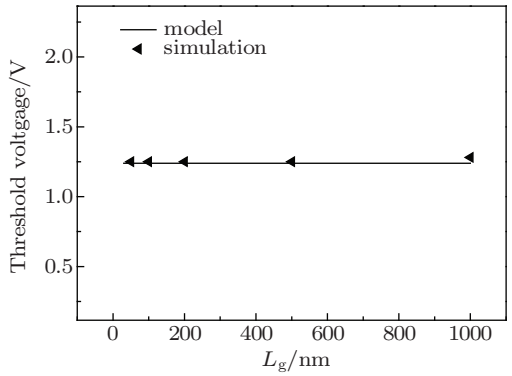


Fig. 9. Threshold voltage versus gate length with $V_d = 1$ V, $\varepsilon_{ox} = 29$, $t_{ox} = 3$ nm, and $t_{si} = 10$ nm.

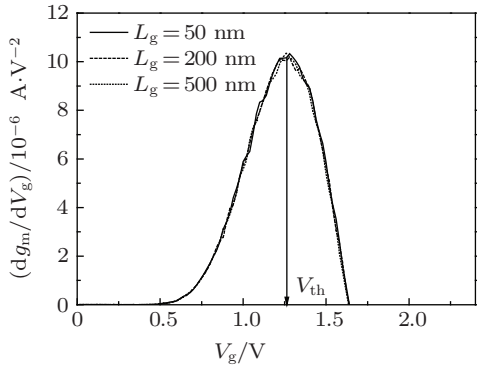


Fig. 10. The V_{th} extracted from the derivative dg_m/dV_g for different gate lengths with $\varepsilon_{ox} = 29$, $t_{ox} = 3$ nm, $t_{si} = 10$ nm, and $V_{ds} = 1$ V.

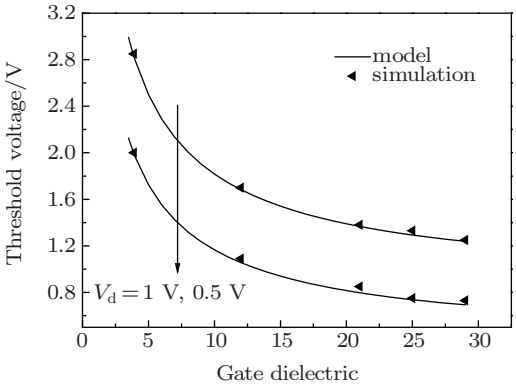


Fig. 11. Variations of threshold voltage with the gate dielectric for structure $L_g = 50$ nm, $t_{ox} = 3$ nm, $t_{si} = 10$ nm, $V_{ds} = 1$ V, and $V_d = 0.5$ V.

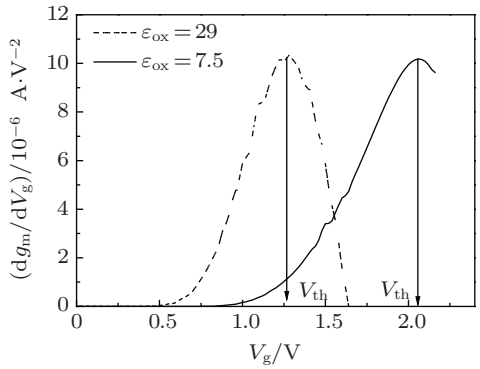


Fig. 12. The V_{th} extracted from the derivative dg_m/dV_g for a structure with 3 nm dielectric ($\varepsilon_{ox} = 29$ and $\varepsilon_{ox} = 7.5$), where $t_{si} = 10$ nm, $L_g = 50$ nm, and $V_d = 1$ V.

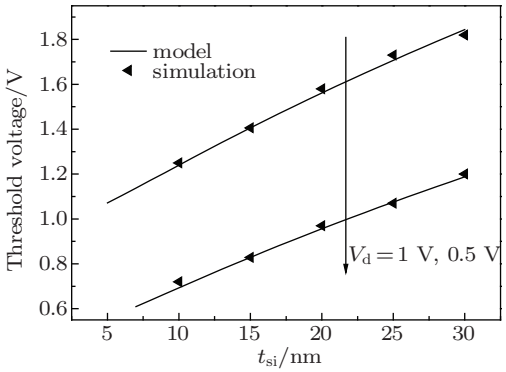


Fig. 13. Variations of threshold voltage with the Si film thickness for structure with $L_g = 50$ nm, $t_{ox} = 3$ nm, and $\varepsilon_{ox} = 29$.

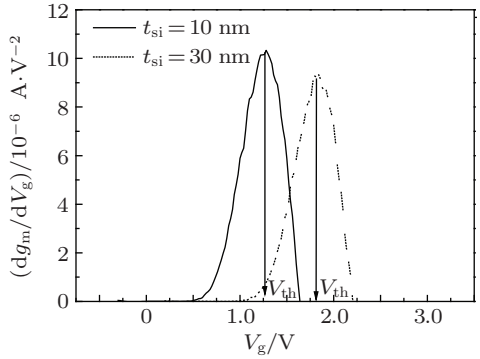


Fig. 14. The V_{th} extracted from the derivative dg_m/dV_g for a structure with $t_{si} = 10$ nm and 30 nm, $t_{ox} = 3$ nm, $L_g = 50$ nm, $\varepsilon_{ox} = 29$, and $V_d = 1$ V .

5. Conclusion

In this paper, expressions have been derived for the potential and the electric field in the channel and two depletion regions of the N-TFET based on the 2D solution of the Poisson's equation. Then, based on the physical definition of the threshold voltage, a threshold voltage model for the TFET has been developed. We have shown that the models predict the device characteristics for a large range of parameters and permit gaining an insight into the device physics. The model can also predict the improved performance of the physical threshold voltage when using high-κ dielectrics and thin Si film and

the limited effect on the threshold voltage when scaling the gate length.

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