The effects of radiation damage on power VDMOS devices with composite SiO_2–Si_3N_4 films

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Total dose effects and single event effects on radiation-hardened power vertical double-diffusion metal oxide semiconductor (VDMOS) devices with composite SiO_2–Si_3N_4 film gates are investigated. The relationships among the important electrical parameters of the samples with different thickness SiO_2–Si_3N_4 films, such as threshold voltage, breakdown voltage, and on-state resistance in accumulated dose, are discussed. The total dose experiment results show that the breakdown voltage and the on-state resistance barely change with the accumulated dose. However, the relationships between the threshold voltages of the samples and the accumulated dose are more complex, and not only positively drift, but also negatively drift. At the end of the total dose experiment, we select the group of samples which have the smaller threshold voltage shift to carry out the single event effect studies. We find that the samples with appropriate thickness ratio SiO_2–Si_3N_4 films have a good radiation-hardening ability. This method may be useful in solving both the SEGR and the total dose problems with the composite SiO_2–Si_3N_4 films.

Keywords: power VDMOS device, total dose effects, single event effects, composite SiO_2–Si_3N_4 films

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1. Introduction

Due to their special structures, power vertical double-diffusion metal oxide semiconductor (VDMOS) devices have high input impedance, low driven power, high switching speed, and good thermal stability. In addition, they have negative temperature coefficients and do not have the second breakdown as in normal transistors. With these advantages, the power VDMOS devices have been extensively applied to different fields, such as aerospace and nuclear environments.[1,2]

It is well known that there are many energetic charged particles, cosmic rays, and solar flares in space. The performance of power VDMOS devices degrades in high-frequency switching power supplies, degrading the electrical parameters, decreasing the reliability, and even failing in function.[3,4] Compared with other devices, such as a satellite's secondary power switching device, the reliability of power VDMOS devices is particularly important. Once the device's performance is affected, it may reduce the life of the satellite, and in severe cases it may lead to the failure of the space mission.

When power VDMOS devices are used in a satellite electronic system, the space radiation environment will lead to single event burnout (SEB) and single event gate rupture (SEGR).[5–7] In recent years, SEGR has attracted more and more attention. Studies show that the most effective way to mitigate the SEGR susceptibility of power MOSFETs is to increase the thickness of the gate oxide.[8] Increasing the gate oxide thickness increases the SRGR threshold drain–source and gate–source biases. However, we know that by making the oxide layer thicker, the sensitivity of the power VDMOS devices to the total dose is increased. This is because the thicker the gate oxide is, the larger the number of ionizing generated electron–hole pairs is.[8] Therefore, the number of trapped holes near the Si–SiO_2 interface is larger, and may cause the electrical parameters to degrade severely in power VDMOS devices.

It has been reported that composite SiO_2–Si_3N_4 (silicon nitride–silicon dioxide) films are less sensitive to ionizing radiation than pure SiO_2 (silicon dioxide) films.[9–16] Because the permittivity of Si_3N_4 is greater than that of SiO_2, composite SiO_2–Si_3N_4 films can be thicker than pure SiO_2 films, but still have the same charge storage capability.[15] Consequently, composite SiO_2–Si_3N_4 films may solve both SEGR and total dose problems. In the present work, the total dose effects on different thickness ratios of SiO_2–Si_3N_4 films for power VDMOS devices are studied. The experimental results show that the threshold voltages of the power VDMOS devices with different thickness ratios of SiO_2–Si_3N_4 films exhibit complex changes with the total dose, not only positive drift, but also negative drift. It is found that the threshold voltage shift of a certain suitable thickness ratio sample is only 0.2 V at 1500 Gy(Si). Although, as the oxide layer thickness increases, the power VDMOS devices with suitable thickness ratios of SiO_2–Si_3N_4 films gate oxide structure are less sensitive to the ionizing radiation. Meanwhile, the single event irradiation experimental results show that this method improves the SEGR-hardened level without increasing any total dose ra-

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diation damage. The research results are used to help design an optimum thickness ratio of SiO_2–Si_3N_4 films to minimize the threshold voltage shift of power VDMOS devices during total dose irradiation and improve the SEGR-hardened level.

In this paper, the total dose irradiation damage effects and the single event effects of power VDMOS devices with composite SiO_2–Si_3N_4 films are investigated. The paper is organized as follows. In Section 2, we describe samples to be tested and then experimental methods developed. In Section 3, we report some preliminary experimental results, and then in Section 4, the relevant basic mechanisms are presented and used to explain the device behaviors influenced by the radiation. Finally, the conclusion is drawn in Section 5.

2. Experimental samples and methods

2.1. Experimental samples

The experimental samples are n-channel VDMOS devices obtained using radiation-hardening technology, as shown in Fig. 1(a). The device package is the TO-254AA. Typically, the threshold voltage is 2–4 V, the breakdown voltage is 100 V, and the on-state resistance is 65 mΩ. The samples with composite SiO_2–Si_3N_4 films are divided into three groups. The SiO_2 film thickness of all samples is 60 nm, but the Si_3N_4 film thickness is different, which is denoted by A, B, and C with the increasing thickness.

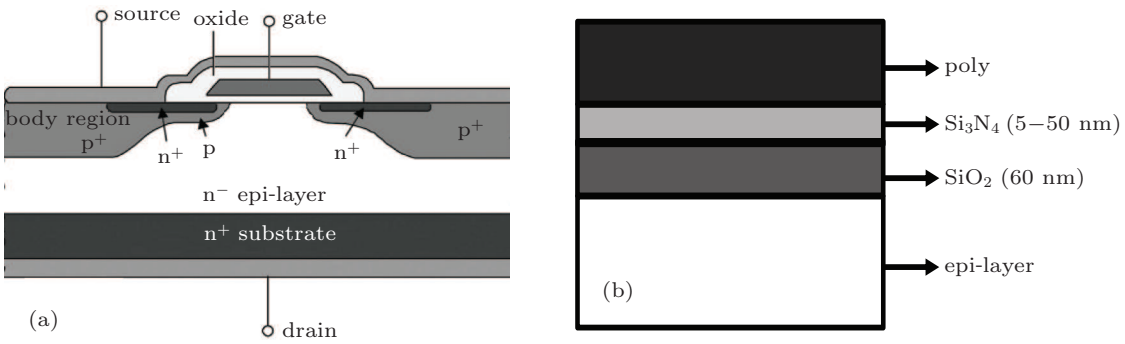


Fig. 1. Cross-section views of (a) the VDMOS structure and (b) the composite SiO_2–Si_3N_4 structure.

2.2. Experimental conditions

The total dose experiment was carried out on a seventy-thousand Curie ^{60}Co γ irradiation source. The dose rate was calibrated by a Fricke (ferrous sulfate) dosimeter. The devices were irradiated with ^{60}Co γ rays to a level of 1×10^3 Gy(Si), the dose rate was 5×10^{-1} Gy(Si)/s. During irradiation and annealing, for testing samples, two bias conditions were used: gate bias $V_{GS} = 12$ V, $V_{DS} = 0$ V; and gate bias $V_{GS} = 0$ V, $V_{DS} = 80$ V. Before and after the irradiation, the threshold voltage, the breakdown voltage, and the on-state resistance were measured by a T3620 power device parameter testing system.

The single event effect (SEE) experiment was carried out at the HIRFL (Heavy Ion Research Facility in Lanzhou) cyclotron facility. Figure 2 is a schematic diagram. The ion selected for the SEE experiment had a range that exceeded the thickness of the epitaxial layer of all test samples. The ion used in the experiment was krypton. The incident LET of the selected ion was 37.42 MeV·cm^2/mg. The fluence rate was 10^3 ion/(cm^2·s). All samples were assembled and tested in TO-254AA packages without a covering lid. The test samples were biased and measured with two 600 V high voltage source measurement units (SMUs) which were connected to a personal computer via two general purpose instrument buses (GPIBs). During the SEE irradiation, the drain and the gate currents were monitored. The in-circuit testing was automatically terminated when the fluence achieved 10^5 ion/cm^2 or when the leakage currents reached pre-set values. During the SEE experiment, four gate-to-source voltages were used, i.e., 0 V, −5 V, −10 V, and −15 V.

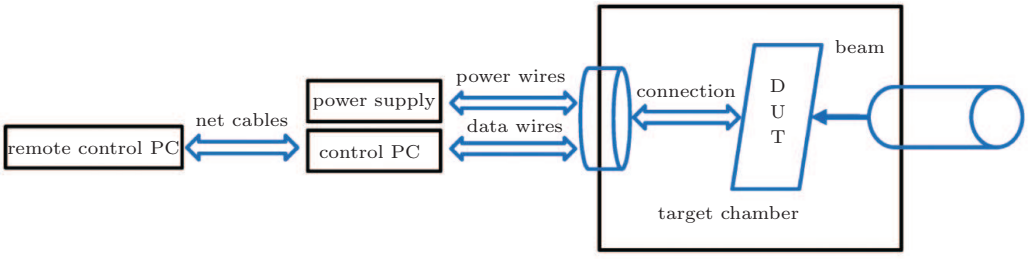


Fig. 2. (color online) Schematic diagram of single event effect irradiation experiments.

2.3. Experimental processes

We performed both total dose and annealing experiments on power VDMOS devices. First, the samples were irradiated at room temperature (25 °C) with ^{60}Co rays to a level of 1×10^3 Gy(Si) under dose rate 5×10^{-1} Gy(Si)/s. Second, those irradiated samples whose threshold voltages exceeded the allowed value were selected for annealing for 168 h at 25 °C. Those irradiated samples whose threshold voltages were within the allowed value were exposed under another 50% irradiation to a total dose of 5×10^2 Gy(Si) at the same dose rate. Third, if the threshold voltage returned back within the allowed value after 25 °C annealing, then the samples were also exposed under another 50% irradiation. After that, they were left in an environmental chamber at 100 °C under the same bias condition with irradiation for 168 h. After the irradiation and annealing, the electrical parameters were measured within 20 min. We carried out the single event irradiation experiment according to the U.S. MIL-STD-750D SEGR experimental method, .

3. Experimental results

Figure 3 shows the threshold voltage shifts of three groups of samples, which are functions of total dose and annealing time. Obviously, the threshold voltages of samples A and B decrease with cumulative dose increasing, especially the threshold voltage of sample B, which only drifts about 0.2 V in an additional 50% dose irradiation. The results show that the threshold voltages of samples A and B have almost recovered to the initial values after annealing for 168 h at 100 °C. Note that the threshold voltage of sample C increases with cumulative dose increasing, as shown in Fig. 3. When the total dose is 1000 Gy(Si), the threshold voltage positive drift is about 2 V. We did not carry out the additional irradiation for this sample. The results of the room annealing experiment show that the threshold voltages of samples C do not recover, so the irradiation was not continued.

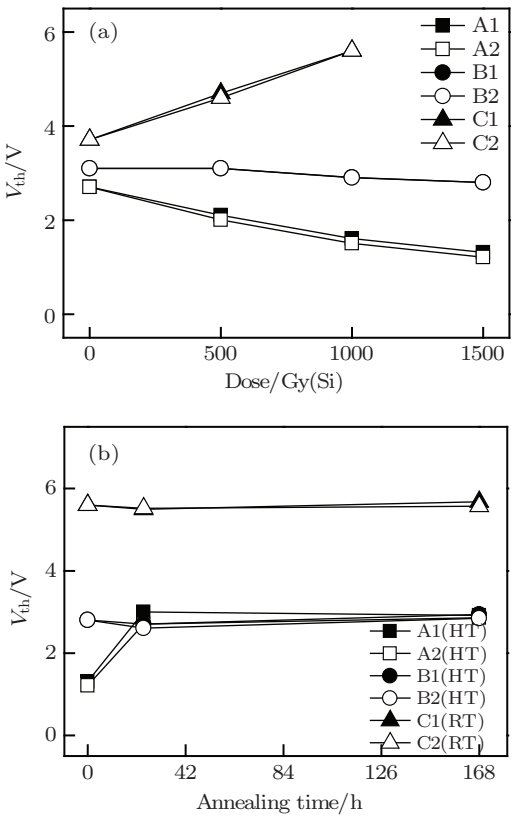


Fig. 3. Threshold voltages of samples A, B, and C versus (a) total dose and (b) annealing time.

For the three groups of samples, which have different thickness ratios of composite SiO_2–Si_3N_4 films, the change of breakdown voltage is not obvious during irradiation and annealing, as shown in Fig. 4. Moreover, the on-state resistances of all samples change slightly with the accumulated dose and the increasing annealing time, as shown in Fig. 5. It is notable that samples C, which have the most obvious change in threshold voltage, have the largest difference in on-state resistances with the accumulated dose.

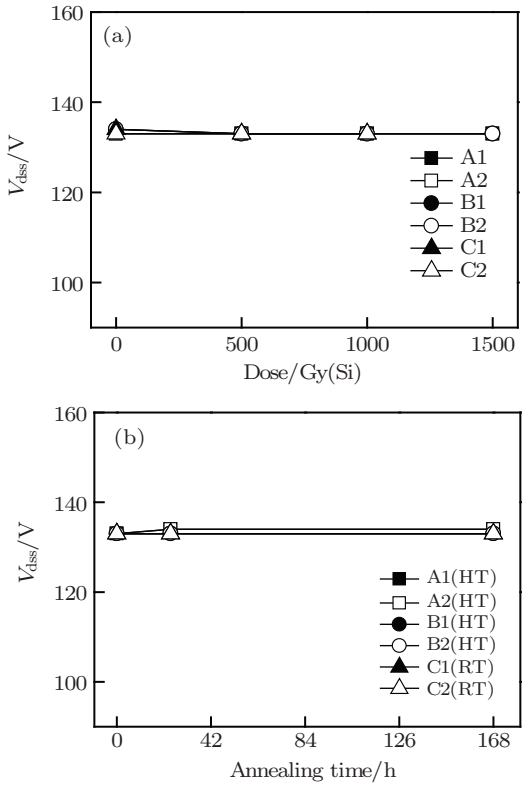


Fig. 4. Breakdown voltages of samples A, B, and C versus (a) total dose and (b) annealing time.

At the end of the total dose irradiation experiments, we selected samples B whose threshold voltages had not changed obviously to carry out an SEE experiment. Figure 6 shows the safe operating area of samples B. From the figure we can see that in the worst bias condition ($V_{GS} = -15$ V, $V_{DS} = 100$ V), the devices do not have the SEGR. Our preliminary view is

that the power VDMOS devices with suitable thickness ratios of composite SiO_2–Si_3N_4 films have good SEGR-hardened ability. In fact, we tested the electrical parameters of the devices. Experimental results show that the threshold voltage and the on-state resistance change slightly, whereas the breakdown voltage and the leakage current change greatly, as shown in Table 1.

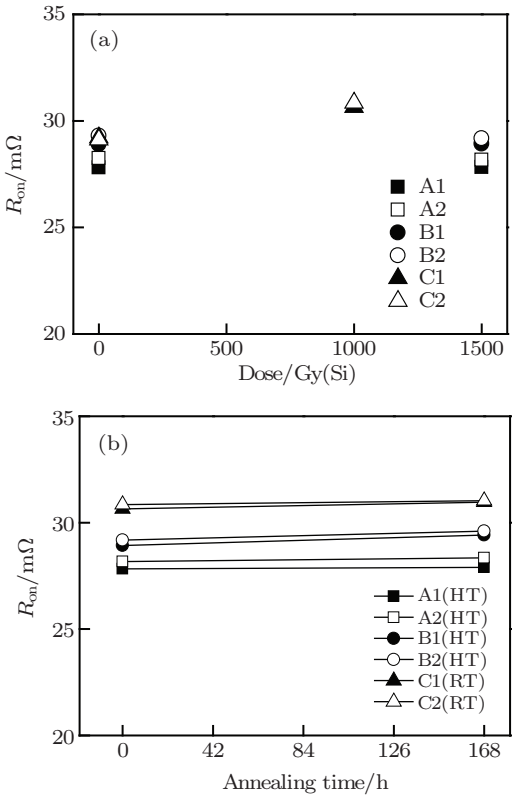


Fig. 5. (color online) On-state resistances of samples A, B, and C versus (a) total dose and (b) annealing time.

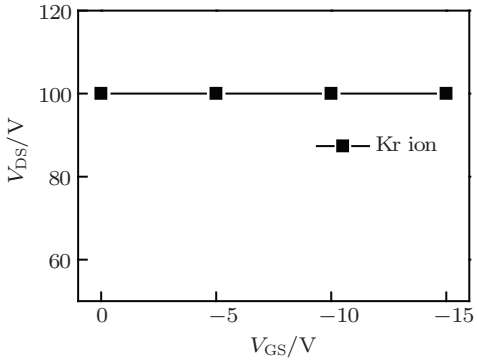


Fig. 6. Single event effect safe operating area of samples B.

Table 1. Static parameters of samples B before and after irradiation.

	$V_{dss(b)}$/V	$V_{GS(th)}$/V	$R_{DS(ON)}$/mΩ	I_{DSS}/mA
Before	133.00	3.03	30.37	1.99×10^{-6}
After	0.48	2.67	30.10	24.16

4. Results and discussion

In Fig. 7, an energy band diagram for an MNOS film at equilibrium is shown. Meanwhile, in Fig. 8, an energy band diagram for an MNOS structure during irradiation with positive bias on the gate and the corresponding electron–hole motion is shown.

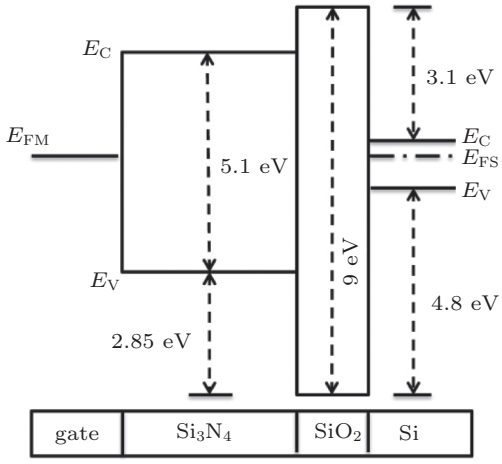


Fig. 7. Energy band diagram for MNOS structure at equilibrium.

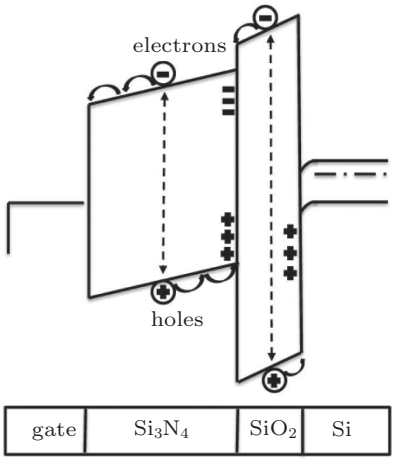


Fig. 8. Energy band diagram for MNOS structure during irradiation with positive bias on the gate and corresponding electron–hole motion.

During the total dose irradiation, the electron–hole pairs are created in the SiO_2 and Si_3N_4 layers. If the gate voltage is positive, the holes generated in the SiO_2 layer will transport to the Si–SiO_2 interface and should be captured by the traps. The electrons generated in the SiO_2 layer will transport to the SiO_2–Si_3N_4 interface and be swept to the Si_3N_4 layer easily because no electron barrier exists at the SiO_2–Si_3N_4 interface.[15] At the same time, electron–hole pairs are generated in the Si_3N_4 layer during irradiation. Because of the large density and capture cross section of both electron and hole traps in the Si_3N_4 layer, most of them will be trapped near their generation sites.[15] However, some of the holes generated in the Si_3N_4 layer will transport to the SiO_2–Si_3N_4 interface and accumulate there because of the hole barrier at the interface. Some of them will recombine with the electrons from SiO_2, and the others will be captured by the traps at the interface.[15]

Most of the electrons generated in the Si_3N_4 layer during irradiation will be swept out of the Si_3N_4 layer under the electric field. The trapped charge in the Si_3N_4 layer can be considered as a sheet charge with an effective areal charge density Q_{ni} projected to the SiO_2–Si_3N_4 interface. Similarly, the trapped charge in the SiO_2 layer can be represented as a sheet charge with an effective areal charge density Q_{ox} projected to the Si–SiO_2 interface.[15] The threshold-voltage shifts under positive bias during irradiation will be discussed here.[15,16] The threshold voltage shift can be expressed as

$$\Delta V_T = -Q_{ox} \times \left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_{ni}}{\varepsilon_{ni}} \right) - Q_{ni} \times \frac{t_{ni}}{\varepsilon_{ni}}, \quad (1)$$

where t_{ox} is the thickness of the SiO_2 layer, t_{ni} is the thickness of the Si_3N_4 layer, ε_{ox} is the permittivity of the SiO_2 layer, ε_{ni} is the permittivity of the Si_3N_4 layer, Q_{ox} is the trapped hole charge near the Si–SiO_2 interface, and Q_{ni} is the trapped charge near the SiO_2–Si_3N_4 interface. We know that the total number of holes generated in the SiO_2 and escaped initial recombination is proportional to the oxide thickness and the total dose. In the experiment, the thicknesses of the SiO_2 layers in all samples are the same, and they absorb the same dose. Therefore, we can assume that the threshold voltages of the three groups of samples have the same negative drift due to the holes captured in the SiO_2 interface. The threshold voltage shift differences of samples are mainly due to different Si_3N_4 thicknesses in the composite films.

According to Refs. [15] and [16], the small number of holes calculated here suggests that only a small percentage of the holes (3%) are trapped at the SiO_2 layer. In contrast to this, most electrons generated in SiO_2 (78%) are transported to the SiO_2–Si_3N_4 interface and trapped at the interface. We also see that the number of electron–hole pairs generated per unit dose in Si_3N_4 is larger than that in SiO_2 by 17% to 75%.[17] Only a small fraction of the holes (12.5% in the best case) generated in the Si_3N_4 layer will contribute to the threshold voltage shift.[15,16]

For samples A, the net trapped negative charge in the SiO_2–Si_3N_4 interface is less than the net trapped positive charge in the Si–SiO_2 interface, so the threshold voltage exhibits a negative drift. But the extent of the drift is far less than that of pure SiO_2 film. For samples B, the net trapped negative charge in the SiO_2–Si_3N_4 interface is slightly less than the net trapped positive charge in the SiO_2 interface, so the threshold voltage also exhibits a negative drift. However, the drift is much smaller than that for samples A. Because of the thicker Si_3N_4 layer, the number of electron–hole pairs induced by irradiation is greater. The net number of trapped negative charge in the SiO_2–Si_3N_4 interface increases, but is slightly smaller than the number of trapped holes in the Si–SiO_2 interface. For samples C, the Si_3N_4 is far thicker than the SiO_2, therefore, the net trapped negative charge in the SiO_2–Si_3N_4 interface is much greater than the net trapped positive charge in the Si–SiO_2 interface. All of them lead to a positive drift of the threshold voltage.

From Fig. 3 we can see that the breakdown voltage does not change significantly, as expected. For all samples, we only change the thickness and the structure of the gate oxide layer, while we do not change the thickness of the epitaxial layer related to the breakdown voltage. The on-state resistance of the samples changes with the accumulated dose, as shown in Fig. 4. The on-state resistance is almost independent of the accumulated dose. In the total dose irradiation experiment, we can see that the threshold voltage shifts of the samples with different thickness ratios of films change differently with the accumulated dose. Some samples exhibit positive shifts, while others have negative drifts. And the drift extents of the threshold voltages are not the same.

At the end of the total dose experiments, we selected a group of samples (B-type power VDMOS devices) with the smallest threshold voltage shifts to carry out the SEE experiment, and the experimental results are shown in Fig. 6. Under the worst bias condition ($V_{GS} = -15$ V, $V_{DS} = 100$ V), the samples have no SEGR effect. The SEGR is caused by the heavy ion induced localized rupture of the gate oxide. In Fig. 9, a VDMOS device is shown with an incident ion track in the gate–drain neck region. Under appropriate bias conditions, the accumulation of charge (generated by the heavy ions) in the silicon at the Si–SiO_2 interface in the neck region can result in sufficiently high electric fields across the gate oxide to cause a localized gate rupture.[8]

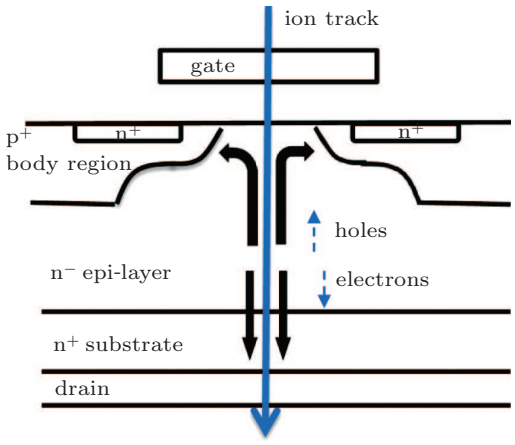


Fig. 9. (color online) Path schematic diagram of the particles in VDMOS device.

The critical electric field to cause the oxide localized gate rupture is greater for the device with a thicker gate oxide layer. From the previous discussion, we know that because the permittivity of Si_3N_4 is greater than that of SiO_2, the composite SiO_2–Si_3N_4 films can be thicker than the pure SiO_2 films but

still have the same charge storage capability. The composite SiO_2–Si_3N_4 films are thicker than the pure SiO_2 films, but the sensitivity of the power VDMOS devices to the total ionizing dose is not increased. Therefore, we have a good way to solve both the SEGR and the total ionizing dose problems with the composite SiO_2–Si_3N_4 films, and improve the SEGR-hardened ability of the power VDMOS devices.

From Table 1, we see that although the SEGR does not occur to the samples in the SEE irradiation, the electrical parameters change significant after irradiation. The incident ions pass through the gate oxide layer to generate electron–hole pairs. The holes generated in the SiO_2 layer will transport to the Si–SiO_2 interface and be captured by the traps, leading to a negative shift of the threshold voltage. Our preliminary view is that the holes captured at the Si–SiO_2 interface form oxide positive charge. The oxide positive charge induces charge in the p–n junction near the surface of the terminal structure, resulting in the reduction of the breakdown voltage and the increase of the leakage current. Here, we have not discussed in detail the reasons for the parameter changes.

5. Conclusion

In this paper, we study the total dose effects and the single event effects of the power VDMOS devices with three groups of differently structured composite SiO_2–Si_3N_4 films. We explore the threshold voltage shift following the accumulated dose changes with reference to the samples with different thickness ratios. The power VDMOS devices with appropriate thickness ratios of SiO_2–Si_3N_4 films have the better anti-total dose ability and SEGR-hardened level. We may solve both the SEGR and the total ionizing dose problems with the composite SiO_2–Si_3N_4 films. The experimental results provide technical support for future designs of power devices to improve the radiation level.

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