The supply voltage scaled dependency of the recovery of single event upset in advanced complementary metal–oxide–semiconductor static random-access memory cells*

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Using computer-aided design three-dimensional simulation technology, the supply voltage scaled dependency of the recovery of single event upset and charge collection in static random-access memory cells are investigated. It reveals that the recovery linear energy transfer threshold decreases with the supply voltage reducing, which is quite attractive for dynamic voltage scaling and subthreshold circuit radiation-hardened design. Additionally, the effect of supply voltage on charge collection is also investigated. It is concluded that the supply voltage mainly affects the bipolar gain of the parasitical bipolar junction transistor (BJT) and the existence of the source plays an important role in supply voltage variation.

Keywords: single event upset, multi-node charge collection, recovery, ultra-low ower voltage

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1. Introduction

With device feature sizes scaling down due to very-large-scale integration (VLSI), charge sharing has become a major single event effect (SEE) issue because of the reduced nodal charge and space between devices.[1–5] Static random access memories (SRAMs) are ubiquitous in modern integrated circuits (ICs), and SRAM is more prone to soft errors because of the larger sensitive volume (SV) and lower node capacitance than its dynamic counterpart.[6] In addition, the soft error rate (SER) in SRAM increases as the technology shrinks.[7,8] As SRAM cells are scaled down in size, a new effect, a different mechanism for SRAM single event upset (SEU) due to indirect charge collection, was observed.[9,10] Qin *et al*.[10] used technology computer-aided design (TCAD) simulations to demonstrate that the SRAM design upsets with less charge deposition, but then recovers to the original state when linear energy transfer (LET) is much larger.

Low power consumption circuits have been used in military and space equipment and implanted medical devices, where the availability of power may be severely limited.[11] Dynamic voltage scaling (DVS) and subthreshold circuits, which operate at a lower supply voltage than the threshold voltage, are expected to be used for ultralow power applications. However, because of lower electric fields and supply currents, soft errors become a main concern for DVS and subthreshold circuits.[12,13] An increase in the radiation susceptibility of SRAM with supply voltage decreasing is observed in Ref. [14], but the feature size is greater than 0.18 μm. Recently, Fuketa *et al*.[12] studied the measurement results of alpha particle-induced soft errors and multiple cell upsets (MCUs) in 65-nm 10T SRAM in a range of supply voltage from 1.0 V to 0.3 V. It revealed that the soft error rate (SER) at 0.3 V is eight times higher than that at 1.0 V, but the charge sharing effect was weak because of the low energy of the alpha particle being used. Reference [13] reported on the transients generated on a bulk 130-nm three-dimensional (3D) TCAD device increase considerably with supply voltage decreasing. Most of the previous work on power supply voltage mainly focused on SRAM cells[12–14] but without considering the charge sharing effect, which cannot be ignored in sub-130-nm technology.

However, to our best knowledge, no studies have been conducted that include the effects of ultra-low supply voltage on the recovery of SRAM and charge sharing. In this paper, 3D device simulations are performed in a power supply voltage range of 0.8 V–1.6 V in 90-nm complementary metal–oxide–semiconductor (CMOS) technology. The effects of supply voltage on the recovery of SRAM and charge sharing are evaluated. Simulation results are discussed and the mechanism of the supply voltage dependency will be explained.

2. Description of the recovery mechanism

A commercial SRAM cell is shown in Fig. 1, which consists of six transistors, two cross-coupled inverters, and two access pass-gate transistors. A 3D device/circuit mixed mode is constructed using Synopsys TCAD, where P1 and P2 use a 3D TCAD model while the other transistors use SPICE models. The unhardened SRAM cell is fabricated in 90-nm CMOS bulk technology, which is the same as that in Ref. [15]. The

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doping profiles are calibrated within the 3D model by processing simulation and an inverse modeling approach,[16] and are in good agreement with the I–V characteristics obtained from the TCAD and SPICE simulations. The 3D dual-PMOS model is shown in Fig. 2, in which the width values obtained from PMOS1 and PMOS2 are both 0.84 μm, the width values of N-well contact and N-well are 0.12 μm and 2.15 μm, respectively. Additionally, the width values of the corresponding N1 and N2 in Fig. 1 are both 0.4 μm.

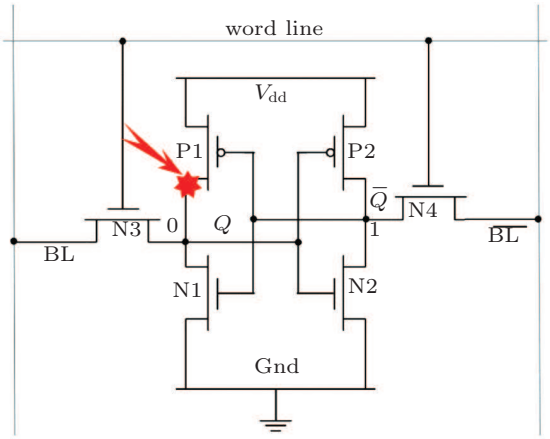


Fig. 1. (color online) A commercial SRAM cell.

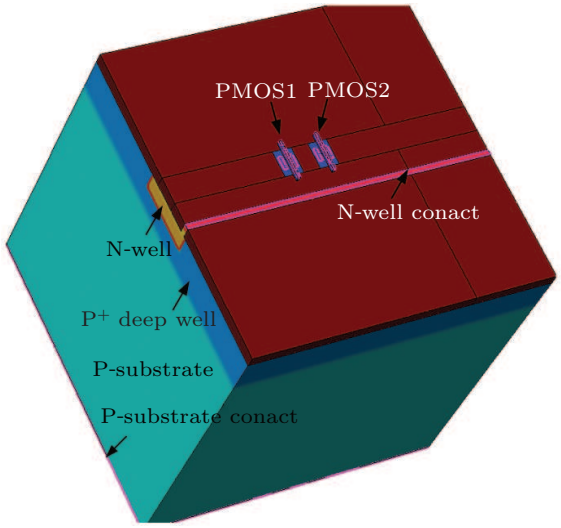


Fig. 2. (color online) A 3D dual-PMOS model for 90-nm bulk CMOS.

Assume that the storage state of Q is low. First, let P1 be off and P2 be on. If a particle strikes the drain of off-state P1, the logic low state at Q is driven to high due to the charge collection. Figure 3 shows the voltage pulses of Q at different LETs of striking particles. With the increase of LET, the design SRAM presents the SEU, but the storage state can recover to low when LET is large enough.

It is found that multi-node charge collection is the key contributor to the recovery mechanism. The SRAM cells with strong charge sharing should exhibit a strong recovery effect and can reduce the dependence of SER on LET. That is, SRAM cells with increased charge sharing should exhibit a weaker LET dependence on SER.

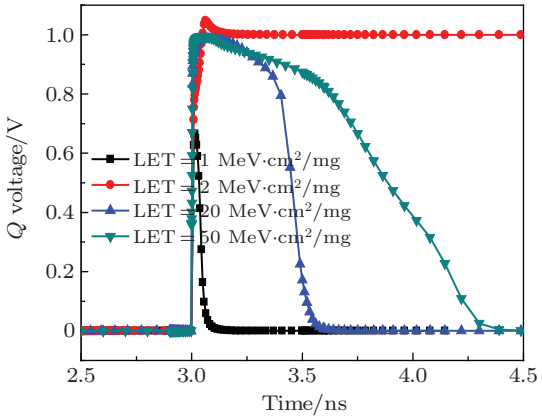


Fig. 3. (color online) Voltage pulses of Q at different LETs of striking particles.

For all simulations, the following physical models are used: (i) Fermi–Dirac statistics; (ii) band-gap narrowing effect; (iii) doping-dependent SRH recombination and Auger recombination; (iv) effects of temperature, doping, electric field, and carrier–carrier-scattering on mobility; (v) incident heavy ions that are modeled by using a Gaussian radial profile with a characteristic $1/e$ radius of 30 nm and a Gaussian temporal profile with a characteristic decay time of 0.5 ps. All simulations are conducted by using the YINHE computing cluster at the Computer Centre of the National University of Defense Technology.

3. Power voltage scaled dependency of the recovery of SEU

The upset LET threshold is the smallest LET causing an SRAM cell to upset. We here define the recovery LET threshold as the smallest LET for SRAM to recover again after the upset. According to the above illustrations, it is known that the storage state of SRAM can only maintain the opposite state when LET is larger than upset threshold and is smaller than the recovery threshold. Table 1 shows the upset and recovery LET threshold at different values of power supply voltage (V_{dd}) for several transistor spacings. Only the spacing between P1 and P2 in Fig. 1 is changed and the rest of the simulation parameters are kept unaltered. It can be seen that the upset LET threshold remains the same for different spacings, while the recovery LET threshold is proportional to transistor spacing for a certain V_{dd}. It reveals that the upset threshold decreases with the supply voltage reducing and keeps constant with the layout spacing changing, which has been illuminated by previous studies.[10,12,14] Taking 0.14 μm for example, when V_{dd} decreases from 1.6 V to 0.8 V, the upset threshold decreases from

5 MeV·cm^2/mg to 2 MeV·cm^2/mg and the recovery threshold decreases from 10 MeV·cm^2/mg to 7 MeV·cm^2/mg. The recovery threshold decreases with the V_{dd} reducing for a certain spacing, which is quite attractive to the DVS and subthreshold circuit radiation-hardened design, because a lower recovery LET threshold means that the circuits can recover from the metastable state more easily. This new conclusion will be explained by in-depth analysis in the following section.

Table 1. Upset thresholds and recovery thresholds of SRAMs for different spacings.

Spacing/μm	Upset LET threshold/MeV·cm^2/mg			Recovery LET threshold/MeV·cm^2/mg		
	$V_{dd} = 0.8$ V	$V_{dd} = 1.0$ V	$V_{dd} = 1.6$ V	$V_{dd} = 0.8$ V	$V_{dd} = 1.0$ V	$V_{dd} = 1.6$ V
0.14	2.0	2.5	5.0	7.0	8.0	10.0
0.5	2.0	2.5	5.0	18.5	19.0	24.0
1.0	2.0	2.5	5.0	36.0	37.0	41.5
1.5	2.0	2.5	5.0	64.5	66.0	70.0

4. Discussion

Since multi-node charge collection plays a key role in the recovery,[10] it can be concluded that the relationship between recovery threshold and V_{dd} must be caused by the changing of charge collection with V_{dd} decreasing.

4.1. Variation of charge collection with supply voltage

In Fig. 4, the charges collected by the active and the passive device for different supply voltages are plotted. The change trends are almost the same for the active and passive PMOS, but the difference between charges collected (or injected) by the active and passive PMOS is much larger in higher V_{dd} than in lower V_{dd}. At very large supply voltage, the parasitical bipolar amplification can be enhanced sufficiently and large number of electrons (holes) will be collected (injected) by the active PMOS source. When the supply voltage is low, the parasitical bipolar junction transistor (BJT) cannot be turned on and the active PMOS source collects (injects) a few charges only, which is close to the charges collected by the passive PMOS.

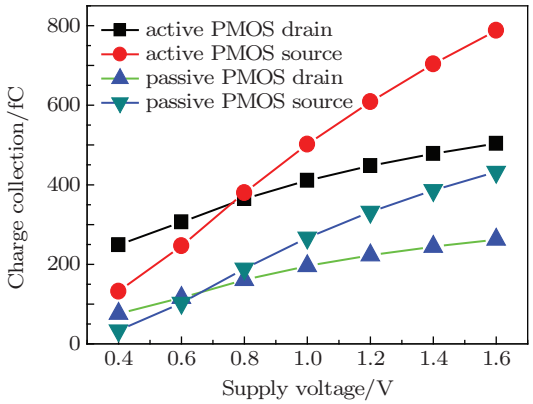


Fig. 4. (color online) Charge collections by the active and the passive device at different supply voltages.

To gain an insight into the dependence of an SET current component on power supply voltage, we investigate the quantity of charges collected by a single off-state PMOS versus supply voltage, in which the gate and source are connected to V_{dd} and the drain is grounded. Figure 5 shows the charges collected by a single PMOS and a diode for different supply voltages. For the PMOS transistor, the collected charge quantity is higher than that in the diode. We can conclude that the supply voltage mainly affects the bipolar amplification of SET components. The bipolar gain as a function of the supply voltage is shown in Fig. 6. The bipolar gain, beta, decreases from 3.2 to 1.4 when the supply voltage reduces from 1.6 V to 0.4 V.

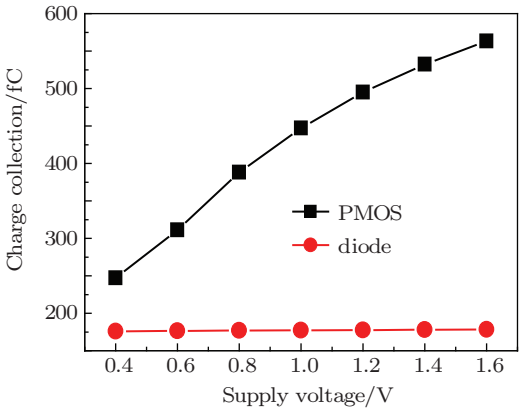


Fig. 5. (color online) Charges collected by a single PMOS and a diode.

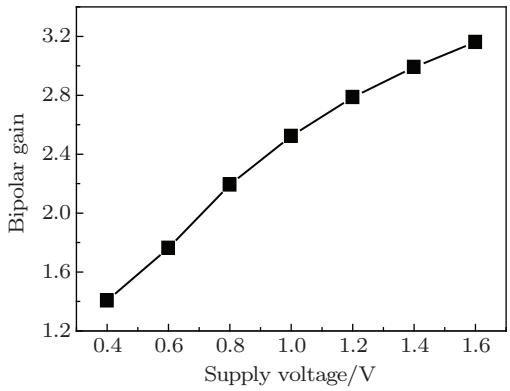


Fig. 6. Bipolar gain versus power supply voltage.

The beta value increases proportionally to the supply voltage, except at very high voltage where a slight bending of the curve

indicates that a high injection phenomenon occurs. This is due to the high electric field produced by the large power supply voltage which tends to collapse the potential barrier between the source and the drain, and thus enhances the charge amplification.

4.2. Variation of strength of quenching with supply voltage

The recovery of the SRAM cell is similar to the quenching effect in inverter chains,[17,18] except that the two inverters in 6-T SRAM cell are cross-coupled. Because the P2 in the second stage inverter will turn off when the SET pulse produced at Q arrives at the next inverter, thus it will start to collect charges and produce an SET pulse at $\bar{Q}$. The more the charges collected by the $\bar{Q}$ node, the wider the SET pulse at the $\bar{Q}$ node is, so the storage state at the Q node will be corrected more easily.

In order to investigate the relationship between V_{dd} and the SET pulsewidth produced at the $\bar{Q}$ node, the same transistors and hit location are used, but set P1 is on while P2 is off. In this case, the resulting SET at $\bar{Q}$ node is induced by charges sharing only. Figure 7 shows the SET waveforms of $\bar{Q}$ node at two different supply voltages when P1 is on. It can be seen that the SET pulsewidth for 0.8 V is larger than that for 1.6 V. By analysis, the passive PMOS drain will collect charges and raise the drain potential after striking P1, but the charges collected would discharge by the complementary on-state N2 at the same time, thus the rise time is determined by these two competing mechanisms. For lower supply voltage, the discharge current is smaller and transition time from low to high is faster, and the rise time reduces and pulsewidth increases. Consequently, the recovery ability of SRAM cells will increase with the supply voltage decreasing, which is the reason why the recovery threshold decreases with V_{dd} reducing for a certain spacing in Table 1.

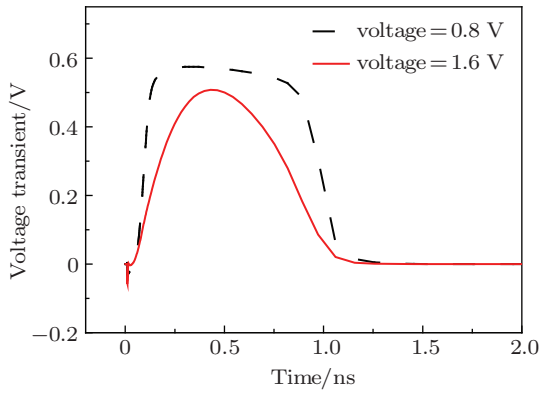


Fig. 7. (color online) The SET waveforms of the $\bar{Q}$ node at two different supply voltages when P2 is on.

5. Conclusion

Based on 90-nm bulk CMOS technology, the supply voltage scaled dependency of the recovery of SEU and charge collection in SRAM cells is investigated using TCAD 3D simulation. It reveals that the recovery LET threshold decreases with the supply voltage reducing for a certain layout spacing. For the minimization rule of layout spacing, the recovery threshold decreases from 10 MeV·cm^2/mg to 7 MeV·cm^2/mg when V_{dd} decreases from 1.6 V to 0.8 V, which is quite attractive to DVS and subthreshold circuit radiation-hardened design. For lower supply voltage, the discharge current of the opposite inverter is smaller and the transition time from low to high is faster, and the rise time reduces and pulsewidth increases. It rectifies the pessimistic conclusion that ultra-low power applications are susceptive to particle strike. Furthermore, the effect of supply voltage on charge collection is also investigated. It is concluded that the supply voltage mainly affects the bipolar gain of parasitical BJT and the existence of the source plays an important role in the supply voltage variation.

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