The temperature dependence of single-event transients in 90-nm CMOS dual-well and triple-well NMOSFETs*

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This paper investigates the temperature dependence of single-event transients (SETs) in 90-nm complementary metat–oxide semiconductor (CMOS) dual-well and triple-well negative metal–oxide semiconductor field-effect transistors (NMOSFETs). Technology computer-aided design (TCAD) three-dimensional (3D) simulations show that the drain current pulse duration increases from 85 ps to 245 ps for triple-well but only increases from 65 ps to 98 ps for dual-well when the temperature increases from −55 °C to 125 °C, which is closely correlated with the NMOSFET sources. This reveals that the pulse width increases with temperature in dual-well due to the weakening of the anti-amplification bipolar effect while increases with temperature in triple-well due to the enhancement of the bipolar amplification.

Keywords: single event transient, temperature dependence, dual-well, triple-well, N^+ deep well

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1. Introduction

Excess carriers are created in silicon bulk when heavy ions cross semiconductor devices and are collected by sensitive nodes, forming a single event transient (SET). This is the main radiation-induced noise and the source of soft errors in advanced complementary metat–oxide semiconductor (CMOS) integrated circuits (ICs).[1–4] The parameters that determine the transient pulse shape, such as charge generation and collection processes after particles strike, are strong functions of operating temperature. Thus, for circuits and devices operating in extreme environments, temperature is an important factor in radiation hardening. Heavy ion tests and technology computer-aided design (TCAD) simulations show that SET pulse width increases significantly with temperature in bulk CMOS technologies, which is mainly caused by the enhancement in the parasitic-bipolar action at elevated temperatures.[5–7]

Dual-well CMOS technology comprises p-wells in a p-substrate with a buried p+ deep well (Fig. 1(a)). A P^+ deep well has little effect on the *I*–*V* characteristics of the device, but it can reduce the effects of substrate disturbance on well potential. Triple-well CMOS technology comprises p-wells that are contained in a buried n+ deep well in a p-substrate (Fig. 1(b)). Triple-well technology reduces substrate-noise coupling in analog radio frequency (RF) and mixed signal circuits by isolating the p-well from the p-substrate.[8] The additional junction capacitances in triple-well structures can get lower drain-bulk series capacitance than dual-well structures in low noise amplifiers.[9]

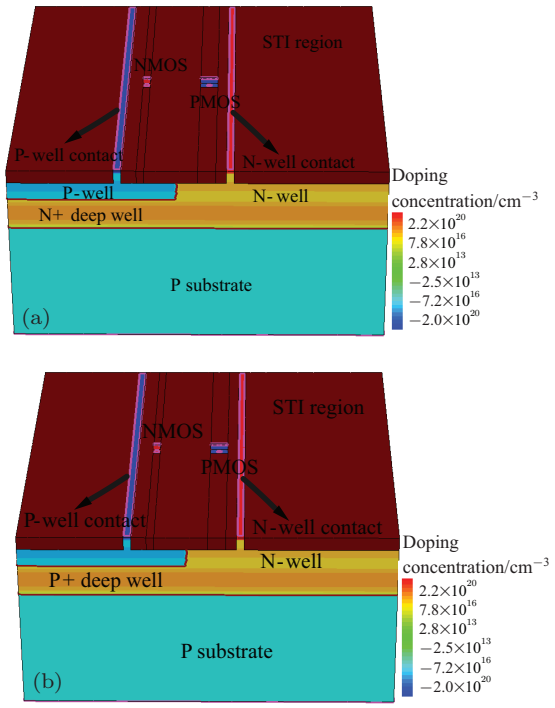


Fig. 1. (color online) An inverter in 90-nm dual-well and triple-well CMOS technology: (a) dual-well MOSFETs and (b) triple-well MOSFETs.

Previous studies mainly focus on the SET in dual-well bulk positive channel metal–oxide semiconductor field-effect transistors (PMOSFETs) and silicon-on-insulator (SOI) devices at elevated temperatures,[5–7] or the SET characteristic in a triple-well situation without considering temperature dependence.[8,10] The mechanisms affecting charge collection include drift, diffusion, and bipolar amplification, and bipolar amplification is especially sensitive to temperature. The par-

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asitic structures for dual-well and triple-well NMOSFETs are quite different, which will affect the bipolar amplification effect directly, thus affecting the SET pulse width and soft error rate (SER) in circuits. Hence, it is necessary to examine the temperature dependence of SET in dual-well and triple-well MOSFETs. In this paper, the impact of temperature on charge collection and SET pulse width are calculated. Simulation results will be discussed and the mechanism of temperature dependency will be explained.

2. Simulation setup

Device simulation is one of the effective means to study the generation and propagation of an SET pulse. In this paper, Synopsys TCAD three-dimensional (3D) simulation is employed to study the characteristics of the SET generated in an inverter. The 90-nm CMOS bulk technology used in this paper is the same as in Ref. [11]. Device model parameters are consistent with other transistor models in which the same technology is used. The doping profiles are calibrated within the 3D model by process simulation and an inverse modeling approach,[12] and are consistent with the I–V characteristics between TCAD and SPICE simulations, as shown in Fig. 2.

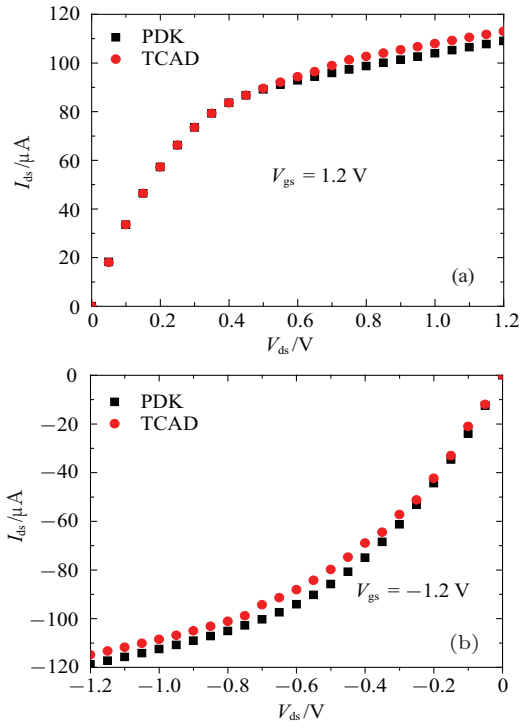


Fig. 2. (color online) I_D–V_D curves of the TCAD model versus the SPICE model: (a) NMOS; (b) PMOS.

The NMOSFET and PMOSFET are constructed on the same wafer, as shown in Fig. 1, where the width is 200 nm for the negative metal-oxide semiconductor (NMOS) and 480 nm for the positive metal–oxide semiconductor (PMOS). The depth of the deep well is 820 nm. Gaussian distribution is presented for the deep well concentration, and the peak value is $1 \times 10^{18}/\text{cm}^3$.

The following physical models are used: (i) Fermi–Dirac statistics; (ii) band-gap narrowing effect; (iii) doping-dependent Shockley-Read-Hall (SRH) recombination and Auger recombination; (iv) temperature, doping, electric field, and carrier–carrier-scattering impacts on mobility; (v) incident heavy ions, which are modeled using a Gaussian radial profile with a characteristic $1/e$ radius of 30 nm and a Gaussian temporal profile with a characteristic decay time of 0.5 ps. All simulations are conducted on the YINHE high performance computing cluster, and each case will cost about 8 hours at a single compute node.

3. Role of the source in dual-well and triple-well NMOSFETs

The location of the heavy ion strike is the center of the NMOSFET's drain, which is the most sensitive location for striking the device, and the normally incident ion linear energy transfer (LET) is fixed at 10 MeV · cm^2/mg. The temperature used in the TCAD is 300 K. The same simulation setup is used for both the dual-well and triple-well. The SET drain voltage and SET source current are shown in Figs. 3 and 4 for dual-well and triple-well, respectively.

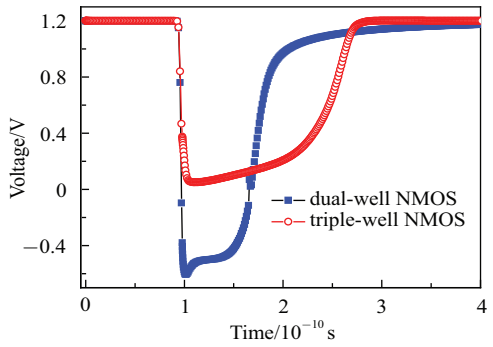


Fig. 3. (color online) Drain voltage versus time for dual-well and triple-well for an NMOS hit.

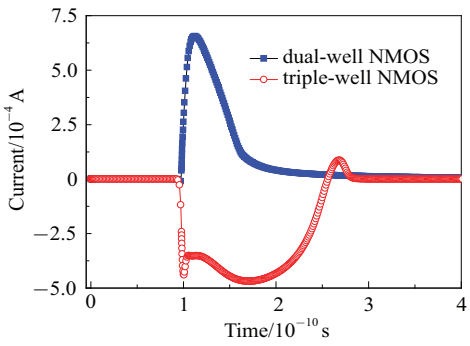


Fig. 4. (color online) Source current versus time for dual-well and triple-well for an NMOS hit.

It is clear from Fig. 3 that the pulse width for the triple-well is about twice that of the dual-well for striking an NMOS device. Since the SET pulse width is the most important factor

to predict SER in circuits, the mechanism for these phenomena should be investigated carefully. In Fig. 4, the source current for the dual-well is positive while it is negative for the triple-well, which means the NMOSFET source collects electrons (or injects holes) in the dual-well and injects electrons (or collects holes), so the contribution of the NMOS source to drain voltage is totally opposite for the dual-well and the triple-well. It can be found that the largest source current appears when the drain voltage is at its lowest, not only for the dual-well but also for the triple-well.

In order to investigate the mechanism in depth, we plotted the electron flow direction 50 ps after strike for the dual-well and the triple-well, as shown in Fig. 5. A reversed P–N junction will be formed by the source and p-well for the dual-well, which helps to collect electrons created by the heavy ion (Fig. 5(a)). For the triple-well, because of the existence of the N^+ deep well, the source p-well junction will forward and source inject a large amount of electrons into the p-well (while collects holes), most of which will be collected by drain (Fig. 5(b)), thus a bipolar amplification effect appears. In short, the source in the dual-well weakens the charges collected by the drain, while in the triple-well it enhances the charges collected by the drain. Consequently, the SET pulse width for the triple-well is larger than that for the dual-well.[8]

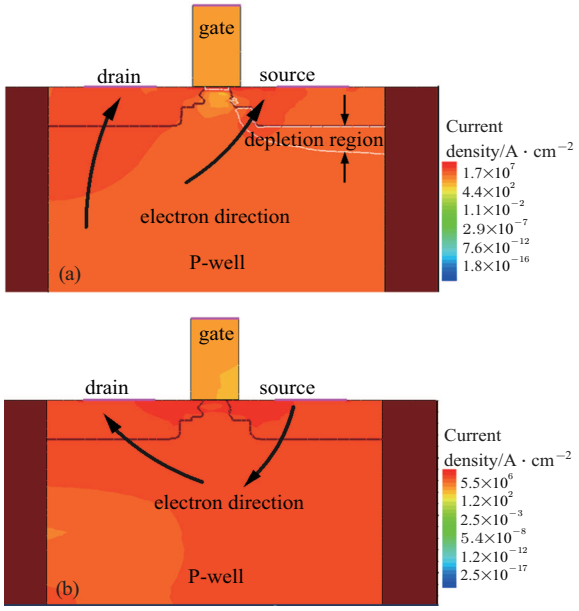


Fig. 5. (color online) The flow direction of electrons for dual-well and triple-well NMOSFETs 50 ps after a heavy ion strike: (a) dual-well; (b) triple-well.

4. Temperature dependence of an SET in a dual-well and a triple-well

Onboard temperature usually ranges widely from less than −55 °C to higher than 125 °C in a space environment, which makes temperature an important factor in radiation hardening. The temperature in our study was varied from

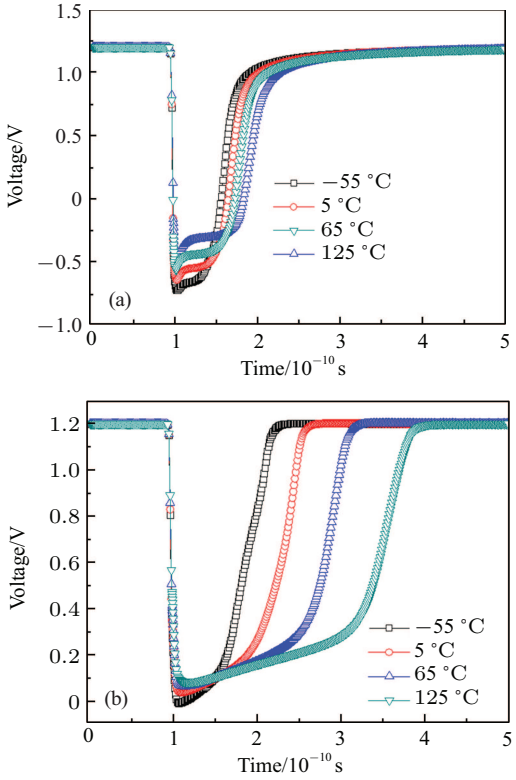


Fig. 6. (color online) The SET voltage pulse shape for striking an NMOS at four different temperatures: (a) in the dual-well; (b) in the triple-well.

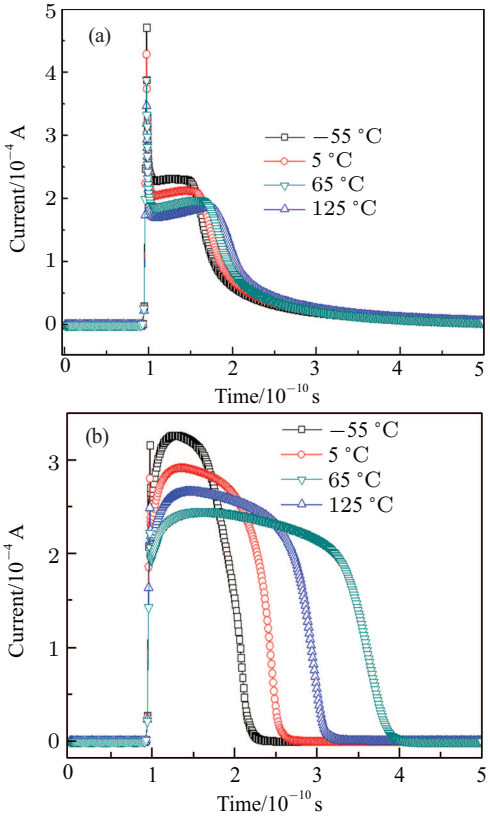


Fig. 7. (color online) The drain current pulse shape for striking an NMOS at four different temperatures: (a) in the dual-well; (b) in the triple-well.

−55 °C to 125 °C. For the simulations, temperature-dependent physical models were used. Figure 6 shows the SET voltage pulse shape for striking an NMOS at four different temperatures in the dual-well and the triple-well, showing an increase in pulse width from 65 ps to 98 ps for the dual-well and from 85 ps to 245 ps for the triple-well as the temperature increases from −55 °C to 125 °C. The corresponding drain SET current pulse is shown in Fig. 7, which is consistent with the change trend of the drain voltage pulse. Figure 8 gives the SET voltage pulse width versus temperature for the dual-well and the triple-well, respectively. SET pulse width in the triple-well obviously manifests much stronger temperature dependence than in the dual-well.

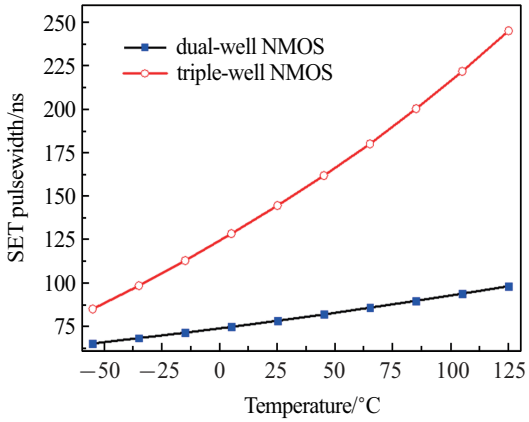


Fig. 8. (color online) The SET pulse width versus temperature for the dual-well and the triple-well.

5. Discussion

SET pulse is determined by the charge collection at the drain node. In order to investigate the different relationship between pulse width and temperature in dual-well and triple-well, we plot the charge collected at different temperatures by the NMOS drain in the dual-well and the triple-well, shown in Fig. 9. It can be seen that the charge collected in the dual-well remains nearly constant while charge increases linearly with temperature in the triple-well. By the analysis in Section 3, this difference must be caused by the existence of the NMOS source, because the source of the NMOSFET collects electrons (or injects holes) in the dual-well while it injects electrons (or collects holes). Table 1 gives the charges collected by the drain and the source of the NMOS in the dual-well and the triple-well for a temperature range from −55 °C to 125 °C. The charge collected by the NMOS source in the dual-well decreases from 34.17 fC to 31.95 fC, just a very little change, when temperature increases from −55 °C to 125 °C. However, the source injects the charges in the triple-well and the charges increase from 16.34 fC to 110.39 fC, enhanced by four times.

The mobility of carriers will be dominated by lattice scattering with increasing temperature, which decreases the mobility and increases the resistance in silicon. The parasitic resistance from p-well contact to bulk can be divided into a vertical part and a horizontal part, and the vertical part is in parallel connection with the parasitical diode composed of the source and the p-well. The voltage drop on this diode is determined by the value of the resistance, and larger resistance leads to a larger voltage drop. For the dual-well, the increased voltage weakens the reversed state of the parasitical diode, and reduces the reversed current and charge collected by the source, thus the charges collected by the drain increase a little due to the reduction collected by source. For the triple-well, the parasitical diode is forward and the increased voltage enhances the bipolar amplification effect, and the charges collected by drain are enhanced a lot because the current increases exponentially with the forward voltage. Some of the electrons injected to the p-well recombine with holes, and others are collected by the drain of the NMOS, so the charge collected by the drain will also increase prominently with increasing temperature.

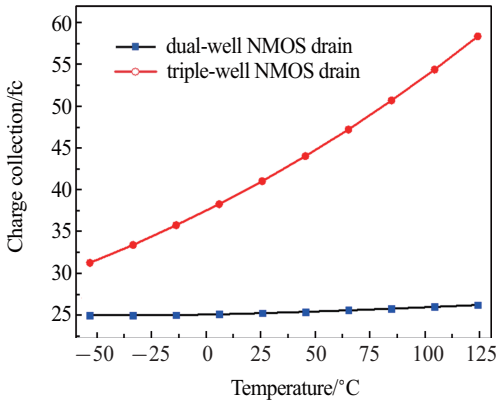


Fig. 9. (color online) The charge collection versus temperature for the dual-well and the triple-well.

Table 1. The charge collected by the drain and source of the NMOS in the dual-well and the triple-well for temperatures from −55 °C to 125 °C.

Temperature/ °C	Charge collected in the dual-well/fC		Charge collected in the triple-well/fC	
	by drain	by source	by drain	by source
−55	24.94	34.17	31.52	−16.34
−35	24.95	34.17	33.76	−26.15
−15	24.97	34.1	36.24	−36.09
5	25.06	34.1	38.89	−46.31
25	25.21	33.9	41.77	−56.53
45	25.38	33.64	44.9	−66.89
65	25.57	33.32	48.24	−77.52
85	25.78	32.92	51.89	−88.15
105	26	32.47	55.76	−99.06
125	26.24	31.95	59.93	−110.39

Also, we plot the distribution of electrostatic potential of the triple-well NMOSFET at −55 °C and 125 °C 50 ps after a heavy ion strike, as seen in Fig. 10. For −55 °C, the potential

in bulk near source-bulk junction is lower, and few electrons flow from source to bulk. For 125 °C, the bulk potential near the source-bulk junction is higher, thus many electrons flow from the source to the bulk and the drain can collect more charges than at −55 °C.

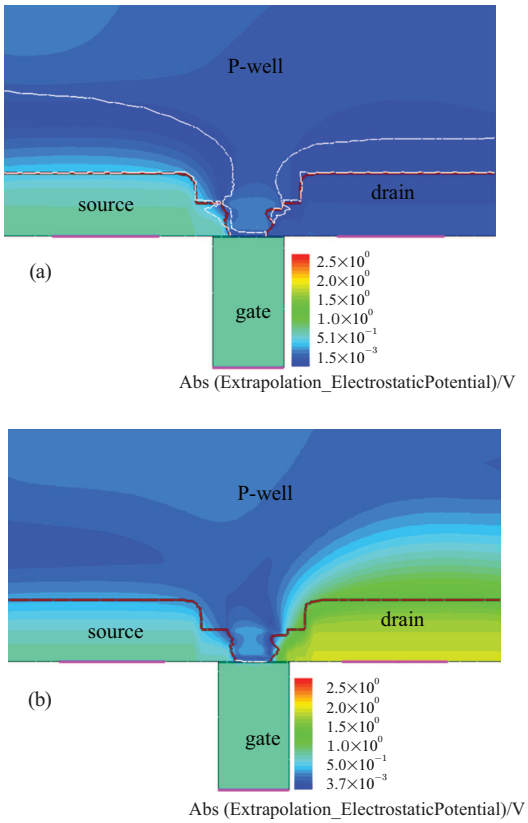


Fig. 10. (color online) The electrostatic potential distribution of the triple-well NMOSFET at different temperatures 50 ps after a heavy ion strike: (a) −55 °C, (b) 125 °C.

6. Conclusion

As the SET pulse width is the most important factor affecting SER mitigation, such variations as a function of temperature must be considered during the design for radiation hardening. The temperature dependence of SET in CMOS dual-well and triple-well NMOSFETs over temperatures from −55 °C–125 °C has been studied. It is found that the source of NMOSFETs plays an opposite role in the dual-well and the triple-well: it helps the drain to collect excess carriers in a dual-well but injects a mass of carriers to the drain in a triple-well. The pulse width increases with temperature in the dual-well due to the weakening of anti-amplification bipolar effect, while increases with temperature in the triple-well due to the enhancement of the bipolar amplification, which is also the reason why pulse width in the dual-well increases only a little while it increases a lot in the triple-well with an increase in temperature.

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