The effect of substrate doping on the flatband and threshold voltages of a strained-Si pMOSFET*

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The effect of substrate doping on the flatband and threshold voltages of a strained-Si/SiGe p metal–oxide semiconductor field-effect transistor (pMOSFET) has been studied. By physically deriving the models of the flatband and threshold voltages, which have been validated by numerical simulation and experimental data, the shift in the plateau from the inversion region to the accumulation region as the substrate doping increases has been explained. The proposed model can provide a valuable reference to the designers of strained-Si devices and has been implemented in software for extracting the parameters of a strained-Si MOSFET.

Keywords: strained-Si pMOSFET, flatband voltage, threshold voltage, doping

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1. Introduction

Silicon-based devices play a decisive role in the semiconductor industry. Scaling down the feature size has been the main method of changing the performance of Si devices. However, as the device is scaled down to nanoscale, serious challenges are posed by the materials' properties, device physics, and fabrication technologies. Such challenges have impelled researchers to look for various alternatives, and as a result, the strained-Si/SiGe (SSi/SiGe) material system has emerged.[1–5]

By inducing strain into Si, the *I*–*V* characteristic of a strained-Si/SiGe p metal–oxide semiconductor field-effect transistor (pMOSFET) is enhanced,[6–8] but its *C*–*V* characteristic is distorted. A "plateau" has been observed in the gate *C*–*V* characteristics of a strained-Si/SiGe pMOSFET, and it can shift from the inversion region to the accumulation region as doping concentration increases, as shown in Fig. 1.[9–11] The physics of the above phenomenon is due to the different flatband and threshold voltages at the SiO_2/SSi and SSi/SiGe interfaces, resulting from the special structure and the confinement of the carriers at the different interfaces.[12,13]

Recently, several models of the threshold voltages for a strained-Si pMOSFET have been proposed.[14–16] However, these models either do not take into account the holes and electrons confined at the SSi/SiGe interface, or do not consider the doping concentration in the strained-Si layer. Hence, with these theories, the shift in the plateau cannot be explained as the doping concentration increases. Most of all, these models cannot serve the *C*–*V* characteristics well.

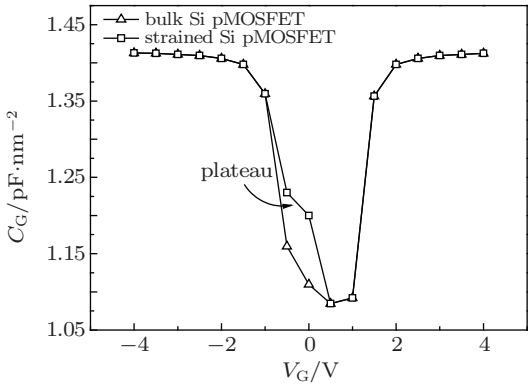


Fig. 1. Gate *C*–*V* characteristics of the strained Si and the bulk Si pMOSFET.

For this reason, the effect of substrate doping on the flatband and threshold voltages of a strained-Si/SiGe pMOSFET has been studied. By physically deriving the models of the flatband and threshold voltages, the shift in the plateau observed in the gate *C*–*V* characteristics of the strained-Si pMOSFET from the inversion region to the accumulation region as the doping concentration increases has been explained. The results from the models are validated with simulated and experimental data. The proposed models can provide a valuable reference for the design of strained-Si devices and has been implemented in software for extracting the parameters of strained-Si MOSFETs.

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2. Device structure and operation of an SSi/SiGe pMOSFET

The structure of an SSi/SiGe pMOSFET is shown in Fig. 2,[17] where G, D, B, and S represent the gate, drain, bulk, and source electrode, respectively.

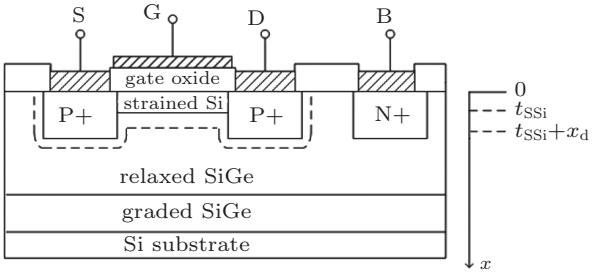


Fig. 2. Schematic diagram of an SSi/SiGe pMOSFET.

The device consists of a SiO_2 gate dielectric layer with a thickness of t_{OX}, an SSi layer with a thickness of t_{SSi}, a relaxed SiGe layer, and a graded SiGe layer. In analysis, it is assumed that the SSi layer, the SiGe layer, and the Si substrate are uniformly doped with a concentration of N_D.

When $V_G > V_{FB}^S$ (flatband voltage at the SSi surface), electrons are accumulated at the SSi/SiO_2 interface. When $V_{FB}^H < V_G \leq V_{FB}^S$, the strained-Si layer is depleted, and electrons are accumulated only in the SiGe layer. At $V_G = V_{FB}^H$ (flatband voltage at the SSi/SiGe interface), the depletion region begins to extend to the SiGe layer. We now discuss the following two cases.

(i) The lightly doped epitaxial layer case

In this case, the inversion layer first forms in the SiGe layer and then in the SSi layer. Therefore, when $V_T^H < V_G \leq V_{FB}^H$, the depletion extends into the SiGe layer and reaches its maximum width at $V_G = V_T^H$ (inversion threshold voltage of the SiGe layer). After that, with V_G getting more negative, inversion occurs in the SiGe layer. Eventually, the concentration of the holes in the SiGe layer get its maximum value at $V_G = V_T^S$ (inversion threshold voltage of the SSi layer). When $V_G < V_T^S$, the hole sheet concentration in the 2-DHG at the SSi surface increases when V_G is made increasingly negative, resulting in an increased electric field and potential drop across the strained silicon and oxide layers. Figure 3 shows the energy band diagram of the lightly doped SSi/SiGe pMOSFET for $V_G < V_T^S$.

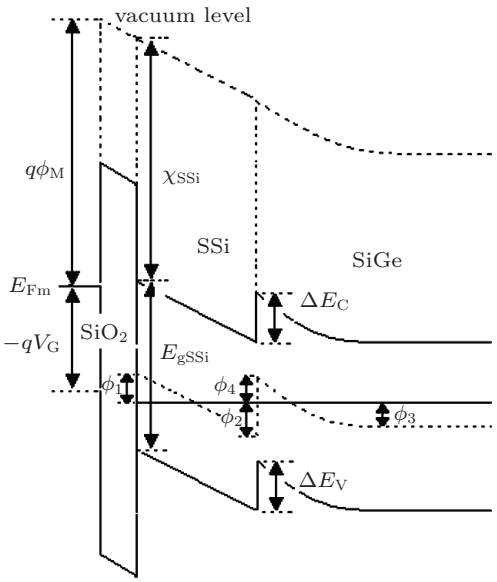


Fig. 3. Energy band diagram of the lightly doped SSi/SiGe pMOSFET for $V_G < V_T^S$.

(ii) The highly doped epitaxial layer case

In this case, there is no inversion layer formed in the SiGe layer. Therefore, when $V_{FB}^S < V_G \leq V_{FB}^H$, the depletion layer is formed in the SiGe layer, and the depletion region widens as V_G is made increasingly negative. At $V_G = V_T^S$, the depletion region reaches its maximum width, and the inversion occurs at the surface of the strained-Si layer. Figure 4 shows the energy band diagram of the highly doped SSi/SiGe pMOSFET at this condition.

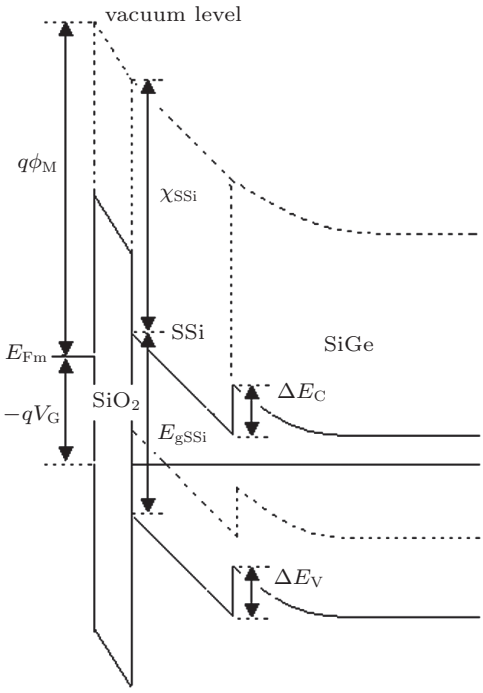


Fig. 4. Energy band diagram of the highly doped SSi/SiGe pMOSFET for $V_G < V_T^S$.

3. Model for flatband voltages and threshold voltages

3.1. Model for flatband voltages

When V_G scans from positive to negative, the flatband first occurs at the SSi surface, and then at the SSi/SiGe interface. Assuming that the interface states can be negligible, the flatband voltage at the surface of an SSi layer can be expressed

as

$$V_{\rm FB}^{\rm S} = \phi_{\rm MS} = \phi_{\rm M} - \phi_{\rm SEMI}, \tag{1}$$

where $\phi_{\rm M}$ is the work function of the gate material and $\phi_{\rm SEMI}$ is the equivalent work function of the semiconductor.

When the energy band at the SSi/SiGe interface gets flat, the gate voltage $V_{\rm G}$ becomes $V_G = V_{\rm OX} + V_{\rm FB}^{\rm S} + V_{\rm SSi}$, where $V_{\rm OX}$ is the potential dropped across the oxide layer and $V_{\rm SSi}$ across the SSi layer.

Assuming the entire SSi layer is depleted rapidly, we have

$$V_{\rm OX} = -\frac{qN_{\rm D}t_{\rm SSi}}{C_{\rm OX}}. \tag{2}$$

Solving Poisson's equation across the SSi layer, the potential $V_{\rm SSi}$ is given by

$$V_{\rm SSi} = -\frac{qN_{\rm D}t_{\rm SSi}^2}{2\varepsilon_{\rm SSi}}. \tag{3}$$

Therefore, the flatband voltage at the SSi/SiGe interface can be expressed as

$$V_{\rm FB}^{H} = V_{\rm FB}^{\rm S} - \frac{qN_{\rm D}t_{\rm SSi}}{C_{\rm OX}} - \frac{qN_{\rm D}t_{\rm SSi}^2}{2\varepsilon_{\rm SSi}}. \tag{4}$$

3.2. Model for threshold voltages

For very small drain voltages $V_{\rm D}$ and a long MOSFET channel, an analysis can be carried out in one dimension perpendicular to the surface. For negative voltages $V_{\rm G}$ applied to the gate, the silicon n-type substrate is depleted and the width of the depletion layer is denoted as $x_{\rm d}$. Depending on the gate voltage, strong inversion conditions can be induced at both the top SSi/SiGe interface and at the SSi surface or at one of them. To provide design guidelines, the conditions for channel formation are first derived.

3.2.1. Conditions for strong inversion

From the above discussions, it is known that inversion first occurs in the SiGe layer and then in the SSi layer when the epitaxial layers are lightly doped. The gate voltage that causes strong inversion at the SSi surface is denoted as the surface threshold voltage $V_{\rm T}^{\rm S}$. The condition for the onset of strong inversion is defined in a similar manner as for conventional MOS structures, as the gate voltage at which the concentration of minority carriers (holes in this case) is equal to the substrate doping concentration $N_{\rm D}$. This leads to the expression for ϕ_1 in Fig. 3 as

$$\phi_1 = \frac{KT}{q}\left(\ln\frac{N_{\rm D}}{n_{\rm i,SSi}}\right).$$

Considering the following conditions

a)

$$\phi_2 + \phi_4 = \frac{\Delta E_{\rm V} + \Delta E_{\rm C}}{2},$$

b)

$$\phi_3 = \frac{KT}{q}\left(\ln\frac{N_{\rm D}}{n_{\rm i,SiGe}}\right),$$

the condition for the threshold potential $\Phi_{\rm T}^{\rm S}$ at the surface can be expressed as

$$\Phi_{\rm T}^{\rm S} = -\left[\frac{KT}{q}\left(\ln\frac{N_{\rm D}}{n_{\rm i,SSi}} + \ln\frac{N_{\rm D}}{n_{\rm i,SiGe}}\right) + \frac{\Delta E_{\rm V} + \Delta E_{\rm C}}{2}\right], \tag{5}$$

where $n_{\rm i,SSi}$ and $n_{\rm i,SiGe}$ are the intrinsic carrier concentrations of the SSi and SiGe layers, respectively.

The gate voltage which causes strong inversion at the SSi/SiGe interface is denoted as the interface threshold voltage $V_{\rm T}^{\rm H}$. The condition for the onset of strong inversion at the interface is defined, in a similar manner, as the gate voltage at which the minority carrier concentration at the interface is equal to the substrate doping concentration. The threshold interface potential $\Phi_{\rm T}^{\rm H}$ for strong inversion at the interface is given by

$$\Phi_{\rm T}^{\rm H} = -\frac{2KT}{q}\left(\ln\frac{N_{\rm D}}{n_{\rm i,SiGe}}\right). \tag{6}$$

When the epitaxial layers are highly doped, inversion occurs only at the SSi surface, and it can be easily observed from the Fig. 4 that the expression of the threshold potential $\Phi_{\rm T}^{\rm S}$ at the surface is the same as that for light doping concentrations, given by Eq. (5).

3.2.2. Threshold voltage for a lightly doped pMOSFET

To derive the expressions for the threshold voltages, Poisson's equation has to be solved. For a lightly doped pMOSFET, the analytical solution in the one-dimensional case can be obtained by taking into account the charge in the depletion layer and the hole charge in the SiGe layer. The hole charge in the SSi layer is neglected, since strong inversion first occurs at the SSi/SiGe interface.

Under these assumptions, the one-dimensional Poisson's equation can be written for each region of the structure as follows:

$$\frac{\partial^2\Phi_1(x)}{\partial x^2} = -\frac{qN_{\rm D}}{\varepsilon_{\rm SiGe}}\left[1 + \exp\left(\frac{2\phi_{\rm F} - \Phi_1}{v_t}\right)\right], \quad t_{\rm SSi} < x < t_{\rm SSi} + x_{\rm d}, \tag{7}$$

$$\frac{\partial^2\Phi_2(x)}{\partial x^2} = -\frac{qN_{\rm D}}{\varepsilon_{\rm SSi}}, \quad 0 < x < t_{\rm SSi}, \tag{8}$$

where $t_{\rm SSi}$ and $x_{\rm d}$ are the thickness of the SSi layer and the depletion width respectively.

Integrating Eq. (7) from $x = t_{\rm SSi}$ to $x = t_{\rm SSi} + x_{\rm d}$ and using $E_1(t_{\rm SSi} + x_{\rm d}) = 0$, we have

$$E_{\rm H} = -\sqrt{\frac{2qN_{\rm D}}{\varepsilon_{\rm SiGe}}[v_t(\,{\rm e}^{(2\phi_{\rm F}-\varphi_{\rm H})/v_t} - 1) - \varphi_{\rm H}]}, \tag{9}$$

where $\varphi_{\rm H}$ and $E_{\rm H}$ are defined as the electric potential and the electric field at the SSi/SiGe interface respectively.

Integrating Eq. (8) over the SSi region and using the boundary conditions

$$E_2(t_{\rm SSi}) = \frac{\varepsilon_{\rm SiGe}}{\varepsilon_{\rm SSi}} E_{\rm H},$$

$\Phi_1(t_{\rm SSi}) = \varphi_{\rm H}$, the following equations can be obtained

$$\frac{\partial \Phi_2}{\partial x} = -\frac{qN_{\rm D}}{\varepsilon_{\rm SSi}}(x - t_{\rm SSi}) - \frac{\varepsilon_{\rm SiGe}}{\varepsilon_{\rm SSi}} E_{\rm H}, \tag{10}$$

$$\Phi_2 = -\frac{qN_{\rm D}}{2\varepsilon_{\rm SSi}}(x - t_{\rm SSi})^2 - \frac{\varepsilon_{\rm SiGe}}{\varepsilon_{\rm SSi}} E_{\rm H}(x - t_{\rm SSi}) + \varphi_{\rm H}. \tag{11}$$

By taking into account all potential drops across the structure, the expression for the gate voltage $V_{\rm G}$ can be written as

$$V_{\rm G} = V_{\rm FB}^{\rm S} - \frac{Q_{\rm SSi} + Q_{\rm SiGe}}{C_{\rm OX}} + \Phi_2(0), \tag{12}$$

where $Q_{\rm SSi}$ and $Q_{\rm SiGe}$ are the whole charge in the SSi layer and SiGe layer respectively.

When the inversion occurs at the SSi/SiGe interface, the potential $\varphi_{\rm H}$ is pinned to $\Phi_{\rm T}^{\rm H}$, $Q_{\rm SSi}$ and $Q_{\rm SiGe}$ can be calculated by

$$Q_{\rm SSi} = -\frac{qN_{\rm D}t_{\rm SSi}^2}{\varepsilon_{\rm SSi}}, \tag{13}$$

$$Q_{\rm SiGe} = -\varepsilon_{\rm SiGe} E_{\rm H} = \left(2\varepsilon_{\rm SiGe} qN_{\rm D}[v_t(e^{(2\phi_{\rm F} - \Phi_{\rm T}^{\rm H})/v_t} - 1) - \Phi_{\rm T}^{\rm H}]\right)^{1/2}. \tag{14}$$

The expression for $V_{\rm T}^{\rm H}$ can be derived directly from Eq. (12) as

$$V_{\rm T}^{\rm H} = V_{\rm FB}^{\rm H} + \left(\frac{t_{\rm OX}}{\varepsilon_{\rm OX}} + \frac{t_{\rm SSi}}{\varepsilon_{\rm SSi}}\right)\varepsilon_{\rm SiGe} E_{\rm H} + \Phi_{\rm T}^{\rm H}. \tag{15}$$

This equation can be simplified by noting that the hole contribution is very small at the onset of strong inversion at the SSi/SiGe interface and therefore the maximum depletion width is then obtained as

$$x_{{\rm d},V_{\rm T}^{\rm H}} = \sqrt{-\frac{2\varepsilon_{\rm SiGe}\Phi_{\rm T}^{\rm H}}{qN_{\rm D}}}. \tag{16}$$

The threshold voltage $V_{\rm T}^{\rm S}$ can be also obtained from Eq. (12), but in this case the hole contribution in the SiGe layer is important. Using Eqs. (5) and (12), the threshold voltage $V_{\rm T}^{\rm S}$ can be expressed as

$$V_{\rm T}^{\rm S} = V_{\rm FB}^{\rm S} - \frac{qN_{\rm D}t_{\rm SSi} + qN_{\rm D}x_{{\rm d},V_{\rm T}^{\rm H}} + Q_{\rm i1}}{C_{\rm OX}} + \Phi_{\rm T}^{\rm S}, \tag{17}$$

where $Q_{\rm i1}$ is the inversion charge in the SiGe layer, given by

$$Q_{\rm i1} = -C_{\rm oxeff}(V_{\rm T}^{\rm S} - V_{\rm T}^{\rm H}), \tag{18}$$

$$C_{\rm oxeff} = \left(\frac{t_{\rm OX}}{\varepsilon_{\rm OX}} + \frac{t_{\rm SSi}}{\varepsilon_{\rm SSi}}\right)^{-1}. \tag{19}$$

3.2.3. Threshold voltage for a highly doped pMOSFET

In this case, inversion occurs only in the SSi layer. Therefore, Eq. (17) can be rectified as

$$V_{\rm T}^{\rm S} = V_{\rm FB}^{\rm S} - \frac{qN_{\rm D}t_{\rm SSi} + qN_{\rm D}x_{{\rm d},V_{\rm T}^{\rm S}}}{C_{\rm OX}} + \Phi_{\rm T}^{\rm S}, \tag{20}$$

where $x_{{\rm d},V_{\rm T}^{\rm S}}$ is the depletion width when $\Phi_2(0) = \Phi_{\rm T}^{\rm S}$, and can be calculated by

$$x_{{\rm d},V_{\rm T}^{\rm S}} = -\frac{\varepsilon_{\rm SiGe}}{\varepsilon_{\rm SSi}} t_{\rm SSi} + \sqrt{\left(\frac{\varepsilon_{\rm SiGe}}{\varepsilon_{\rm SSi}} t_{\rm SSi}\right)^2 - \frac{\varepsilon_{\rm SiGe}}{\varepsilon_{\rm SSi}} t_{\rm SSi}^2 - \frac{2\varepsilon_{\rm SiGe}}{qN_{\rm D}}\phi_{\rm T}^{\rm S}}. \tag{21}$$

4. Formation mechanism of plateau

As discussed above, when the epitaxial layers are lightly doped, the flatband voltages are almost the same, but the threshold voltages are different. As the voltage goes from $V_{\rm T}^{\rm H}$ to $V_{\rm T}^{\rm S}$, holes gradually enter into the SSi layer, which means the inversion capacitance at the surface SSi layer $C_{\rm T}^{\rm S}$ becomes more significant. Defining $C_{\rm T}^{\rm H}$ as the inversion capacitance at SSi/SiGe interface and $C_{\rm OX}$ as the oxide capacitance, the gate capacitance $C_{\rm G}$ transfers from $C_{\rm G} = \left[C_{\rm OX}^{-1} + (C_{\rm T}^{\rm H})^{-1}\right]^{-1}$ to $C_{\rm G} = \left[C_{\rm OX}^{-1} + (C_{\rm T}^{\rm S})^{-1}\right]^{-1}$, causing a "plateau" to appear in the inversion region of the C–V characteristics.

When the epitaxial layers are highly doped, however, inversion occurs only in the SSi layer, and the difference between the flatband voltages are more apparent according to Eq. (4). Therefore, as the gate voltage goes from $V_{\rm FB}^{\rm S}$ to $V_{\rm FB}^{\rm H}$, the gate capacitance $C_{\rm G}$ transfers from $C_{\rm G} = C_{\rm OX}$ to $C_{\rm G} = C_{\rm oxeff}$. This leads to a "plateau" appearing in the accumulation region of the C–V characteristics.

5. Results and discussions

To validate our model, the results obtained from our model are compared with experimental data available in this section.

Figure 5 shows the experimental results of the gate C–V characteristics of the strained-Si/SiGe pMOSFET when the doping concentration is 1×10^{16} cm^{-3}. From the figure, we can observe that there is a plateau formed in the inversion layer, which means that inversion occurs first in the SiGe layer and then in the SSi layer. The inset shows the derivative of the C–V curves. The first two peaks observed in the inversion region are explained by the inversion of holes at the SSi/SiO_2 and SSi/SiGe interfaces respectively, the values of $V_{\rm T}^{\rm H} = -1.01$ V and $V_{\rm T}^{\rm S} = -1.26$ V that were obtained from our model agree very well with the values of $V_{\rm T}^{\rm H} = -0.98$ V and $V_{\rm T}^{\rm S} = -1.30$ V that were extracted from the inset. Since the epitaxial layers are lightly doped, the difference between

V_{FB}^{S} and V_{FB}^{H} can be negligible. So there is only one peak observed and no plateau formed in the accumulation region.

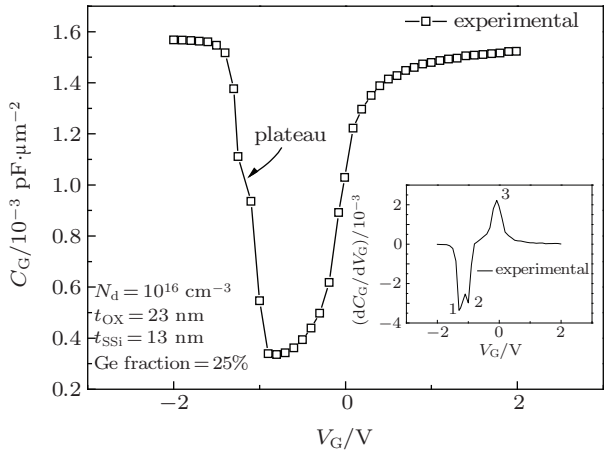


Fig. 5. Experimental results of the gate *C*–*V* characteristics for a lightly doped SSi/SiGe pMOSFET. The inset shows the derivative of the *C*–*V* curves.

The results from the model are also compared with the results from Synopsys ISE TCAD v10.0 when the epitaxial layers are highly doped, as shown in Fig. 6. Here, there is a plateau in the accumulation region since the V_{FB}^{S} is larger than V_{FB}^{H}. As shown in the inset, the difference between the last two peaks, corresponding to the accumulation of electrons at the two interfaces, is more apparent than that in Fig. 6. The reason for the absence of a plateau in the inversion region is that there is no inversion charge formed in the SiGe layer. The flatband and threshold voltages, extracted from the inset, are $V_{FB}^{S} = 0.3$ V, $V_{FB}^{H} = -0.2$ V, and $V_{T}^{S} = -2.4$ V, consistent with the results of our model.

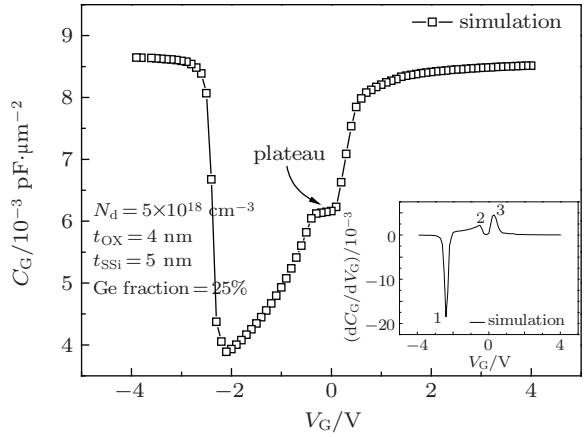


Fig. 6. Simulation results of the gate *C*–*V* characteristics for a highly doped SSi/SiGe pMOSFET. The inset shows the derivative of the *C*–*V* curves.

Figure 7 shows the variations of flatband and threshold voltages with different doping concentrations. Since the potential drop across the oxide and SSi layers increases with increasing N_D, the difference between V_{FB}^{S} and V_{FB}^{H} becomes more apparent, as discussed above. Also, it can be observed that V_{T}^{S} and V_{T}^{H} are inversely proportional to the doping concentration N_D, because the increasing ionized charges cause the inversion charge density to decrease. The threshold V_{T}^{H} reduces to V_{T}^{S} at $N_D = 3.8\times10^{17}$ cm^{-3}, which means the conduction of the device shifts from the buried channel to the SSi channel. After that, the conduction of the device is caused only by surface-channel conduction.

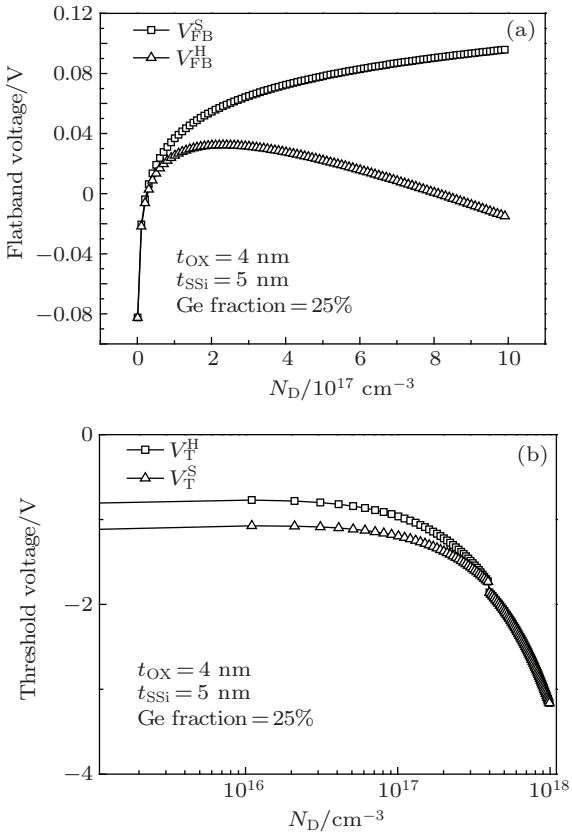


Fig. 7. Variations of flatband and threshold voltages with different doping concentrations. (a) Flatband voltages and (b) threshold voltages.

6. Conclusion

In conclusion, by physically deriving the models of the flatband and threshold voltages, the effect of substrate doping on the flatband and threshold voltages of a strained-Si/SiGe pMOSFET has been studied to explain the shift in the plateau from the inversion region to the accumulation region as the substrate doping increases, which is observed in the gate *C*–*V* characteristics of the strained-Si pMOSFET. The results from the models show excellent agreement with the simulated and experimental data. The proposed model can provide a valuable reference to the designers of strained-Si devices and has been implemented in software for extracting the parameters of strained-Si MOSFET.

References

[1] Wu T F, Zhang H M, Wang G Y and Hu H Y 2011 *Acta Phys. Sin.* **60** 027305 (in Chinese)

[2] Song J J, Zhang H M, Hu H Y, Dai X Y and Xuan R X 2007 *Chin. Phys.* **16** 3827

[3] Li G J, Lai H K, Li C, Chen S Y and Yu J Z 2008 *Chin. Phys.* B **17** 3479

[4] Zhang Z F, Zhang H M, Hu H Y, Xuan R X and Song J J 2009 *Acta Phys. Sin.* **58** 4648 (in Chinese)

[5] Maiti C K 2007 *International Workshop on Physics of Semiconductor Devices (IWPSD'07)*, December 16–20, 2007, Bombay, India, p. 55

[6] Li B, Liu H X, Yuan B, Li J and Lu F M 2011 *Acta Phys. Sin.* **60** 017202 (in Chinese)

[7] Q S S, Zhang H M, Hu H Y, Wang G Y, Wang X Y, Qu J T and Xu X B 2011 *Sci. Chin.: Phys. Mech. Astron.* **54** 2181

[8] Flachowsky S, Wei A, Illgen R, Herrmann T, Hontschel J, Horstmann M and Klix W 2010 *IEEE Trans. Electron Dev.* **57** 1343

[9] Bera L K, Mathew S, Balasubramanian N, Braithwaite G, Currie M T and Singaporewala F 2004 *Appl. Surf. Sci.* **224** 278

[10] Liao J H, Canonico M, Robinson M and Schroder D 2006 *ECS Trans.* **3** 1211

[11] Zainuddin A N M and Haque A 2007 *Semicond. Sci. Technol.* **22** 125

[12] Wei J Y, Maikap S, Lee M H, Lee C C and Liu C W 2006 *Solid State Electron.* **50** 109

[13] Bindu B, DasGupta N and DasGupta A 2007 *IEEE Trans. Electron. Dev.* **54** 1889

[14] Li L, Liu H X and Yang Z N 2012 *Acta Phys. Sin.* **61** 166101 (in Chinese)

[15] Qin S S, Zhang H M, Hu H Y, Dai X Y, Xuan R X and Shu B 2010 *Chin. Phys.* B **19** 117309

[16] Zhang W M and Fossum J G 2005 *IEEE Trans. Electron. Dev.* **52** 263

[17] Fossum J G and Zhang W M 2003 *IEEE Trans. Electron. Dev.* **50** 1042