The pulsed microwave damage trend of a bipolar transistor as a function of pulse parameters*

Ma Zhen-Yang(马振洋)†, Chai Chang-Chun(柴常春), Ren Xing-Rong(任兴荣), Yang Yin-Tang(杨银堂), Zhao Ying-Bo(赵颖博), and Qiao Li-Ping(乔丽萍)

School of Microelectronics, Key Lab of Ministry of Education for Wide Band-Gap Semiconductor Materials and Devices, Xidian University, Xi'an 710071, *China*

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In the present paper we conduct a theoretical study of the thermal accumulation effect of a typical bipolar transistor caused by high power pulsed microwaves (HPMs), and investigate the thermal accumulation effect as a function of pulse repetition frequency (PRF) and duty cycle. A study of the damage mechanism of the device is carried out from the variation analysis of the distribution of the electric field and the current density. The result shows that the accumulation temperature increases with PRF increasing and the threshold for the transistor is about 2 kHz. The response of the peak temperature induced by the injected single pulses indicates that the falling time is much longer than the rising time. Adopting the fitting method, the relationship between the peak temperature and the time during the rising edge and that between the peak temperature and the time during the falling edge are obtained. Moreover, the accumulation temperature decreases with duty cycle increasing for a certain mean power.

Keywords: bipolar transistor, high power microwave, pulse repetition frequency, duty cycle

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1. Introduction

Electromagnetic interference induced by a high power microwave (HPM) on an electronic system is attracting increasing attention at the moment.[1–8] Such interference could cause upset, component degradation, and even permanent physical damage of the electronics. Some of the experimental studies focused on the effect as a function of pulse parameters. The susceptibility levels of an electronic device to different threats like electromagnetic pulse (EMP), ultra-wideband (UWB), and HPM pulses have been assessed,[9] which shows that the effect of a rising of the pulse repetition frequency (PRF) can significantly lower the susceptibility levels. System immunity testing of electronic systems to HPM radiation showed that the pulses could not induce permanent damage when the PRF was lower than 1 kHz.[10] The effects of UWB and radar pulses on the receiver of a digital wireless communication system was investigated by changing the power, the pulse length and the PRF,[11] which showed that some disturbances and disruptions occurred in the baseband of the receiving unit, and disturbance PRFs were more than 3.5 kHz for a wireless local area network (WLAN) and 2 kHz for the Bluetooth. All the experimental investigations indicate that the study of the microwave susceptibility trend as a function of pulse parameters is a profound task. However, few attempts have been made of the theoretical study. Specifically, there is a particular lack of device failure levels, while the assessment of pulse parameters on the upset and destruction effects is important for developing models of the susceptibility behaviors and protection elements.

In our previous studies[12,13] we have shown the physical damage to a bipolar transistor due to continuous wave (CW) microwaves, and investigated the effects of some important parameters such as pulse width and frequency on the damage process. In the present paper, the thermal accumulation effect of the bipolar transistor, induced by high power pulsed microwaves, is presented, and the effects of the pulsed waveform parameters such as pulse repetition frequency and duty cycle on the damage process of the device are studied. The damage threshold is established and the internal damage mechanism is investigated using a two-dimensional (2D) electro-thermal model.

2. Structure and model

2.1. Device structure

Figure 1 shows the three-dimensional (3D) view of the analyzed silicon n^+–p–n–n^+ epitaxial planar transistor. Due to the symmetry of the transistor, only half of the central emitter finger needs to be analyzed. The transistor consists of a 200-μm-thick n^+-type collector substrate and a 2-μm-thick n-type epitaxial layer. Here B, C, and E refer to its base, collector, and emitter contact, respectively; N^+ denotes the heavily doped region of the n-type silicon; N and P represent the n-

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†Corresponding author. E-mail: zyma@mail.xidian.edu.cn

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and p-type silicon regions respectively. The doping profile of the transistor is given in Fig. 2. Ohmic contacts at the three contacts are charge neutral and in equilibrium. The thermal electrode is located at the bottom of the transistor where the lattice temperature remains at 300 K. The upper surface and the sidewall boundaries are thermally insulated from the environment.

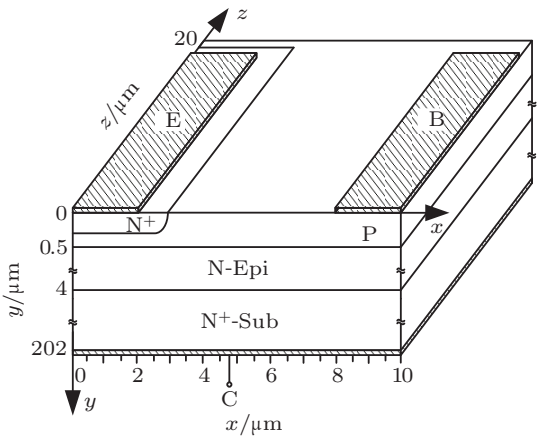


Fig. 1. Three-dimensional view of a typical n^+–p–n–n^+ transistor.

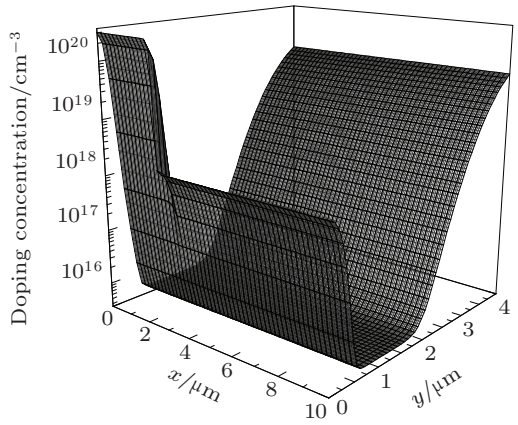


Fig. 2. Doping profile of the transistor.

2.2. Numerical modeling

To investigate the pulse thermal accumulation effect of the bipolar transistor, the advanced mixed mode device and circuit simulator ISE-DESSIS is employed, which computes the electrical behavior of the device by iteratively solving the Poisson equation and the current-continuity equations. During the microwave injection, its high current and high voltage cause huge Joule heating in parts of the device. Hence, a thermodynamic model is adopted in the present paper, in which the drift-diffusion approach extends to taking the electro-thermal effect into account[14] on the assumption that the charge carriers are in thermal equilibrium with the lattice. The three basic semiconductor equations should also account for the thermal effect. The current densities of electrons and holes are given by

$$\boldsymbol{J}_{\mathrm{n}} = -nq\mu_{\mathrm{n}}\left(\nabla\phi_{\mathrm{n}} + P_{\mathrm{n}}\nabla T\right), \tag{1}$$

$$\boldsymbol{J}_{\mathrm{p}} = -pq\mu_{\mathrm{p}}\left(\nabla\phi_{\mathrm{p}} + P_{\mathrm{p}}\nabla T\right), \tag{2}$$

where μ_{n} (μ_{p}) is the electron (hole) mobility, ϕ_{n} (ϕ_{p}) is the electron (hole) quasi-Fermi potential, and P_{n} (P_{p}) is the electron (hole) absolute thermoelectric power.

To obtain a non-uniform temperature distribution, the internal self heating is taken into account by solving the following heat flow equation

$$\begin{aligned} & c\frac{\partial T}{\partial t} - \nabla\cdot\kappa\nabla T \\ = & -\nabla\cdot\left[(P_{\mathrm{n}}T+\phi_{\mathrm{n}})\boldsymbol{J}_{\mathrm{p}} + (P_{\mathrm{p}}T+\phi_{\mathrm{p}})\boldsymbol{J}_{\mathrm{p}}\right] \\ & -\left(E_{\mathrm{C}} + \frac{3}{2}k_{\mathrm{B}}T\right)\nabla\cdot\boldsymbol{J}_{\mathrm{n}} \\ & -\left(E_{\mathrm{V}} - \frac{3}{2}\mathrm{k_B}T\right)\nabla\cdot\boldsymbol{J}_{\mathrm{n}} + qR(E_{\mathrm{C}} - E_{\mathrm{V}} + 3k_{\mathrm{B}}T), \end{aligned} \tag{3}$$

where c is the lattice heat capacity; κ the thermal conductivity; $\boldsymbol{J}_{\mathrm{n}}(\boldsymbol{J}_{\mathrm{p}})$ is the electron (hole) current destiny; E_{C} (E_{V}) is the conduction (valence) band energy; R denotes the recombination rate; k_{B} is the Boltzmann constant. A more detailed description of the physical model can be found in Ref. [12].

3. Results and discussion

3.1. HPM burnout power threshold versus pulse duration

The schematic representation of the simulation circuit is shown in Fig. 3, in which the transistor is in the active mode of operation. By using the device simulator ISE-TCAD, device failure is present when the local lattice temperature reaches the melting point of silicon, 1688 K. In a previous paper we presented the damage effect and the mechanism of a bipolar transistor, caused by continuous wave (CW) microwaves, and found that the base-emitter junction was damaged due to the localized heat accumulation.[12] In the present paper,

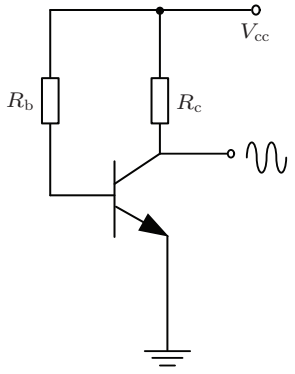


Fig. 3. Schematic diagram of the circuit used in our simulation.

the square pulse modulated sinusoidal signals with a frequency of 1 GHz are injected from the collector terminal. Figure 4 shows the variation of the peak temperature of the device with time. The injected signal is characterized by the amplitude $U_0 = 20$ V, the pulse width $\tau = 40$ ns and the PRF = 1 MHz. As can be seen from Fig. 4, the overall peak temperature is raised by the energy of the pulses, and decreases in the pulse interval. The overall temperature of the device presents a periodic rise-fall-rise process.

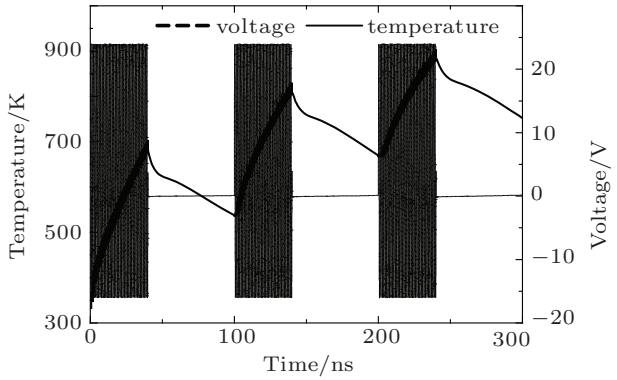


Fig. 4. Peak temperature of the device and injected signal, each versus time.

3.2. Influence of PRF on damage process

The study is conducted by varying the pulse repetition frequency from 2 kHz to 10 MHz. All the injected signals are characterized by $U_0 = 20$ V. Because of the computer capacity constraint, only four repetition periods are studied. Figure 5 shows the transient temperature responses of pulse signals with $\tau = 40$ ns for the values PRF of 5 MHz, 500 kHz, and 2.5 kHz, respectively. The accumulation temperature ΔT during the first four cycles is defined as

$$\Delta T = T_{1,4} - T_{\rm op}, \tag{4}$$

where $T_{1,4}$ is defined as the peak temperature at the end of the fourth cycle, and the $T_{\rm op}$ as the operating temperature. $T_{\rm op}$ is about 333.4 K for the transistor. It is obvious that ΔT increases rapidly with PRF increasing, which means that the device is more vulnerable to the damage at higher PRF. Here, ΔT is about 259.4 K when the PRF is 5 MHz. However, when the PRF decreases to 500 kHz ΔT is only about 61.3 K, and when the PRF is about 2.5 kHz, ΔT is about 0.445 K, which can be neglected. It is also shown that the temperature-rising process is easier and faster than the temperature-falling process.

Figure 6 shows the variations of ΔT with PRF for $\tau =$ 40 ns, 60 ns, and 100 ns, respectively. It indicates that the three curves each produce an increasing dependence on PRF but their gradients are different from each other. For a certain PRF of the injected pulse, ΔT goes up gradually with the increase of pulse width. Meanwhile, the ΔT increment increases with PRF increasing. For example, ΔT for the case of $\tau = 100$ ns is about 36.7 K higher than that for the case of $\tau = 40$ ns when the PRF is 100 kHz. However, when the PRF is 1 MHz, ΔT for the case of $\tau = 100$ ns is about 123.7 K higher than that for the case of $\tau = 40$ ns. The former is about three times higher than the latter. The PRF and the pulse width both have a significant influence on the temperature accumulation. It can be predicted that the higher the PRF and the longer the pulse width, the higher the ΔT will be. In other words, increasing the PRF can lead to accumulating more heat and lowering burnout peak power. The three curves in Fig. 6 also show that there does not seem to be any thermal stacking between the subsequent pulses when the PRF is lower than 2 kHz for the device used in the present paper.

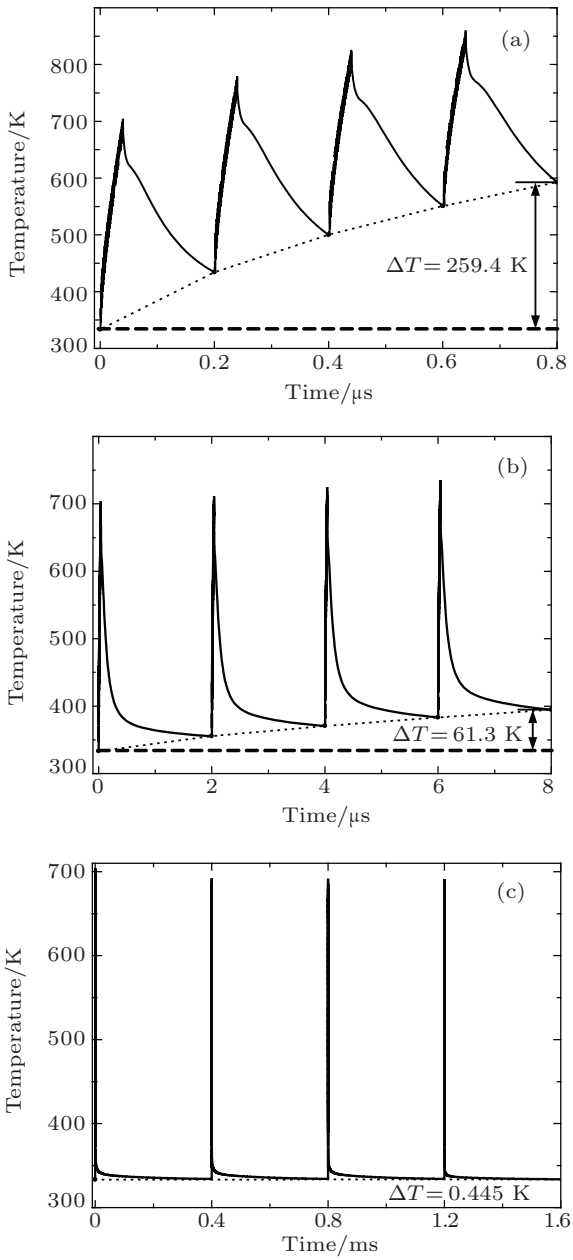


Fig. 5. Variations of peak temperature with time for PRF = 5 MHz (a), 500 kHz (b), and 2.5 kHz (c).

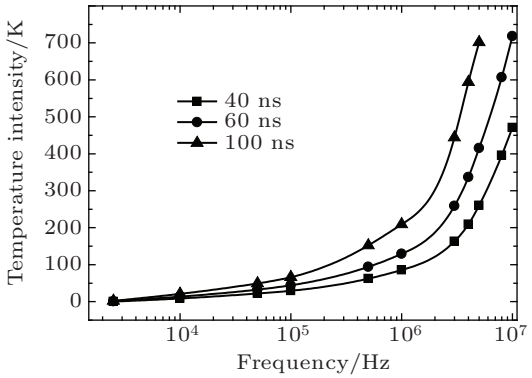


Fig. 6. Curves of temperature increment ΔT versus RPF for $\tau = 40$ ns, 60 ns, and 100 ns.

In order to study the mechanism of the effect of PRF on the pulse temperature accumulation, the single pulses are injected from the collector terminal until the temperature drops to initial value ($T_{\rm op}$). Figure 7 shows the rising edges and the falling edges of the injected pulses with $U_0 = 20$ V and the pulse widths in a range from 20 ns to 100 ns. It indicates that there exists an asymmetry phenomenon between the two edges. For each injected pulse, the rising time is far shorter than the falling time, indicating that the rising time is on the order of nanoseconds, while the falling time is on the order of microseconds. Both the rising edge and the falling edge undergo abnormal exponential progression. Adopting the curve fitting method to fit the data points, the relationship between the peak temperature and the time during the rising edge is given by

$$T = 366.0 + 840.1 \times (1 - \exp(-t/8.33 \times 10^{-8})), \qquad (5)$$

of which the correlation coefficient (R^2) is 0.996, showing a high degree of fitting between peak temperature and time. For the various falling response curves, the curves with $\tau = 40$ ns and 80 ns are chosen to be fitted. The relationships between the peak temperature and the time during the falling time are expressed as

$$T = 335.6 + 460.9 \times \exp(-t/1.3 \times 10^{-7}), \qquad (6)$$

$$T = 337.5 + 853.0 \times \exp(-t/1.8 \times 10^{-7}). \qquad (7)$$

Equations (6) and (7) are for the cases of $\tau = 40$ ns and 80 ns, respectively, each of which has a high degree of fitting, up to 0.99. The fitting curves indicate that all the falling edges conform with the same equation:

$$T = T_0 + P \cdot \tau_{\rm th} \cdot \exp(-t/\tau_{\rm th}), \qquad (8)$$

where P is the injected electrical power, and $\tau_{\rm th}$ is the thermal time constant. Due to the fact that $\tau_{\rm th}$ is an increasing function of temperature[15] and the initial temperatures of the falling edges for different pulse widths are different, the values of $\tau_{\rm th}$ for different pulse widths are not the same. The fitting formula can be used to predict the temperature responses of the device under the injections of pulse signals with different pulse widths.

Figure 7 demonstrates that the peak temperatures dropping to their initial value after $t = 5$ ms for all the pulse widths. It indicates that no stacking effect occurs when the pulse train is shorter than 5 ms, and the result coincides with the conclusion depicted in Fig. 6. When the PRF is lower than 2 kHz, permanent damage is usually caused by the first pulse of a pulse train. If not, there will be no heat stack during the interval, and the device will not be damaged.

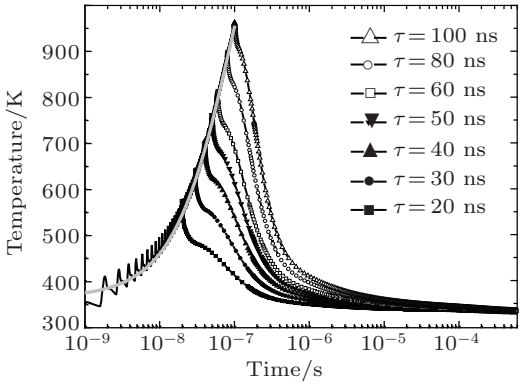


Fig. 7. Responses of peak temperature of the device versus time for single pulses in the cases of several different pulse widths.

3.3. Influence of duty cycle on the damage process

In order to study the effect of duty cycle (DC) on the device damage process, the signals with a PRF of 1 MHz and mean power of 1.8×10^{-2} W are injected from the collector using the circuit in Fig. 3. Figure 8 shows the dependence of ΔT on duty cycle. The duty cycle varies from 0.03 to 0.1. It can be seen that ΔT decreases rapidly with the increase of duty cycle. When the duty cycle ranges from 0.02 to 0.1, ΔT reduces 132.8 K in the first four cycles.

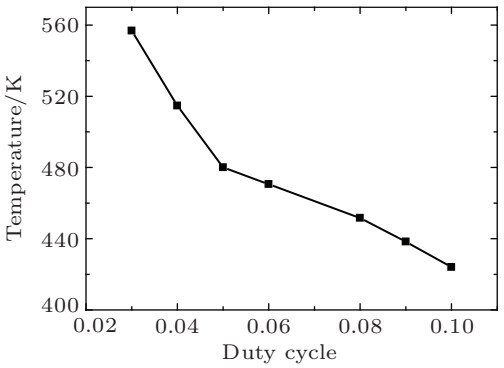


Fig. 8. Temperature increment ΔT versus duty cycle for a certain signal mean power.

In previous work, the results showed that temperature accumulation occurred mostly in the negative half-period,[12] so our study focuses on the negative half-period in this section. Figure 9 shows the variations of the current density across the damage position (along the line $y = 0.1$ μm), with the signals with different duty cycles injected at the moment of the valley value ($U = -|U_0|$), indicating that the current density at

the edge of the emitter drops off gradually with the increase of duty cycle. The current density at DC = 0.03 is four times larger than that at DC = 0.1. It is known that the total current and the displacement current are directly proportional to the injected voltage and the change rate of the injecting voltage, respectively.[16] For a certain mean power, the smaller the duty cycle, the higher the amplitude of the pulse will be. In the present paper, each of all the injected pulses has a frequency of 1 GHz, so the change rate of the pulse increases gradually with duty cycle decreasing. Consequently, both the total current and the displacement current increase with duty cycle decreasing.

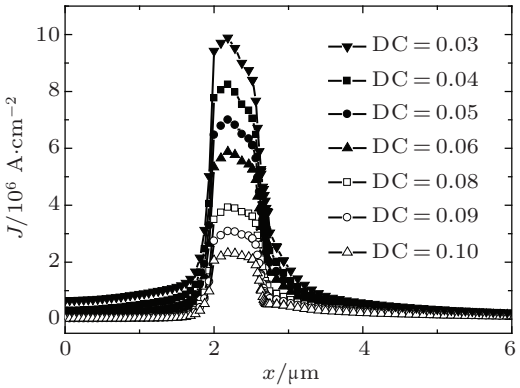


Fig. 9. Current densities across B–E junction at the moment of the valley value for different duty cycles (along the line $y = 0.1$ μm).

The electric field across the damage position (along the line $y = 0.1$ μm) at the moment of the valley value is shown in Fig. 10. It can be seen clearly that the electric field increases with duty cycle increasing. The electric field at DC = 0.1 is raised by 20% compared with the value at DC = 0.03. According to the above analysis, the amplitude of the injected voltage drops off gradually with the increase of duty cycle, and the electric field should also be in direct proportion to the signal amplitude at the moment of the valley value. However, the current density is so high under the microwave injection that the voltage drop across the substrate cannot be ignored.[17] The lower the current, the lower the voltage drop across the substrate and the higher the voltage drop across the B–E junction will be. Therefore, the electric field presents an increasing tendency.

The normalized power density dissipated at the damage position is also displayed in Fig. 10. The power density is shown to be a linear function of the duty cycle. It is known that the power density is a function of electric field and current density. Because the electric field is one order of magnitude lower than the current density, the power density at the damage position is mainly determined by the current density and the power density has a similar trend to that the current density has. When the power density dissipated at the damage position decreases with duty cycle increasing, the temperature accumulation will decrease naturally.

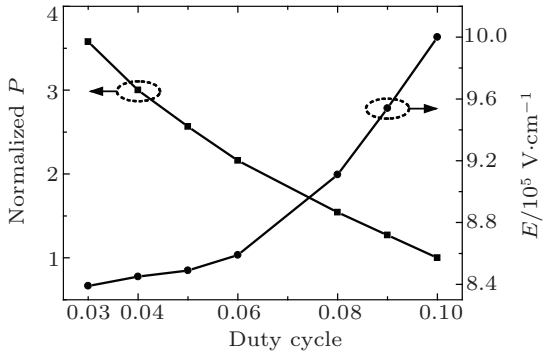


Fig. 10. Normalized power dissipated at the damage position (■) and the electric field across the damage position (●) (along the line $y = 0.1$ μm).

4. Conclusion

A typical n^+–p^--n^--n^+ bipolar transistor is established using the ISE-TCAD simulator, and the thermal accumulation effect of the device, induced by the pulsed microwave, is presented. The influences of the PRF and duty cycle on the damage process are investigated. The findings show that the PRF threshold for the transistor is approximately 2 kHz. The pulses with lower PRFs cannot induce any thermal stacking and the device cannot be damaged. Increasing the PRF can lead more to accumulating temperature. In other words, the burnout power threshold of the injected pulsed can be reduced. When the mean power of the pulse is given, the current density across the damage position drops off gradually with duty cycle increasing. Due to the fact that the electric field is one order lower than the current density, the accumulation temperature is determined mainly by the latter, and the accumulation temperature decreases with duty cycle increasing.

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