Discussion of the metric in characterizing the single-event effect induced by heavy ions*

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The single-event effect (SEE) is the most serious problem in space environment. The modern semiconductor technology is concerned with the feasibility of the linear energy transfer (LET) as metric in characterizing SEE induced by heavy ions. In this paper, we calibrate the detailed static random access memory (SRAM) cell structure model of an advanced field programmable gate array (FPGA) device using the computer-aided design tool, and calculate the heavy ion energy loss in multi-layer metal utilizing Geant4. Based on the heavy ion accelerator experiment and numerical simulation, it is proved that the metric of LET at the device surface, ignoring the top metal material in the advanced semiconductor device, would underestimate the SEE. In the SEE evaluation in space radiation environment the top-layers on the semiconductor device must be taken into consideration.

Keywords: cross-section curve, metric, linear energy transfer, field programmable gate array

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1. Introduction

Radiation effects in electronics range from loss of data to catastrophic failure. The single-event effect (SEE) caused by the passage of single energetic particles (such as protons, neutrons, or heavy ions) through a sensitive device becomes the most serious problem.[1] The result of the SEE characterized by ground-based testing is commonly presented as a cross section.[2–4] The cross section results are then used to estimate the SEE in space environment.[5,6] The linear energy transfer (LET) is the only engineering metric of heavy ions, so the result of accelerator testing is always presented as a cross section curve (the cross section versus LET).

The modern semiconductor technology makes the workaround less practical.[7] The material changing accompanied with the lithography shrinking results in the changing of the physics process as heavy ions pass through the microelectronic device.[8,9] The top layers containing the high-z material have affected the feasibility of the traditional SEE characterizing method. In this paper the metric in characterizing SEE ions is discussed based on heavy ion irradiation experiments and numerical simulation.

2. Experimental details

2.1. Experiment setup

The object device for the experiment is the Virtex XCV300PQ240 produced by Xilinx. It is fabricated with 0.25-μm complementary metal-oxide semiconductor (CMOS) process. The Xilinx Virtex device is a static random access memory (SRAM)-based in-system configuration, and it is most suited for use in many telecommunications, digital signal processor (DSP) application, and so on in space and other areas. The usual static single event upset (SEU) testing on an SRAM-based field programmable gate array (FPGA) is to determine the saturation cross section and threshold of upsets in the configuration logic block (CLB) (the array of SRAM cells, which provides functional elements, for combinatorial and synchronous logic are an array of SRAM cells).[10] The static SEU testing in this paper is to determine the saturation cross section and threshold of upsets in the CLB.

The heavy ion irradiations were performed using the tandem electronic static accelerator in Beijing, China. Table 1 shows the heavy ions that were used in the SEU testing. The LET in the table is the linear energy transport in silicon at the surface of the device. The penetration depth calculation is also achieved on the assumption that the heavy ions strike on the silicon material directly without passing through the multi-layer metals.

Table 1. Heavy ion beams used in this work.

Species	Energy/MeV	LET/(MeV·cm^2/mg)	Penetration depth*/μm
$^{12}C^{6+}$	80	1.73	140
$^{19}F^{8+}$	110	4.17	82.6
$^{19}F^{8+}$	80	5.02	54.4
$^{35}Cl^{11+}$	140	13.6	39.6
$^{48}Ti^{16+}$	170	22.0	
$^{63}Cu^{13+}$	190	32.8	30.2
$^{79}Br^{12+}$	210	42.0	29.4

The SRAM SEU cross section was measured using the radiation effect measurement system developed by Northwest Institute of Nuclear Technology. Experiments were performed using ions at normal incidence. Error counts were limited to no more than 2% (and usually much lower) of the memory array size to reduce the probability of bits being upset more than once during an irradiation cycle. During the heavy ion irradiation the power supply current and the FPGA function

were monitored. Once the abnormalities of FPGA power supply current and function appear, the testing system would self-reboot. If the power supply current exceeded a preset value (just above the static current), a latch was counted. The devices in all of the tests were at the same bias voltage, and the configurations of the device were the same. All tests were performed under the same conditions except the incidence heavy ions.

2.2. Experiment result

Figure 1 is the plot of the SEU cross section versus LET, where the SEU cross section data of CLB are achieved from the heavy ion irradiation experiments. The value of LET is the metric of the cross section curve. The concept of LET has been developed continually to meet the improving radiation effect research, for example, the effective LET as defined by the standard inverse cosine law was developed for the angled irradiation.[11–13]

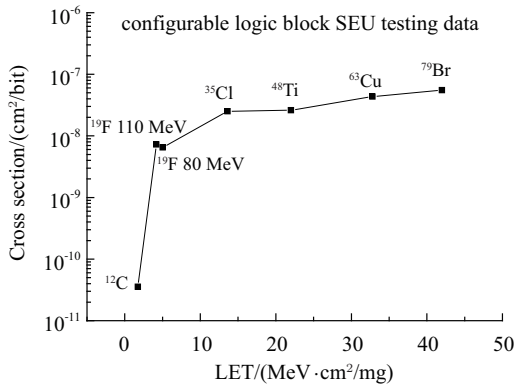


Fig. 1. Curve of cross section versus LET, where the cross section data are achieved from the heavy ion testing.

3. Numerical simulation

Recently the nuclear interaction between heavy ion and semiconductor material has attracted much attention.[9,14] Many papers have been published supporting that the concept of LET as metric of heavy ions will break down because of nuclear interaction between the heavy ions and the materials.[6] There is also a worry about the influence of the device?s multi-layer metal structure on the LET.[15]

The over layers of the 0.22-μm CMOS device could be tens of micrometers thick, which include the Si–nitride layer, aluminum layer, and tungsten layer. The heavy ions striking the semiconductor device must penetrate the top layers before reaching the sensitive silicon region. Figure 2 indicates the slices of the FPGA SRAM cell structure fabricated using technology of computer-aided design (TCAD). The top structure is constituted by Si_3N_4, tungsten, aluminum materials, and so on. The energy loss in the layers would change the heavy ion energies in the SEE sensitive regions.

The top materials in the simulations are consistent with those of the top layers used to fabricate the SRAM. The most sensitive region for SEU is consistently recognized to be the drain regions of the off-mode metal-oxide semiconductor field-effect transistor (MOSFET).[16] Figure 2 details the layer structure of the FPGA device. The complex mixed material structure would be treated as the necessary path to the most sensitive region for SEE.

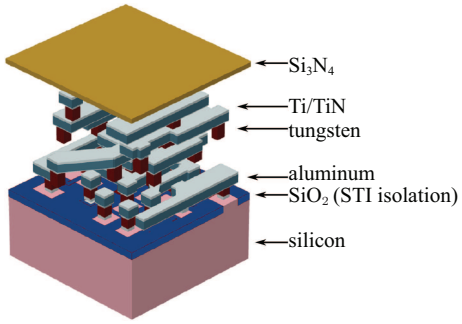


Fig. 2. (colour online) The FPGA SRAM cell structure fabricated using TCAD. The top layers over the silicon are composed of Si_3N_4, tungsten, aluminum material, and so on.

The energy loss versus depth in this device is simulated using Geant4[17] which is a group of Monte Carlo programs. The nuclear reaction and the column reaction between heavy ions and top material are calculated. The detailed top material is shown in Fig. 3.

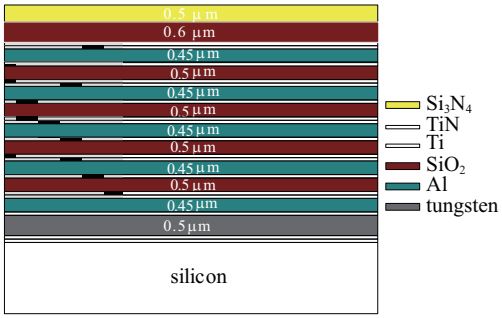


Fig. 3. (colour online) Detailed structure of the FPGA device, where the complex mixed material structure is treated as the necessary path, which would lead the heavy ions to the most sensitive region for SEE.

Table 2 shows heavy ion characteristics in the ground-based testing achieved from the Geant4 calculation. The data in the "surface" columns are achieved at the device surface using an ion detector, and the data in the "surface" LET column and the penetration depth column are calculated on the assumption that the heavy ions with initial energy strike the silicon material directly. The data in the "actual" column are data that are corrected utilizing the Geant4 calculation according to the real device structure. The energy values in the "actual" column are those of the heavy ions arriving at the surface of silicon through the metal layers.

Table 2. Results of Geant4 calculation.

Species	Energy/MeV		Penetration depth/μm		LET/(MeV · cm^2/mg)		
	Surface	Actual	Surface	Actual	Surface	Actual	Relative change
$^{12}C^{6+}$	80	75.498	140	116.14	1.73	1.813	↑ 4.74%
$^{19}F^{8+}$	110	99.434	82.6	72.1	4.17	4.443	↑ 6.50%
$^{19}F^{8+}$	80	67.469	54.4	44.02	5.01	5.442	↑ 8.54%
$^{35}Cl^{11+}$	140	106.223	39.6	29.54	13.8	15.15	↑ 9.95%
$^{48}Ti^{16+}$	170	117.136	34.85	24.85	21.8	23.66	↑ 8.53%
$^{63}Cu^{13+}$	190	111.222	30.2	20.04	32.8	33.61	↑ 2.56%
$^{79}Br^{12+}$	210	108.39	29.4	18.73	42	38.43	↓ −8.57%

4. Discussion

Table 2 indicates that the multi-layer top structure of semiconductor devices indeed affects the heavy ion LET in silicon. The top layers would change the charge accumulations in sensitive regions by heavy ions. SRAM static heavy ion SEU response data set usually fit to the Weibull integral curve function to facilitate orbital rate calculations,[18] and the function is given as

$$\sigma(\mathrm{LET}) = \sigma_{\mathrm{sat}}(1 - \exp\{-[(\mathrm{LET} - L_{\mathrm{th}})/W]^S\}),$$

where σ_{sat} is the saturation of the cross section, L_{th} is the LET threshold parameter, W is the width parameter, and S is a dimensionless exponent dubbed "power". These parameters describe the device cross section and characteristics so that the upset rate can be calculated. Table 3 gives the parameter values that are achieved from the experiment data fitting according to the expression. The values of parameters in the "surface" line are the fitted results by using the "surface LET" as metric, and the values of parameters in the "actual" LET line are the fitted results by using the corrected "actual" LET as metric. The two fittings have the same relevant coefficients.

Table 3. Parameter values received from the experiment data fitting according to the expression.

Parameter	$\sigma_{\mathrm{sat}}/10^{-7}$	L_{Th}	W	S
Surface	1.7269	1.2452	46.53	0.90494
Actual	3.346	1.2832	43.28	0.95243

Table 3 shows that the multi-layer top structure of the FPGA device can increase the fitted cross section of the experiment data. The cross section saturation with the metric of "surface" LET is about half the cross section with "actual" LET as metric.

It is obvious that ignoring top metal material in an advance semiconductor device will underestimate the SEE when using LET as the metric in characterizing SEE induced by heavy ions. The top metal structure must be acquired for the evaluation of the single event effect of an advanced integrated circuit.

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